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The SI/PI Modeling and Measurement of Memory System by Probing on Top of DRAM Package

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Abstract

Continuous increase in the performance and speed of computer systems has led to more frequent field failures of memory systems. As a result, accurate measurement and modeling are becoming of utmost importance for memory vendors in order to guarantee the electrical reliability of their products. However, conventional on-chip measurement methodologies such as probing on the decoupling capacitor or a use of a test interposer between chip pads and measurement points. In this paper, we propose a novel method of measuring Signal Integrity and Power Integrity (SI/PI) performances of DRAM operation by directly probing on top of DRAM package. With this proposed test package, we prove the effectiveness of monitoring on-chip operation through simulation and measurement and hence, effectively enhance the level of SI/PI modeling and predictability of memory systems.

Author(s) Biography

WonSuk Choi is a Signal and Power Integrity engineer at Samsung Electronics where his responsibilities have been SI/PI analysis and sign-off of memory modules. His current research area includes SI/PI modeling and failure analysis for various high speed memory systems. He received the B.S. and M.S. degrees in Electrical Engineering from Yonsei University, Seoul, Korea.

SangKeun Kwak received the B.S. degree in Electronic Engineering from Soong-Sil University, Seoul, Korea, in 1992 and M.S and Ph.D. degree in Electronic and Electrical Engineering from Sungkyunkwan University, Suwon, Korea, in 2004 and 2012, respectively. In 1994, he joined Samsung Electronics, where he has been working in the area of memory testing and System Board SI/PI Modeling. His interests include SI/PI/EMI, high-speed interface circuits and noise-sensing circuits.

Dongyeop Kim received the B.S. and M.S. degrees in electrical engineering from Ajou University, Suwon, Korea, in 2007 and 2009, respectively. Since 2009, he has been with the Memory Division, Semiconductor Business, Samsung Electronics Co. Ltd., Hwasung, Korea, where he has been engaged in the research and development of memory module. His current research interests include signal integrity (SI) and power integrity (PI) co-simulation in high speed digital system.

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Jaeseok Park received a B.S. degree in Semiconductor System Engineering from the University of Sungkyunkwan, Suwon, Korea, in 2016. Since 2016, he has joined Samsung Electronics Device Solution division in Hwaseong, Korea, where he has been working in the System Board SI/PI Modeling. His current research interests include signal integrity (SI), power integrity (PI), electromagnetic interference (EMI) and system board design

Wonyoung Kim received a bachelor's degree in electronics engineering from Changwon University, South Korea, in 2006. He joined Samsung Electronics in 2005. He works for Samsung Electronics as a staff engineer in package design. He is responsible for package design and package process architecture. His interest is next-generation Package technology and the trend of Package products.

Sangnam Jeong received the B.S. and M.S. degrees in electrical engineering and computer science from the Hanyang University, Seoul, Korea, in 2006 and 2008. He joined the Samsung Electronics in 2011. He is working as a senior signal and power integrity engineer at Samsung Electronics. He is responsible for the electrical models, substrate design optimization, SI and PI of high speed packages. His interests include SI/PI/EMI on high speed packages and systems.

Daae Heo received the B.S. degree in electrical engineering from Sungkyunkwan University, Suwon, Korea, in 2011. Since 2011, she has been working as an engineer at Samsung Electronics. She is interested in layout optimization for SI and PI performance of memory products in high-speed and high-power system. And her interests range from package level to system level analysis.

Jonghoon J. Kim received the B.S., M.S., and Ph.D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2011, 2013, and 2017, respectively. He is currently with the Memory Division, Samsung Electronics, Hwaseong, South Korea, where he is involved with signal and power integrity analysis of DDR5 memory modules.

Sung Joo Park is a principal hardware engineer at Samsung Electronics. He received the Ph.D. in Electrical and Computer Engineering from the Georgia Institute of Technology, Atlanta, Georgia. His current research interests include the area of high-speed interfaces and memory systems.

Do-Hyung Kim received the M.S. degrees in Electrical Engineering from the University of Sungkyunkwan University, Suwon, Korea, in 2008. He is working as a Principal Memory sub-system engineer at Samsung Electronics. His main research interest is high speed channel, high density and low power memory module.

Jeonghyeon Cho received the B.S. and M.S. degrees in electronic engineering from the Sogang University, Seoul, Korea, in 1996 and 1998, respectively, and Ph.D degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2011. In 1998, he joined the Samsung Electronics, Gyeonggi-do, Korea, where he is currently a Principal Engineer. From 2014 to 2016, he was a chair person of a technical committee and a task group for high density memory modules affiliated to Joint Electron Device Engineering Council (JEDEC). His current research interests include the area of DRAM solution methodology that include signal integrity (SI), power integrity (PI), electromagnetic interference (EMI), and electrostatic discharge (ESD).

YongHo Cho received the Ph.D degree in electrical engineering from Korea Advanced Institute of Science and Technoloy (KAIST), Daejeon, Korea, in 1999. He is working as a vice president at Samsung Electronics and is responsible for the high speed DRAM product test. His interests include high speed DRAM IO and its test methodology, and DFT for mass production.

Jonghyoung Lim received B.S degree in Electronic Engineering from Hanyang University, Seoul, South Korea, in 1994. In 1994, he started working at Memory Division, Samsung Electronics, South Korea, where he was engaged in design of DRAM architecture and product engineering. In 1996, He developed the world's first technique for DRAM wafer burn in to increase the performance. He has been working as a Corporate Vice President since 2015, and he is currently a head of DRAM Solution team. His research interests include the development of the high density/speed memory module and management of the mass-products for server and mobile DRAM.

Jung-Bae Lee received the B.S., M.S., and Ph.D. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1989, 1991, and 1995, respectively. He joined Samsung Electronics, Hwaseong, South Korea in 1995 as a circuit design engineer in DRAM design team, where he participated in development of various DRAM products, including DDR, DDR2, DDR3, GDDR, LPDDR2, LPDDR3, and so on. He became the head of DRAM design team in 2012, the head of memory product planning & application engineering team in 2014 and the head of quality assurance in 2017. His leadership through various backgrounds, including design, product planning, and quality assurance enhance overall completeness of Samsung memory products. From 2019, he is leading DRAM Product and Technology. His research interests include design of high-speed low-power architecture for next-generation memory and noise phenomena in devices.

1. Introduction

The ever-rising demand for high-speed and high-performance computing systems has dramatically increased the data rate of main memory; 3200Mbps-DDR4 is now available in the market and DDR5 is expected to launch in the following year. Process refinement is in progress due to speed increase and low voltage use of semiconductor. As a result, the level of defect rate and development difficulty keeps on increasing [1]. Therefore, improved correlation between measurement and modeling of DRAM chip becomes highly important to predict and prevent memory-related failures beforehand.

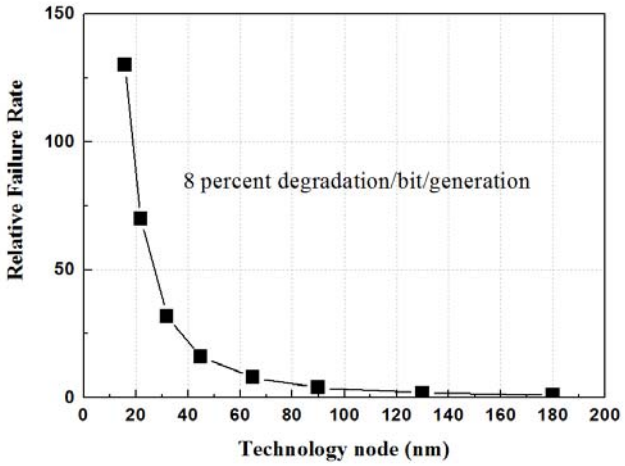


Figure 1: Soft-error failure-in-time of a chip (logic and memory) [1]

Conventional methodologies for probing on-chip signals are depicted in Figure 2. In Figure 2, a number of package balls are connected directly to on-chip power delivery network through package plated through-hole (PTH) vias and bumps. The package is then mounted on the PCB and accordingly, chip operation can be monitored by probing on the backside of the PCB. This on-chip sensing probe is isolated from the rest of power and ground network in the package and PCB [2].

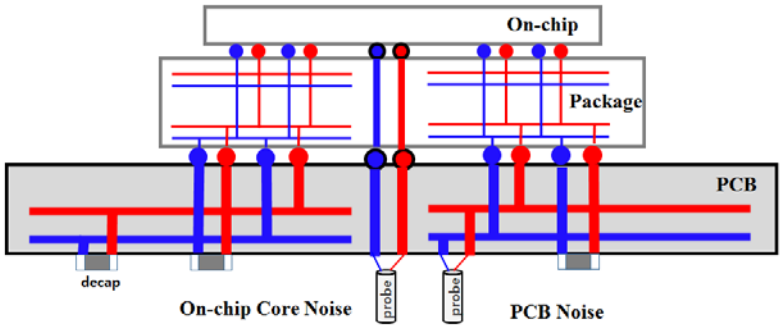


Figure 2: Cross section of chip mounted on package and PCB for on-chip PDN noise [2]

However, due to the substantial amount of physical lengths between chip pads and measurement points, the measured waveform is likely to show some discrepancies from the actual on-chip waveform. In order to overcome the physical length limit, there is a case where EMC of package is removed and micro probing is performed on on-chip pad. However, this method can only be applied if the chip is manufactured using bond wires; in other words, on-die probing solution cannot be applied to the majority of devices produced by flip chip technology. In addition, since there is a difficulty in measuring currents, a number of current prediction methods based on the network theory are being proposed using the actual voltage measurement results [3].

In this paper, we introduce a novel methodology to overcome the limitations of the conventional on-chip measurement techniques. The proposed method comprises of a test package that forms a probing pad on the top of a DRAM package, and the test module PCB that allows a direct measurement on the package ball side by probing on the back side of a dual in-line memory module (DIMM) PCB. The newly proposed test package uses laser drilling to penetrate hole in EMC so that SI/PI of on-chip can be directly probed and evaluated. Power noise and DQ were measured at the shortest distance from chip pad using new measurement hardware (probing package/probing MDL). In addition, we analyzed the difference between measurement and simulation to verify the accuracy of modeling. Further, we introduce a network-theory-based methodology that can be used to predict the current profile from the measured voltage on the probing package.

2. The Proposed Model

2.1. Design Model of Probing DRAM Package

In this paper, we designed a structure that forms a pad on the top side of a conventional DRAM package to measure the on-chip signal at the shortest distance, while maintaining the general package structure. Taking into account the size difference of chip die and package, we formed a probing pad at the package edge and drilled a via in package EMC to develop the proposed package capable of direct probing on the package top. In order to form a via in the package EMC, through mold via (TMV) technology, which is used for multiple package connections in mobile package on package (POP) products [4] [5], is adopted. The probing package is a branch structure composed of the package top pad (A), the package bottom ball pad (B), and the on-chip pad (C) as shown in Figure 3. The structure can be further illustrated as a daisy chain topology as shown in Figure 4.

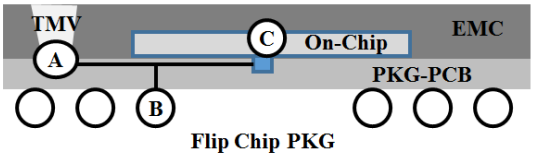


Figure 3: Cross section model of probing package

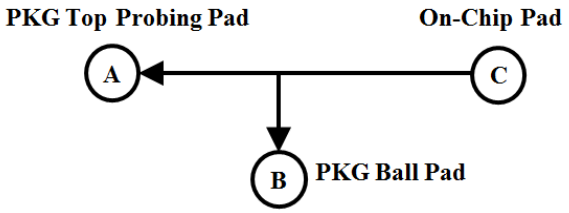


Figure 4: Block diagram of probing package

Figure 5 depicts the top floor plan of the proposed probing package, where some powers (Vdd, Vddq) and signals (DQ1, DQS_c) are configured to have the same structure as the one shown in Figure 3. For stable measurements, a GND pad is placed next to each probing pad as a pair. Figure 6 is a side view of the fabricated package, which confirms the use of the aforementioned structure shown in Figure 3. We will discuss the actual measurement results in the verification part.

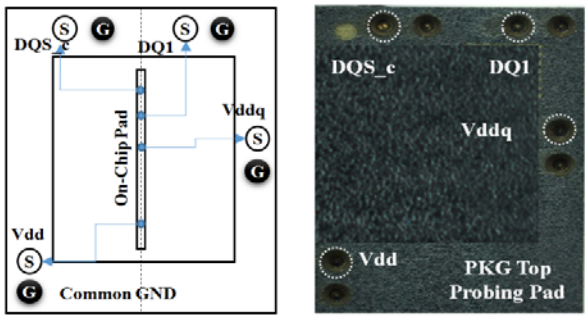


Figure 5: Probing package floor plan - conceptual (left) and real (right) top images

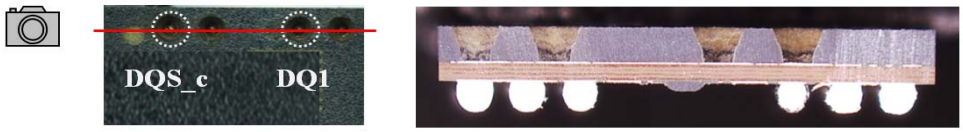


Figure 6: Package side structure analysis results

2.2. Design Model of Probing DIMM PCB

In order to check the normal operation of the probing package, we designed the special PCB on which the probing packages are mounted as illustrated in Figure 7. The on-chip power noise (C) that is supposed to be monitored at the probing package (A) is also detected on the backside of probing PCB. It passes through the original package ball (B) soldered down on the PTH via isolated from the conventional PDN. Then, it is seen at (D) as close as at on-chip without the effect from decap and power plane of the DIMM PCB.

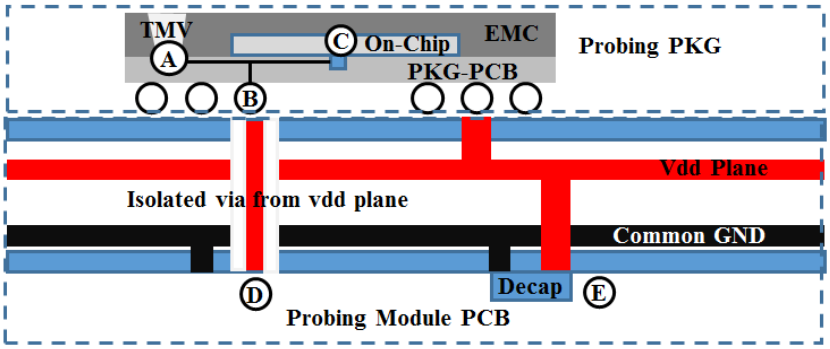


Figure 7: Probing module PCB structure with probing package

The signal and power of on-chip are measurable within the physically shorter distance both at the top of package and at the backside of PCB rather than at the conventional measurement points such as DQ series resistor (R_s) and decoupling capacitor (Decap) (E) using the proposed measurement hardware (Probing package and Probing module PCB). However, the usage of probing PCB is restricted only in case the backside is not mounted. On the other hand, the probing package is more flexible to monitor the on-chip pad signal effectively and unrestrictedly for high capacity DRAM module above 2 ranks. We will analyze the effectiveness of the probing package mounted at all DRAM locations for 1Rx8 Registered Dual In-line Memory Module (RDIMM).

2.3. Current Prediction Model Based on Measurement Using Network Theory

Unlike voltage waveforms, it is highly difficult to directly measure the amount of current consumed during DRAM operation of the memory module. One general way to measure the DRAM consumption current is to measure the average current value using automatic test equipment (ATE); however, it is almost impossible to extract the accurate current profile.

In this paper, we would like to adopt a methodology that can be applied to overcome this difficulty in extracting the current profile [6]. Recent studies have proposed some methodologies using network theory [3] for predicting current values in structures where direct measurement of current is difficult.

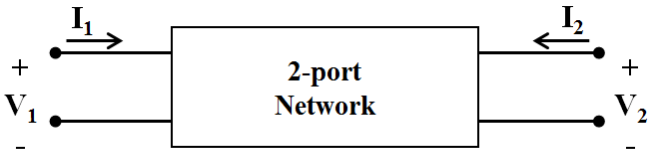


Figure 8: Two-port network equivalent circuit block diagram

$$V_1 = Z_{11} \times I_1 \quad + Z_{12} \quad \times I_2 \tag{1}$$

$$V_2 = Z_{21} \times I_1 \quad + Z_{22} \quad \times I_2 \tag{2}$$

$$Vtotal = \quad \sum Z \times I \tag{3}$$

In the circuit block diagram shown in Figure 8, the relationship between current and voltage at each port can be expressed by (1), where voltage is calculated as the product of impedance and current. If there are many current sources, the resulting voltage can be calculated as the total sum of the voltages generated by each current source. Assuming we know the measured voltage waveforms and the input/transfer impedance with respect to the current source, the value of the current source can be extracted [6].

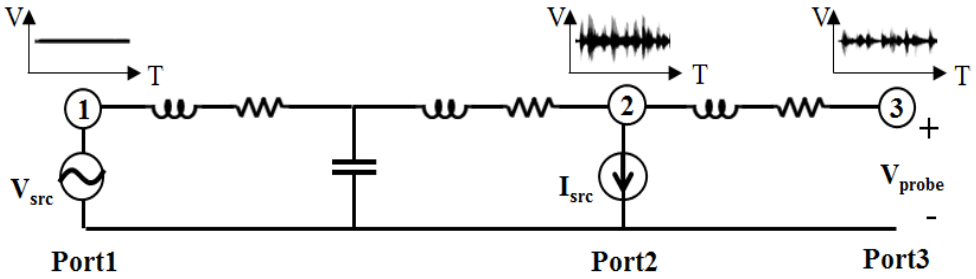


Figure 9: Equivalent circuit for source current prediction by voltage measurement

$$V_{probe}(f) = H_{31}(\mathrm{f}) \times \quad V_{src}(\mathrm{f}) \quad + Z_{32}(\mathrm{f}) \quad \times I_{src}(\mathrm{f}) \tag{4}$$

$$I_{src}(f) = \quad \frac{1}{Z_{32}(f)} \times [V_{probe}(\mathrm{f}) - H_{31}(\mathrm{f}) \times V_{src}(\mathrm{f})] \tag{5}$$

$$I_{src}(t) = FFT^{-1} \quad [\ \frac{1}{Z_{32}(f)} \times \left[V_{probe}(\mathrm{f}) - H_{31}(\mathrm{f}) \times V_{src}(\mathrm{f})\right]] \tag{6}$$

Figure 9 depicts a simple circuitry consisting of 3 ports, where the voltage (V_{probe}) at port 3 is calculated using the voltage source (V_{src}) of port 1 and the current source (I_{src}) of port 2 by the equation expressed in (4). In (4), H_{31} (f) and Z_{32} (f) are voltage transfer functions between port 1 and port 3 and the transfer impedance between port 2 and port 3, respectively. Rearranging (4), the current spectrum at port 2 can be obtained as expressed in (5). Lastly, taking this through inverse fast Fourier transform (IFFT) will result in the extraction of the time-domain current profile, as expressed in (6). For accurate extraction of the current source, accurate modeling and measurements of the functions, H (f) and Z (f) of the channel, and the voltage source V_{src} is of utmost importance. However, in reality, errors are bound to occur due to finite time and frequency ranges. If there are multiple current sources to be considered, one must create a simultaneous equation incorporating these to find a solution.

3. Simulation Results

The PI / SI simulation models and results of this paper are as follows.

3.1. PI Simulation Model and Method

Figure 10 shows the power delivery network (PDN) modeling of 1Rx8 RDIMM with probing package and probing module PCB in the ATE system. The simulation model of PDN consists of DC power, ATE board, ATE socket, probing module PCB, probing DRAM package and chip power model (CPM) [7] [8]. In this paper, we renamed isolated power nets as PVdd and PVddq to distinguish from Vdd and Vddq of the conventional PDN and wrote all the probing node names of real test hardware in italic font to make it clear.

We analyzed the Vdd power noise caused by DRAM refresh (Idd5) operation; therefore, marked probing points of Vdd power inside emphasizing square with number. Three probing node names were defined as follows; Decap on the module PCB which is the conventional probing node is Decap_Vdd. The probing point of the module PCB where the opposite side of DRAM mounted is Prob_MDL_PVdd. The probing point on top of DRAM package which is new in this paper is named as Prob_PKG_PVdd.

ATE board, probing module PCB, and probing package are scattering parameter (S-parameter) based models extracted from the post layout design. Both Cadence PowerSI™ and Synopsis Hspice™ are used for the modeling tool and transient circuit analysis tool respectively. The S-parameter of each component is converted to the broad band spice (BBS) model to avoid an error in the transient simulation. We reflected actual DRAM on-chip PDN characteristics based on CPM and, in real, applied the equivalent model of CPM to save simulation time.

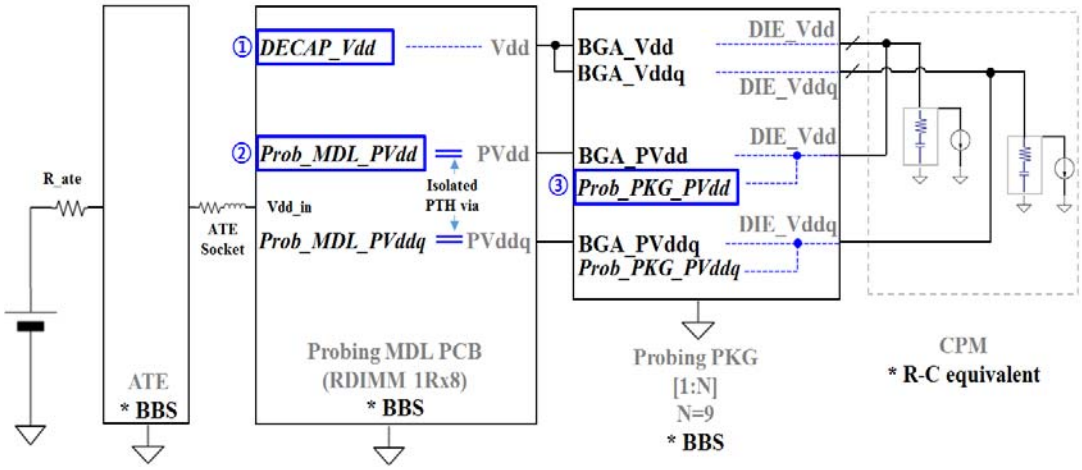
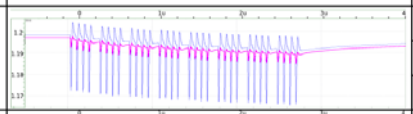
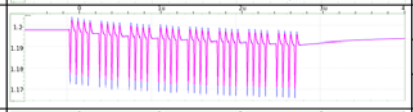
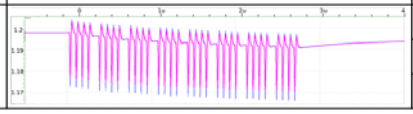


Figure 10: PI simulation block diagram

As mentioned above, we focused on the DRAM refresh (Idd5) mode with the largest core current consumed in this paper. Idd5 operates 8-burst according to the spec and consumes current continuously. The Vdd voltage, meanwhile, drops continuously from the reference voltage until the current consumption is halted. We simulated the time period including idle mode that the current is consumed no longer after Idd5 mode, therefore, the Vdd is restored to the reference voltage. The drop of voltage (V_{drop}) by the Idd5 mode was defined by subtracting the minimum operating voltage (V_{min}) from the DC voltage (V_{dc}) at each probing point and compared the PI characteristics among them.

3.2. PI Simulation Results

In DRAM Refresh (IDD5) mode, core circuit operation is responsible for the most of current consumption. Therefore, core switching current (peak, mA unit) is much larger than I/O switching current (peak, uA unit). As a result, it is crucial to predict the change of Vdd power noise by the core operation for the optimization of system PDN design.

Probing Point	PI Simulation : Vdd drop by Refresh Mode (Idd5)	V_{drop} [mV] = V_{dc}-V_{min}			
		Probing Point		DRAM Pad	% of DRAM pad
① Decap_Vdd (conventional)		V_{dc}	1197.0	Vdc :1198.2 Vmin :1166.8 Vdrop : 31.4	38.5 %
		V_{min}	1184.9		
		V_{drop}	12.1		
② Prob_MDL_PVdd (conventional)		V_{dc}	1197.9		87.8 %
		V_{min}	1170.3		
		V_{drop}	27.6		
③ Prob_PKG_PVdd (proposed)		V_{dc}	1197.9		87.5 %
		V_{min}	1170.4		
		V_{drop}	27.5		

Sim. at Probing Points Sim. at DRAM Pad

Figure 11: PI simulation results for Vdd (Core) power noise (by Idd5) at each probing point compared with DRAM pad

Figure 11 is the simulation results of the Vdd power noise at each probing point compared with that at DRAM pad. The V_{drop} at decap (Decap_Vdd), probing module PCB (Prob_MDL_PVdd) and probing package (Prob_PKG_PVdd) are calculated as 12.1 mV, 27.6 mV and 27.5mV by subtracting V_{min} from V_{dc} respectively. Based on 31.4mV as 100% at DRAM pad, the relative ratio of Vdd power noise at each probing position are 38.5% for decap, 87.8% for probing module PCB and 87.5% for probing package. From the above simulation results, we draw two meaningful conclusions as follows.

First, we are able to predict on-chip power noise more than twice as accurate at the proposed probing position (probing package, 88% of on-chip Vdd noise) as at the traditional probing position (decap, 38.5% of on-chip Vdd noise). Because the test hardware structure of the probing package and module PCB proposed in this paper has isolated power network from the original one, by using this hardware, we can monitor the

on-chip noise as close as possible to the real noise at DRAM pad without decrease of magnitude due to the decap effect of the conventional PDN. Second, we prove the effectiveness of the probing package by comparing the power noise level of it with that of probing module PCB. From the fact they are close together, we confirm that the probing package is effective to monitor the on-chip noise just like we first designed it.

3.3. SI Simulation Model and Method

Figure 12 shows the 1-Byte of DQ-Write channel modeling for 1Rx8 RDIMM with probing package and probing module PCB in the ATE system. The simulation model of DQ write operation consists of voltage source, input driver, ATE board, ATE socket, probing module PCB, probing package and DRAM IBIS receiver model for 60 ohms termination in order. We extracted S-parameter models of DQ 1-byte group (Byte0) from the post-layout design files of ATE board, probing module PCB and probing package respectively. The connection between DRAM package and module PCB is determined by reflecting the DDR4 package ball map defined in JEDEC [9].

For 1Rx8 RDIMM of our study, so is as shown in Figure 12. As PI simulation, we emphasized the real probing nodes in square with number (DQ6 in probing module PCB and DQ1 in probing package in this paper) and wrote all the probing node names in italic. Three probing node names were defined as follows; Damping DQ resistor on the module PCB which is the conventional probing node is Rs_DQ6. Prob_MDL_DQ6 is the probing point of the module PCB where the opposite side of mounted DRAM. The probing point on top of DRAM package which is new in this paper is named as Prob_PKG_DQ1.

In Figure 13, in order to understand DQ channel of the test hardware vividly, we've got an image of DQ6 only, all the way from the module PCB tab to DRAM pad using 3D modeling tool; Ansys HFSS^{TM}. We notice the order of transmission of DQ write signal and analyze the SI characteristic at each probing point more intuitively from the image.

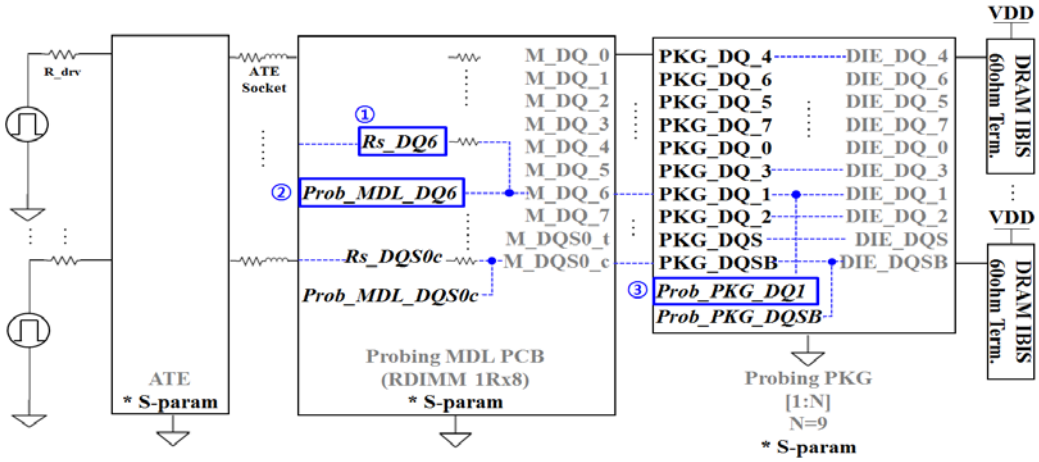


Figure 12: SI simulation block diagram; DQ-Write, 1-Byte (Byte0)

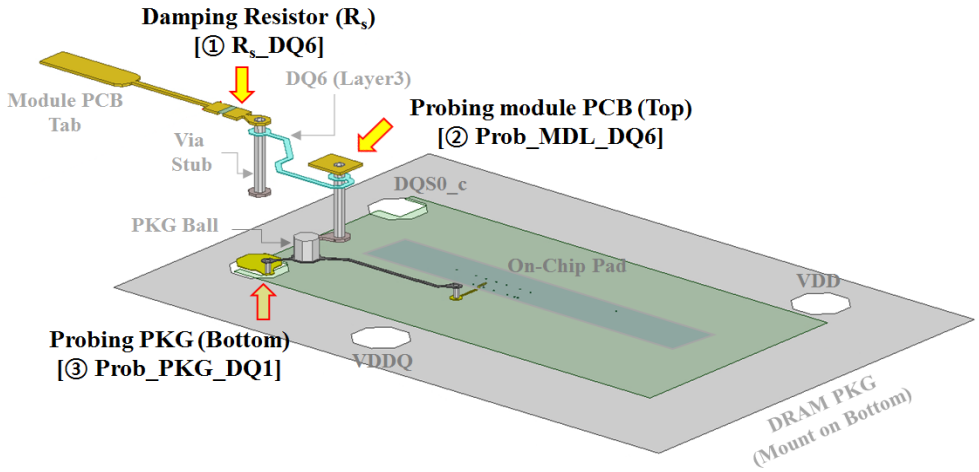


Figure 13: HFSS image of DQ6 channel of test hardware

3.4. SI Simulation Results

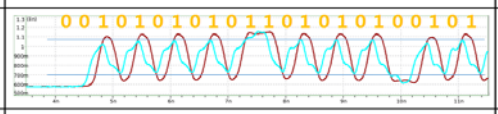
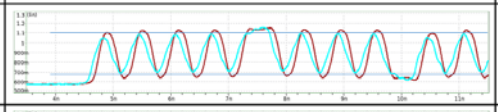
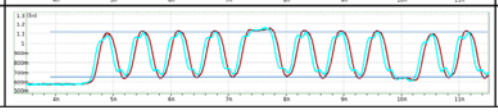
Figure 14 shows simulation results of DQ-write operation with simple input pattern applied to the proposed structure in this paper. We excited single bit toggling pattern sequentially to the channel to see how much the signal is attenuated per probing position due to inter symbol interference (ISI) in general. Based on 100% (493mV) of signal magnitude (Vp-p) at DRAM on-chip pad, the percentage of Vp-p by probing points is as follows. It is 72% (353 mV) at DQ damping resistance (R_S_DQ6) of the conventional probing point, 84% (412 mV) at probing module PCB (Prob_MDL_DQ6) and 92% (453 mV) at probing package (Prob_PKG_DQ1) of the proposed probing point. From the simulation results in Figure 14, we conclude that signal prediction at the nearest probing point shows the closest to the on-chip pad signal.

Therefore, probing at top of package is most effective way to monitor and estimate the on-chip operation for DQ-Write case. Considering the distance from each probing point to on-chip pad, it is reasonable timing difference is proportional to how far from the pad they are physically. Figure 15 shows the DQ Write simulation results in case pseudo random bit sequence (PRBS) is excited as input vector to predict the noise pattern of channel in the system. In general, we measure the DQ eye diagram by the maximum size of vertical and horizontal inside the open eye window. They are called as the eye height (EH) and the eye width (EW) respectively. The operating margin of the system is validated with the EH and EW of the eye window.

In Figure 13, we looked into the channel structure of DQ6 to have deep dive understanding of the results. The reflection from via stub near the damping resister (R_S_DQ6), which is 83% long of total via length, is somewhat related to SI degradation through the entire channel. (Via stub length: 1.166mm, Total via length: 1.402mm) We simulated how much SI could be improved by removing via stub effect by applying back-drilling to PCB as results shown in Table 1. Approximately 3~5% gain of voltage margin

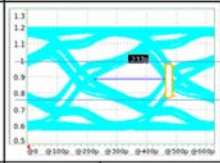
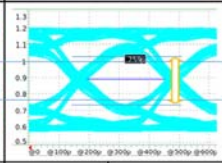
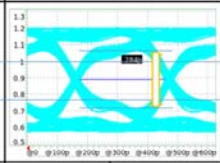
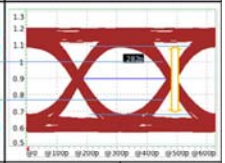
were obtained by decreasing reflection from via stub per probing point. However, negative effect from via stub is not sufficient to explain why EH at damping resistor is only 60% of that at the DRAM pad.

To realize the root cause of it, comparing EH at each probing point with that at on-chip pad in accordance with the physical distances is meaningful to explain why the nearest probing position is effective to monitor on-chip signal. Based on the EH at on-chip, the farthest probing spot of damping DQ resistor (R_S_DQ6) has 59% EH of on-chip. The medium distanced spot of the probing module PCB (Prob_MDL_DQ6) has 74% EH of on-chip. The nearest monitoring point of the proposed probing package (Prob_PKG_DQ1) has 85% EH of on-chip. As summarized in Table 1, the physical distance from DRAM pad is the major clue for our question; SI at each probing point is reciprocally proportional to the distance from DRAM pad. From the simulation results of this chapter, we prove that the proposed probing package is also effective to monitor and estimate on-chip signal in terms of SI as well as PI.

Probing Point	SI Simulation Simple Pattern (DQ6, Write, 3200Mbps)	Vp-p [mV] (Single Bit)		
		Probing Point	DRAM Pad	% of DRAM pad
① R_S_DQ6 (conventional)		353	493	72 %
② Prob_MDL_DQ6 (conventional)		412		84 %
③ Prob_PKG_DQ1 (proposed)		453		92 %

Sim. at Probing Points Sim. at DRAM Pad

Figure 14: SI simulation results at each probing points compared with DRAM pad applying simple pattern for DQ-Write

	① R_S_DQ6 (conventional)		② Prob_MDL_DQ6 (conventional)		③ Prob_PKG_DQ1 (proposed)		DRAM Pad	
Eye Diagram (DQ6, Write, 3200Mbps)								
Item [Unit]	EH [mV]	EW [ps]	EH [mV]	EW [ps]	EH [mV]	EW [ps]	EH [mV]	EW [ps]
Value	242	237	302	259	351	284	411	282
% of DRAM pad	59%	84%	73%	92%	85%	100%	100%	100%

Sim. at Probing Points Sim. at DRAM Pad

Figure 15: SI simulation results by probing point using PRBS7 pattern for DQ-Write

Probing Position		DRAM pad	Prob_PKG _DQ1	Prob_MDL _DQ6	R_s_DQ6
EH (% of DRAM pad, the original)	The Original	100.0 %	85.4 %	73.5 %	58.9 %
	Back-drilled (Removing Via Stub)	103.2 %	89.5 %	78.6 %	62.8 %
	Difference (EH gain by back drill)	3.2 %	4.1 %	5.1 %	3.9 %
Distance from DRAM pad [mm]		0	1.45 mm	1.77 mm	5.37 mm

Table 1: Comparison of % of EH at each probing point based on DRAM pad in accordance with the physical distances including via stub effect

3.5 Simulation Results for Current Prediction Using Network Theory

In this paper, Refresh current (Idd5) of DRAM was extracted by applying this method. We have reviewed the consistency with the chip power model (CPM) of DRAM obtained through the Spice simulation model. Figure 16 is a representation that 1 rank x8 RDIMM is mounted on the socket of ATE board. The 1Rx8 RDIMM is an active device that consumes current. There are 9 DRAM's and 1 RCD in the RDIMM and all the power is supplied from ATE through cable. When the DRAM's perform the refresh operation, the measurement voltage value at the probing package is used to restore the Idd5 of the DRAM.

If all DRAM's in 1Rx8 RDIMM do refresh operation at the same time, RCD current can be assumed to be 0 because DRAM current occupies most of current consumption. So, assuming that the voltage source of the ATE is ideal DC, the $H_{transfer}$ (f) x V_{src} (f) term in Equation 4 can be neglected in the formula for AC calculation because V_{src} (f) affects only DC.

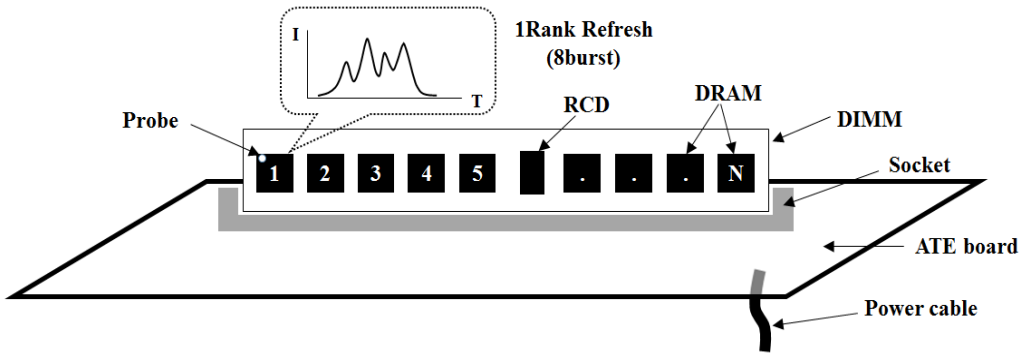


Figure 16: DRAM voltage measurement environment using 1Rx8 RDIMM

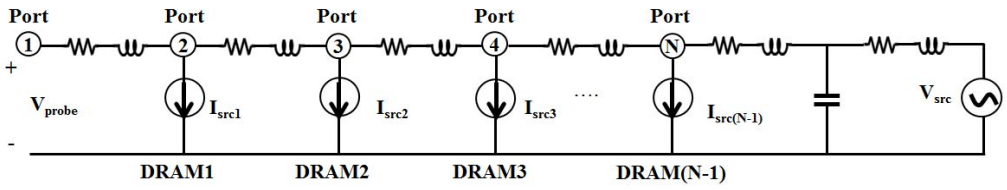


Figure 17: Z-Matrix equivalent circuit model using 1Rx8 RDIMM

$$V_{probe}(f) = \sum Z_{transfer}(f) \times I_{src}(f) \tag{7}$$

Figure 17 is an equivalent circuit made by assuming that the V_{probe} is port 1, and each DRAM stage is port 2 to N, and is expressed in Equation 7. In this equivalent circuit, the Idd5 relation of the measurement voltage value and DRAM can be summarized as follows. The current Idd5 that each DRAM consumes during refresh operation can be obtained by dividing the probed voltage by the sum of the transfer impedance from each DRAM, which is the cause of the current source to the probe point. For 1Rx8 RDIMM, the number of port N is 10 based on Figure 17 above, and the formula using this can be summarized as follows.

$$V_{probe}(f) = Z_{1,2}(f) \times IDD5_{dram}(f) + Z_{1,3}(f) \times IDD5_{dram}(f) + \cdots + Z_{1,10}(f) \times IDD5_{dram}(f) \tag{8}$$

$$V_{probe}(f) = \sum Z_{transfer}(f) \times IDD5_{dram}(f) \tag{9}$$

$$IDD5_{dram}(f) = V_{probe}(f) / \sum Z_{transfer}(f) \tag{10}$$

$$\sum Z_{transfer}(f) = Z_{1,2}(f) + Z_{1,3}(f) + \cdots + Z_{1,10}(f) \tag{11}$$

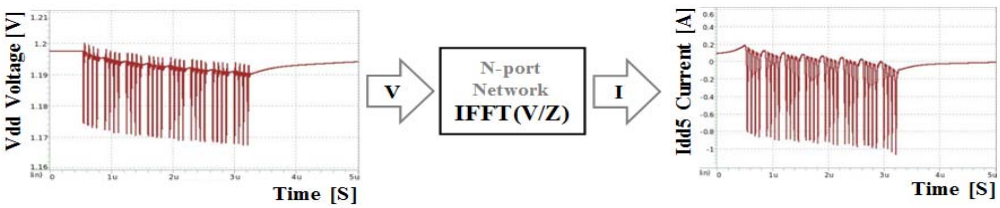


Figure 18: Simulation results for current prediction by probing voltage

Figure 18 shows the simulation results of predicting I_{src} with the results of the V_{probe} using the formula developed above. The V_{probe} is the simulation result at the probing package node and I_{src} is predicted by using the V_{probe} and PDN network as input for Equation 7.

4. Verification Results

In this chapter, we introduce the structures of the package and module, as well as the ATE evaluation system used to verify the model presented in this paper.

4.1 Verification Scenario

For the verification and analysis of the model presented in this paper, the following scenarios have been verified. The power voltage and signal waveforms were measured using the Vdd / Vddq / DQ pads on the proposed package, and were compared with the post-layout simulation results reflecting DDR4 package and 1Rx8 RDIMM model. The comparison assumes that the DC power of ATE is noise-free, and aims to improve the accuracy of the simulation model by analyzing the difference between the measurement of Vdd pad voltage and DQ eye and the simulation prediction.

For PI verification, we proceed with the Idd5 condition based on JEDEC Spec, and compare the on-chip noise measured using the proposed probing package with the CPM model noise prediction obtained through post-layout simulation. The procedure for SI verification is to first measure the eye by implementing an I/O input pattern under PRBS7 condition for write operation, and then compare it with the post-layout-based simulation results. The following sections will introduce the measurement environments and simulation input vectors for each measurement.

4.2 ATE Hardware and Software Configuration for SI/PI Measurement

The hardware of the measurement system was configured as ATE, test board, 1Rx8 RIMM with probing package, oscilloscope, and probe. The software related to DRAM operation has been configured to incorporate Idd5 condition (JEDEC Spec) [9] for PI measurement, and DDR 3200Mbps PRBS7 I/O pattern for SI measurement.

Figure 19: Hardware configuration for model verification (Test board and 1Rx8 RDIMM)

Figure 19 shows the hardware structure of the evaluation environment, which is comprised of a test board for evaluating module DIMM, DIMM Socket of the ATE test board, and 1Rx8 RDIMM assembled with the probing package. The evaluation ATE system is Teradyne's Ultraflex equipment that can evaluate at the maximum frequency of 8Gbps [10].

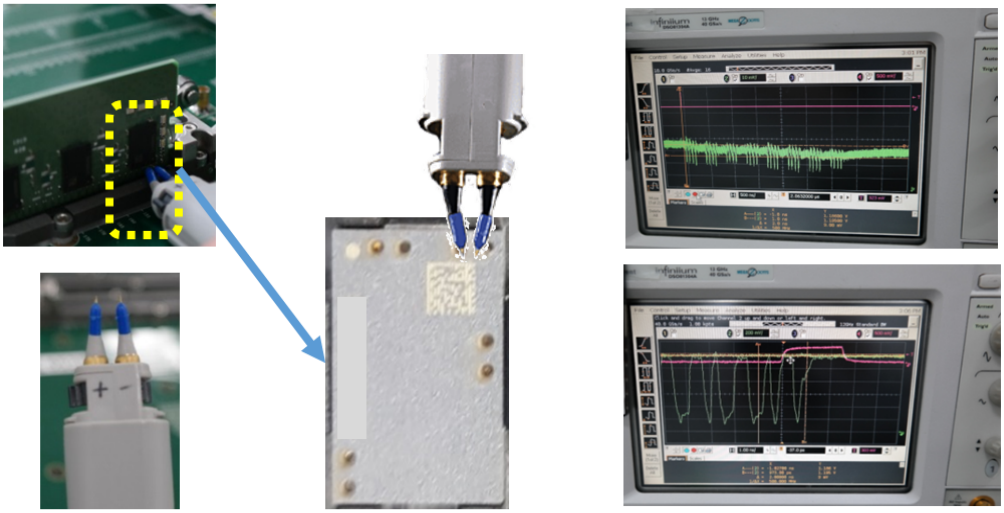


Figure 20: Example of oscilloscope and probe tip for measurement

Figure 20 is a picture of the oscilloscope and probe tip used for SI/PI measurement. Using the probe tip at the bottom left of the figure, PI and SI are measured on the probing pads formed on the top surface of the probing package, and there is a photograph of Vdd and DQ signal waveforms observed in the oscilloscope as shown in the right figure. The oscilloscope used for verification is Agilent's Infiniium DSO81304A, and probe tip used for the measurement was Agilent 1134A type.

The test condition of DRAM chip for PI measurement reflects the JEDEC-based Idd5 (burst refresh current) condition, and I/O test pattern for SI measurement is pseudo-random bit sequence (PRBS). This sequence is 2^7-1, which uses 127 bit patterns to configure the software that tests the signal. The reason for using the PRBS7 is that it is relatively easy to implement the input vector for the ATE test and simulation.

4.3 SI/PI measurement results of 1Rx8 RDIMM

The measurement was performed on the right DRAM chip on the 1Rx8 RDIMM shown in Figure 21 for comparison with simulation, and the old measurement positions (No.1, No.3) and the suggested positions (No.2, No.4) of this paper were measured and compared with one another. The old probing positions are No.1 and No.3, where No.1 is the decap position close to DRAM, and No.3 is the damping DQ resistor (R_S) position over the tab pad of DIMM. The position of the proposed model is No. 2 and No. 4, where No. 2 is the package top Vdd pad, and No. 4 is the package top DQ pad.

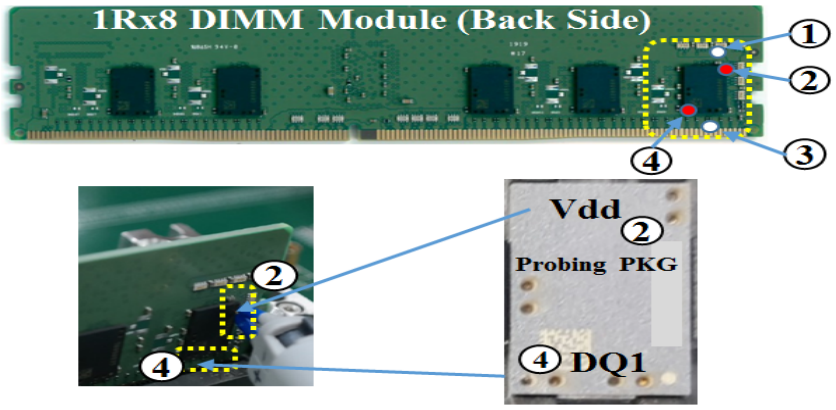


Figure 21: Definition of SI/PI probing position

4.3.1 PI Measurement Results

With the previously mentioned Idd5 conditions, the PI measurement results are shown in Figure 22. The measurements were performed at the conventional measurement position (decap) and the proposed model (top pad of probing package). The amount of voltage drop in the old measurement position is about 11.4 mV, and the measurement result in the newly proposed position is approximately 30.8 mV. In terms of on-chip noise measurement, which excludes the on-DIMM decap effects, it is predicted that the proposed position can better reflect the real on-chip noise. The analysis of the results will be dealt with at the analysis section.

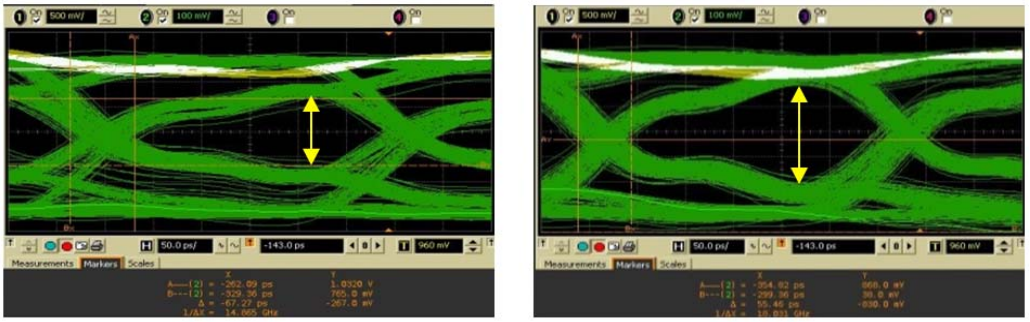
P1: Decap (11.4 mV)

P2: Probing PKG_Vdd (30.8 mV)

Figure 22: PI measurement results per probing position for 1Rx8 DIMM

4.3.2 SI measurement results

The SI measurement was performed with PRBS7 input pattern at DDR 3200 Mbps, of which the result is shown in Figure 23. In the conventional measurement position, R_S resistance, the DQ eye height is measured as 267 mV, and the result in the newly applied package position is 358 mV. Measuring near DRAM pad seems to have a smaller distortion in analyzing eye waveform, and the disparity between simulation and measurement will be summarized in the analysis section.



P3: DQ RS EH(267 mV)　　P4: Probing PKG DQ EH(358 mV)

Figure 23: SI measurement results per probing position for 1Rx8 DIMM

4.3.3 Comparison of Measurement Results for the Proposed Model

Comparing the conventional measurement with the proposed measurement method is shown in Figure 24. As a result of the measurements, we noticed 170% increases in noise from PI measurement, and confirmed 34% improvement from SI measurement.

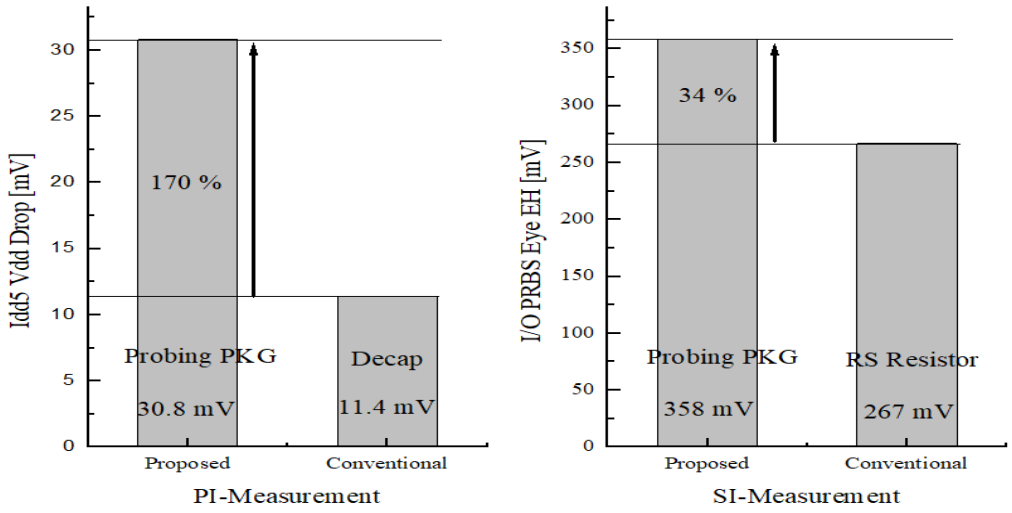


Figure 24: Comparison results of 1Rx8 DIMM SI/PI evaluation

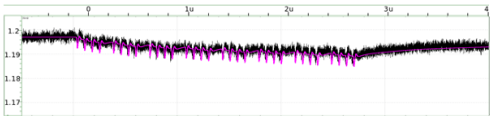
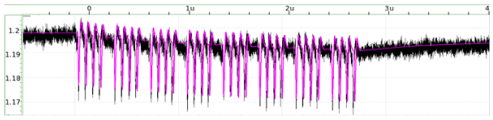
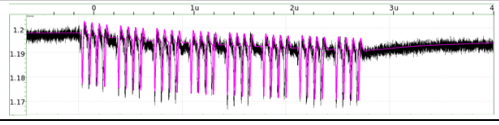
5. Analysis and Discussion

In this chapter, we summarize our study on the new probing method. We already proved that the proposed probing method with probing package is effective on monitoring on-chip signal and power noise through simulation and measurement results. We review the difference of the two and discuss the reason.

5.1 Analysis of Differences for PI Simulation and Measurement by Probing Point

Figure 25 shows PI comparison with V_{drop} by Idd5 between simulation and measurement. The V_{drop} per probing position has similar tendency in simulation and measurement. The error based on measurement ranges from 6% in old probing position (decap) to 11% in new (probing package).

The main reason for V_{drop} error is the high frequency components of noise waveform shown in the measurement were not included in the simulation model. In Figure 26, simulation and measurement waveforms of V_{drop} at probing package are represented in time domain (left) and so are they in frequency domain (right) transformed by Fast Fourier Transform (FFT). In time domain, simulation waveform represents Idd5 operation by the interval defined in spec (tRFC: 350ns) and the four consecutive refresh operations in the tRFC. These are also found in measurement waveform in the same manner. However, high frequency components shown in the measurement are not in the simulation. In frequency domain, even though low frequency trends of tRFC and four refresh modes are correlated in 2.8MHz and 14.2MHz spectrum for simulation and measurement, high frequency trends are not above 150MHz. This is the reason there is difference in simulation and measurement results.

Probing Point	PI Correlation : Vdd drop by Refresh(Idd5)	Vdrop [mV]		Error [%] (|Diff|/ Meas *100)
		Meas.	Sim.	
Vdd Decap (conventional)		11.4	12.1	6.1 %
Probing PCB (conventional)		31	27.6	10.9 %
Probing PKG (proposed)		30.8	27.5	10.7 %

Measurement Simulation

Figure 25: PI (Idd5) comparison results between measurement and simulation

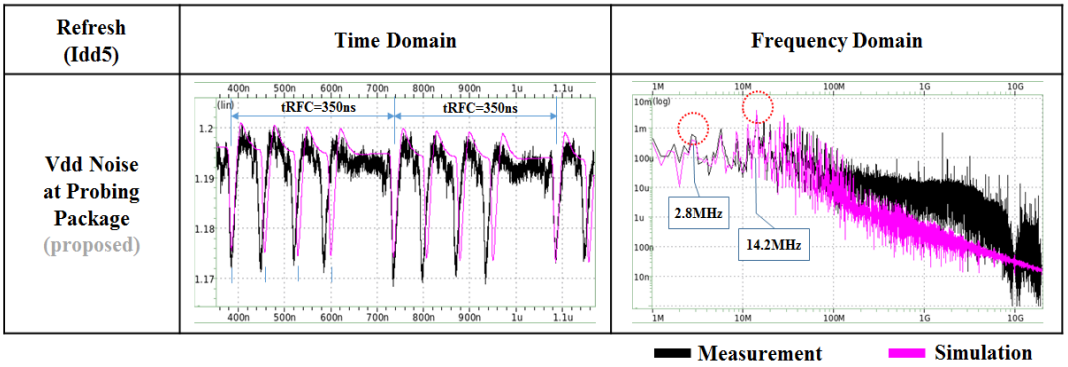


Figure 26: Comparison of Vdd noise at probing package in time and frequency domain

5.2 Analysis of Differences for SI Simulation and Measurement by Probing Point

Next, we discuss the difference of simulation and measurement regarding SI. Figure 27 summarizes the comparison between simulation and measurement of DQ Write at each probing point in case PRBS pattern is excited. In terms of the voltage (EH) of the eye diagram, the difference between measurement and simulation is 7.8% in the conventional probing position (damping DQ resistor) and 1.7% in the new position (on top of probing package). Like PI comparison, the EH of DQ write per probing position has similar tendency in simulation and measurement.

In this chapter, we evaluated the gap between measurement and simulation. Even though there is difference between them, we prove that prediction of on-chip operation is available by using the new probing package with enlarged magnitude for SI/PI within approximately 10% error of measurement.

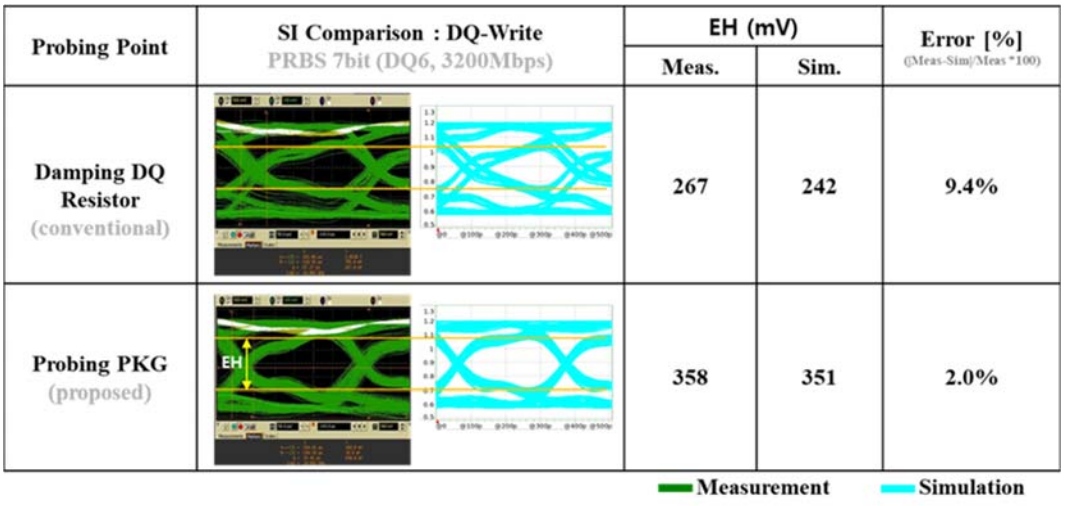


Figure 27: SI (PRBS) comparison results between measurement and simulation

6. Conclusions

In this paper, a new DRAM package for measuring and estimating SI and PI at on-chip is introduced and its effectiveness is verified through simulation and measurement. By using this novel package, we can analyze the chip operation more exactly and enhance the level of SI/PI modeling. This effort is expected to further allow accumulation of sophisticated modeling library and eventually improve predictability of various memory systems in advance using simulation. Moreover, the measurement and SI/PI estimation methods at the top of probing package proposed in this paper can be extended for on-chip noise monitoring and analysis of double-side mounted DIMM products that are unmeasurable on the backside so far.

7. Acknowledgment

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