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EDA Flows and Modeling approaches to study analog-digital coupling

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Abstract

Noise coupling between analog/digital blocks on the chip is a key issue for signal/power integrity (SI/PI) engineers to analyze typically and is a key factor in deciding ground plane sharing/isolation on the die, package and PCB to meet performance specs. While it is possible to conservatively isolate ground planes to mitigate noise coupling to meet performance specs it adds to system cost in terms of BGA pin count and number of routing layers. In this work we discuss EDA flow based approaches to model analog/digital coupling at a system level to help practicing engineers in making the right tradeoff for their design

Author(s) Biography

Karthik Chandrasekar currently works at Seagate Technology as a Signal/power integrity engineer in the IC Packaging team. He has 17 years of combined industry and research experience as a hardware system engineer with various responsibilities such as Signal/Power integrity analysis, die/package physical co-design, Chip Power analysis, 2.5D/3DIC R&D effort program management and managing CAD teams developing analog circuit simulation flows.

Emmanuel Atta is a signal/power integrity engineer within Seagate's VLSI organization. His industry experience and expertise covers signal and power integrity simulation and validation of high speed serial and parallel interfaces.

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Gurdev Dhanota is a Principal Engineer at Seagate Technology. He has been working in HDD/SSD Storage field for 20+ years with various responsibilities from Board/System design to device characterization

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I. Introduction

Noise coupling between analog/digital blocks on the chip is a key issue for SI/PI engineers to analyze typically and is a key factor in deciding ground plane sharing/isolation on the die, package and PCB to meet performance specs. Simple lumped PDN modeling approaches and traditional EDA tool based approaches tend to have weaknesses in capturing the distributed nature of noise coupling at system level leading to pessimism in decision making to mitigate noise which leads to increase in product cost. While die level EDA PDN analysis tools have matured faster for accurate distributed PDN modeling the authors noted that Package/PCB EDA tools haven't quite kept up in this regard possibly because majority of analog/digital coupling occurs at die level. Some prior work has looked at weaknesses and enhancements needed from EDA tools to model packages/PCB's but not specifically in the context of analog/digital coupling [1]. Prior work on modeling analog/digital coupling has focused more heavily on studying benefits of suppressing PDN noise using decoupling capacitor optimizations and substrate noise coupling rather than looking at impact of Package/PCB layout itself [2, 3]. Figure 1 shows a common scenario which often presents itself in product design where one has to decide whether to share the ground or split the ground on package to reduce the interactions.

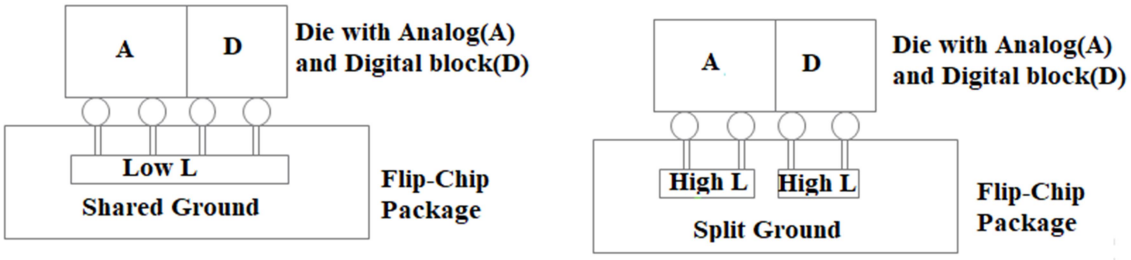


Figure 1: Shared Ground vs. Split ground in die/package co-design

While splitting the ground helps in noise isolation it can also lead to higher power/ground effective inductance (L) which introduces challenges in timing closure for critical nets. Particularly when analog blocks on the chip have higher sensitivity to noise then it becomes critical to model the package/PCB along with their interactions with die more accurately rather than relying on lumped models or traditional S-parameter models of the PDN which tend to have simulator convergence issues in the time domain. Adaptation of existing Industry standard CAD tools was needed and multiple performance metrics were used to make engineering tradeoffs in mitigating noise coupling between analog/digital blocks. For example in the initial phase it was necessary to do simple package/PCB distributed DC IR analysis by injecting distributed current sources at specific points to study how the voltage gradient changed spatially between analog/digital blocks as a function of current stimulus and work with circuit designers to quantify the impact in terms of jitter sensitivity in ps/mV to understand noise sensitivity of the analog block. This process involved adaptations of existing default out of the box

CAD tool flows in terms of setting sources/sinks as they have inherent weaknesses.. In the second step custom SPICE model generation from existing EDA tools was needed for the power grid trading off accuracy and setup complexity. For example, it is more critical to have distributed bump port models on the die to accurately represent the PDN and model local effects in the proximity of the sensitive analog blocks accurately rather than create multi-port models on the package/PCB which raise solution complexity and also leads to invalid non-convergent models in the time domain. In this work authors go through couple of case studies to explain various tradeoffs in modeling approaches which led to better correlation of trends between simulation/measurements of noise coupling between analog/digital blocks. It was also observed that to first order frequency domain metrics like transfer impedance between 2 PDN's could be reliably used to assess analog/digital coupling when PDN was the main factor involved, however as problem complexity increased with multiple variables playing a part, then time domain SI/PI co-simulations with circuit level SPICE models were the only reliable way. This work presents the practicing engineer with insights on how existing CAD tools can be used with adaptations to model system level analog/digital coupling more reliably while avoiding common pitfalls and also validates the approaches presented with simulation/measurement qualitative performance correlation.

II. EDA Flows and approaches for modeling analog/digital coupling

1. EDA flows for system PDN modeling

Accurate modeling of system PDN requires models of detailed granularity to capture subtle interactions between die/package/pcb without going overboard on increasing complexity. Die level power model model contains current signatures and parasitic network distributed across a multiple-terminal equivalent circuit to reflect their temporal and spatial dependencies. The simplest element of the die level power model can be considered to be a serially-connected R_{die} and a C_{die}, in parallel with a current switch. More detailed model consists of all significant sources of capacitance in a chip, including parasitics and decoupling, are included in the chip model, as shown in the circuit of figure 2 below.

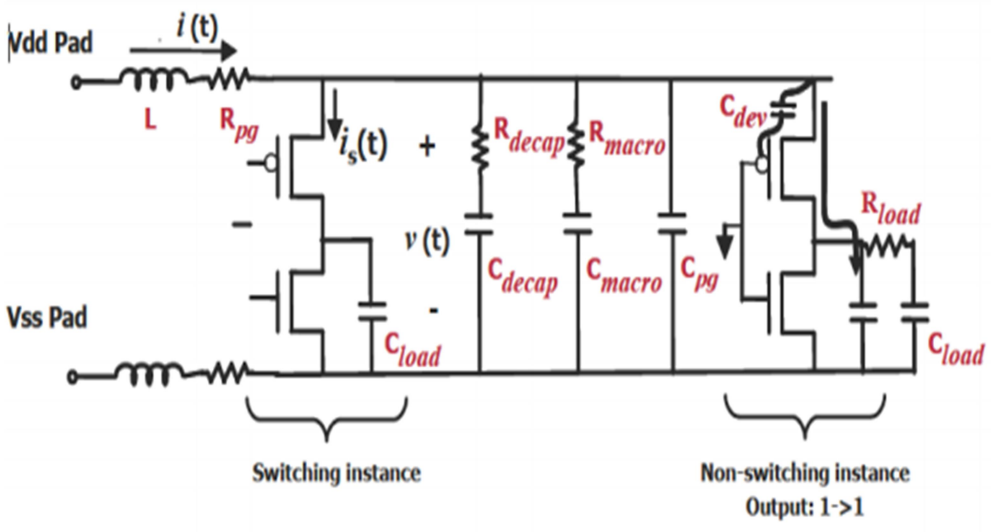


Figure 2: Die level power model

Die level power model consists of intentional decaps, intrinsic device decaps, signal loading capacitance and coupling capacitance between power and ground wires, from chip power model (CPM) extraction. For Analog and digital domain PDN analysis, we are more interested in the coupling information between those domains, and detailed parasitic information around that area. This requires multi-port model extractions around that area. To aid the analysis, we may add probe points on different nodes so that we may watch the performance at those nodes during PDN analysis. These die models are then hooked up to package/PCB models extracted with 2.5D or 3D field solvers. In applications where the focus is more on IO interface simulations or Core Power analysis S-parameter approaches may work fine on the package/PCB. However the authors note that in today's system-on-chips (SOC's) where it is common to split analog and digital ground on the die which are then re-connected back with different layout flavors on package/pcb these approaches have limitations as voltage gradients between different grounds can play a part in net contribution on timing jitter of critical signal nets. These effects are better captured in a SPICE model of the Package/PCB and require close partnership with tool vendors to generate models which are convergent and valid in the time domain. Validity can be checked by looking at frequency of PDN network oscillations and magnitude and decay time. Figure 3 shows block diagram of system level PDN model generation. While tools have capability to generate Package/PCB combined extracted models at this stage we have higher confidence with separately generated models.

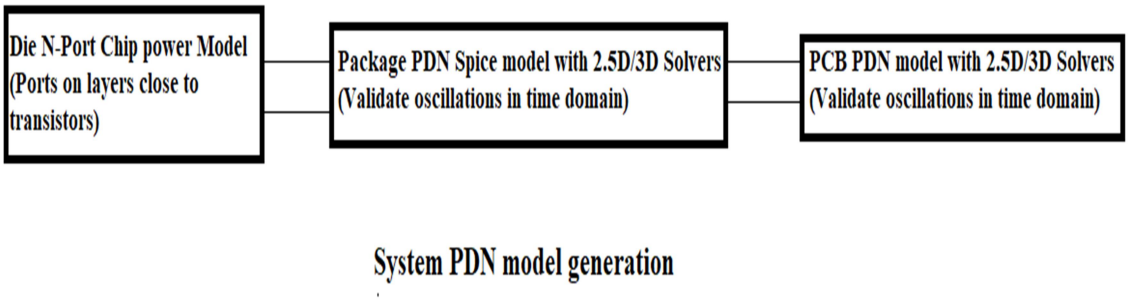


Figure 3: System PDN model generation flow of die/package/pcb

2. Modeling approaches to analyze Power/ground coupling between analog/digital blocks

Analyzing coupling between analog/digital blocks fundamentally hinges on capturing the transfer impedance between the two power domains accurately to start with. The basics of transfer impedance are well discussed in [4]. Simulating transfer impedance accurately requires careful port setup to ensure the interactions across the die and package and board are captured correctly. For example it is typical practice on the die to isolate analog and digital grounds while merging them on package or pcb. In this scenario we have to ensure that the models generated account for it by assigning isolated unique ports for the separate grounds on die. Both S-parameter based approaches and SPICE based models are able to generate comparable numbers for transfer impedance as shown in table 1 below for a set of three different simulation scenarios. Here peak impedance at PDN resonant frequency where coupling occurs is reported. At this point we still don't know which approach correlates better quantitatively; qualitatively both are able to capture the trends with SPICE model based approach working better in our application to study ground bounce in detail.

Design Sample	**S-parameter based transfer impedance (at resonance frequency)**	**SPICE model based transfer impedance (at resonance frequency)**
Simulation Scenario1	17mohms	66mohms
Simulation Scenario2	51mohms	116mohms
Simulation Scenario3	2mohms	50mohms

Table 1: Transfer impedance comparison between S-parameter and SPICE models

However while this helps in identifying the coupling mechanisms it still does not pin point specific design weakness unless you look at voltage gradient on both die and package. It is common practice to look at voltage gradient on the die as part of power sign-off to optimize power/ground mesh to meet DC potential drop (IR) specs. In general since copper is thick on package and pcb, traditional analysis assumes that fine-grained

voltage gradient on the package or pcb plays an insignificant role in amplifying or mitigating analog/digital coupling. Table 2 shows an example of voltage gradient plot generated for an example design. Here a step current source was injected on digital ground in EDA tool simulation and coupling on neighboring analog ground was monitored at a local point on package top ground stripe layer for scenarios when ground is shared vs. when it is isolated. In case of shared ground since there is more current from digital block sinking on the plane we see more voltage gradient vs. in the case of split ground only the local current of the analog block causes a smaller voltage gradient. Also the voltage gradient is a function of package layout resource allocation (# of layers, body size, die size etc...). Also it is important to not use "out-of-the-box" tool vendor provided DC IR drop analysis flows which do not reveal specific weaknesses in the design. Identifying hot spots in the context of analog/digital coupling requires injecting custom current sources at specific points in the design where stitching of ground planes happens between analog/digital blocks and studying local voltage gradients.

Design Example	**Voltage Gradient (in mV) across a 2mm span of ground stripe in package layout**
"Shared Ground"	6.2mV
" Split Ground"	1.82mV

Table 2: Package voltage gradient for shared vs. split ground

Even a few milli-volts can make an impact depending on noise sensitivity of the circuit under test and the effective localized resistance of the on-die power grid in relationship to the package/pcb. There could be designs where the on-die power grid is sufficiently strong and circuit is very robust to noise where any change on package or pcb has no impact whereas other scenarios where the impact is higher. It is important to analyze noise sensitivity of the circuit block under test by injecting power delivery network (PDN) sinusoidal noise at different frequencies in the design phase to identify shortcoming and take corrective action as needed. For example, high performance Phase locked loop circuits (PLL) requiring low long term jitter, could be affected by the disturbance in ground supply noise which is shared between the large digital IPs and sensitive analog circuits. Fig.4 depicts one such case, in which a digital block consuming a large (2A-3A) dynamic power is switched off and on rapidly causing a large disturbance in the ground net. This disturbance induces noise in the bias block, due to its limited power supply rejection ratio (PSRR)(>17dB), leading to large deterministic jitter in the VCO block. Passive filter R_filt1/C_filt1 help suppress the bias disturbance, but requires large area. Power supply disturbance can also lead to noise in the VCO due to limited regulator bandwidth and channel length modulation of transistor MA shown in figure 4. Large digital currents can pass through the ground net supplying the analog blocks, causing drift between MB and MA. To avoid this, care should be taken to place

them closely. The magnitude of deterministic jitter induced due to power supply disturbance can be estimated by obtaining the power spectrum of the disturbance and jitter sensitivity of the VCO with respect to ground noise. The sensitivity can be obtained by transient simulations with ground sinusoidal noise at various frequencies. Frequency domain simulations like Periodic transfer function (PXF) analysis can also be used to obtain the jitter sensitivity function. If the specifications for the deterministic jitter due to ground disturbance caused by digital switching activity are not met, using separate digital and analog ground balls on the package could be an option. Fig.5 shows jitter sensitivity to ground noise obtained from transient simulations for a representative analog block just to illustrate the relationship between PDN design and noise sensitivity.

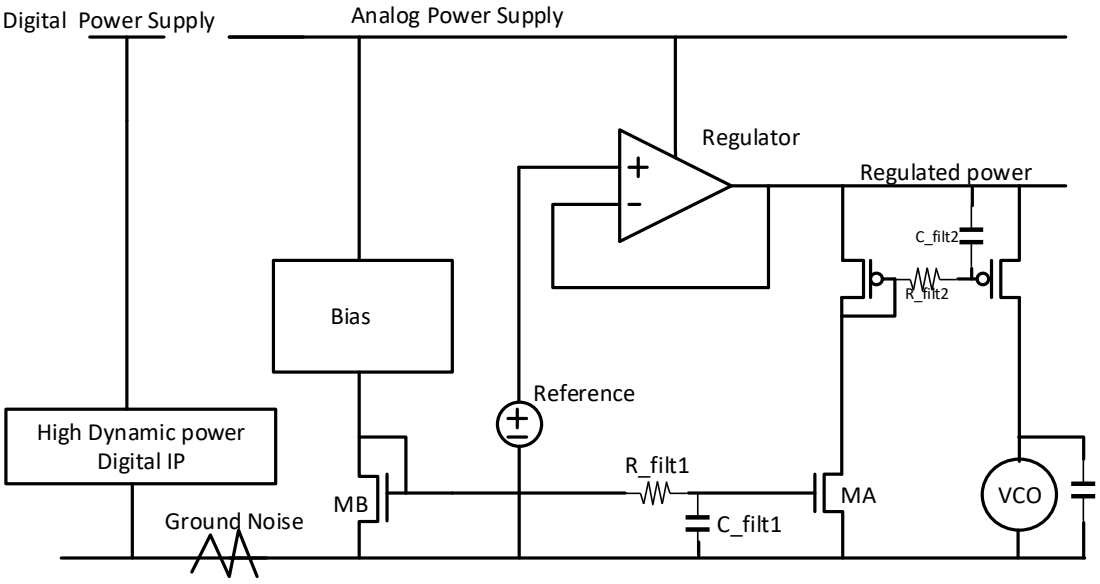


Figure 4: Ground disturbance effect on VCO and bias circuits of the PLL.

For this particular analog block the noise sensitivity expressed in terms of ps variation per mV of PDN noise peaks at 10MHz. So it is important for the power integrity engineer to take special care to engineer the PDN to behave well at these frequencies by reducing the impedance peak or moving the resonance frequency away to other frequencies where the block is not as sensitive.

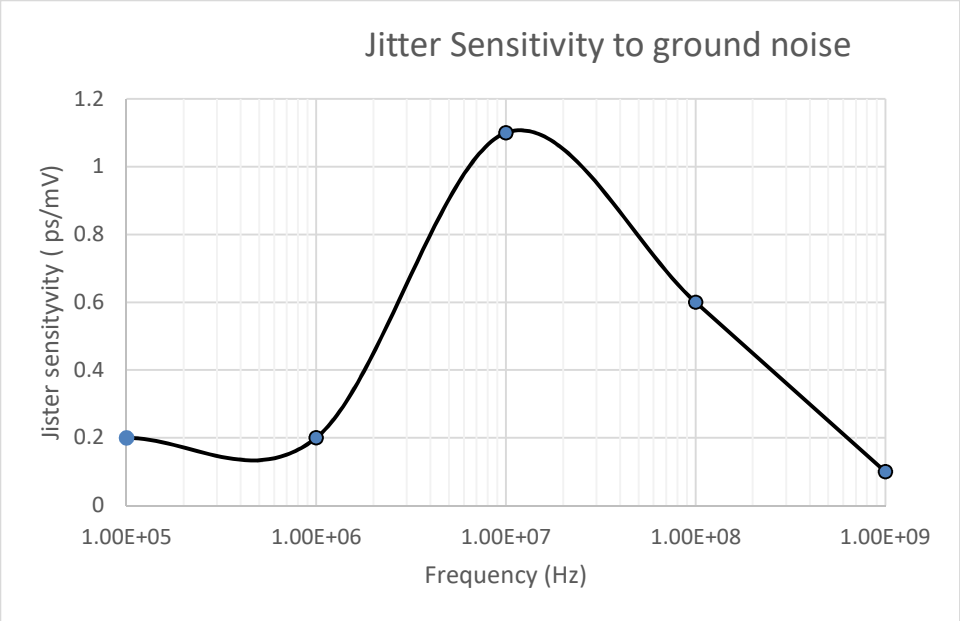


Figure 5: Jitter sensitivity to ground noise for a sample analog block

The S-parameter approach to modeling the PDN has shortcomings in not being able to explicitly understand the delta in potential between different isolated grounds on the die locally which translates to jitter impact in the time domain. While there are pros and cons of using S parameters vs. SPICE models our observation is the choice depends on the application and in our applications using SPICE models helped capture the subtle difference between different grounds for circuit blocks on the die. The caveat however is several iterations and lot of trial and error experimentation was needed to validate the settings in EDA tools to ensure that the SPICE models generated are valid. Another key variable which impacts the coupling between analog/digital blocks through the die/package/pcb is the Q-factor of the PDN's. PDN's with high Q-factor take longer time for the transient noise to decay in the time domain and could potentially translate to higher cycle to cycle jitter in the time domain. Q-factor is defined as $\sqrt{(L/C)}/R$ for a simplified PDN model shown in figure 6 where L is effective inductance of package and C is total on-die capacitance referred to as Cdie or ODC in the figure from reference [5]. As the value of on-die capacitance increases the oscillations in time-domain die down quicker as the Q-factor reduces whereas for lower values of on-die capacitance the oscillations persist more over several cycles.

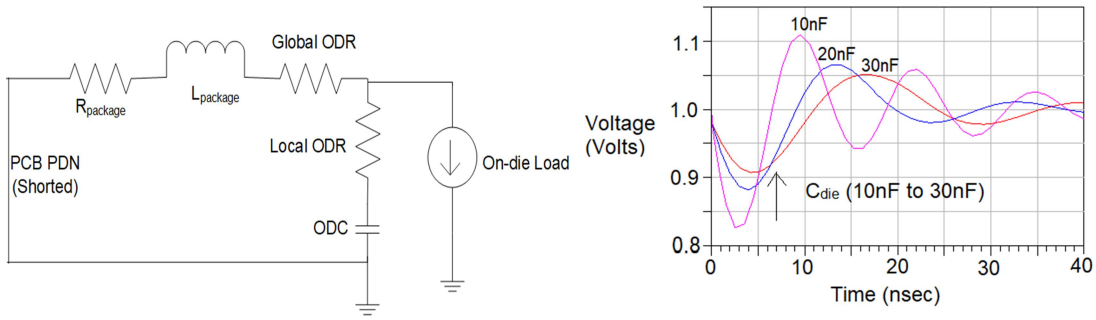


Figure 6: PDN transient response for different values of ODC [5]

In summary there are 5 types of analysis needed to ensure successful modeling of analog/digital coupling

1. Simulate transfer impedance accurately between the analog/digital PDN's with correct port setup and accuracy settings in EDA tools. At this step both S-parameters and SPICE models would work
2. Model the voltage gradient on Power/ground grid on package/PCB in addition to the die for deeper understanding of local hot spots by injecting custom current sources at stitching points of analog/digital grounds rather than using out-of-the box flows. Understand the combined heat map of die/package/pcb (For example if die level hot spots coincide with package/pcb then there could be layout fixes needed on package)
3. Simulate PDN noise sensitivity of critical analog blocks
4. Understand the Q-factor of the PDN's you are working with as it plays an important part in coupling mechanisms. PDN's with higher Q-factor are more sensitive to noise pickup from neighbors.
5. Run SI/PI co-simulation on critical analog signals/power to assess the net impact of PDN coupling on timing jitter. This involves modeling return paths accurately as well which are a source of signal to power coupling [6]. Also at this stage it is important to make a decision on whether to use S-parameter models or SPICE models of the PDN networks. This requires deeper understanding of circuit

The next section discusses a couple of case studies of designs we actually built, tested and simulated in the lab to study analog/digital coupling in more detail.

III. Case Studies based on Test Vehicle designs

1. Description of Test Vehicles

Two test vehicles A (shared ground) and B (split ground) were built in the lab where SOC's were mounted in a flip-chip package and soldered on a motherboard. As shown in figure 1 the main difference between the two designs was that in one case the analog/digital ground was shared on the package while in the other case the analog/digital ground was kept separate on package. Figure 7 shows a simplified diagram of the extracted system as well as stimulus and monitoring mechanism used for analyzing each package. There's a common pcb with VRM supplying power for each domain. The digital and analog power domains are isolated on PCB while sharing a common gnd.

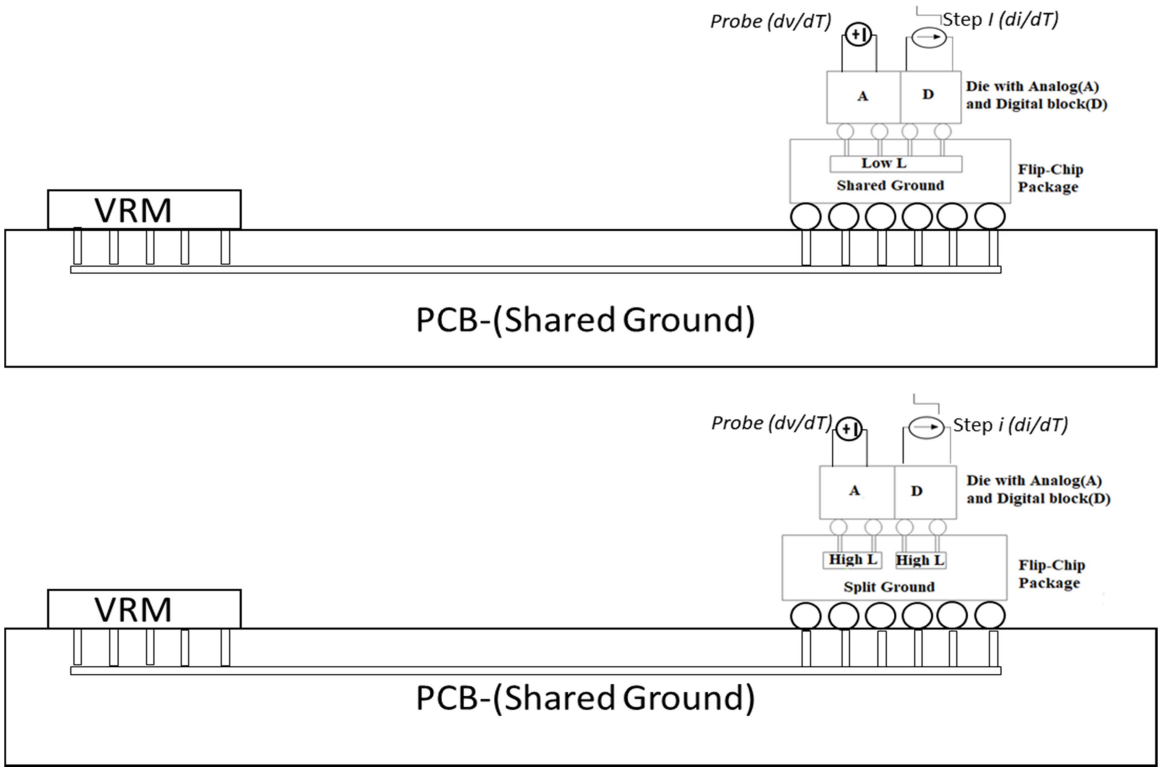


Figure 7: Setup for simulating supply coupling in Shared Ground vs. Split ground in die/package/pcb

Two case studies are discussed below to go over modeling, simulation, measurement tradeoffs for a PLL block and an Oscillator block on these test vehicles.

2. Case 1: Impact of Package ground plane sharing/isolation between analog/digital blocks on PLL block performance

The PLL analog block design was sensitive to difference in local ground potential differences. Hence as explained in section II.2 we used an approach of generating system level SPICE PDN models of the die/package/PCB rather than S-parameter models. Figure 8 shows transfer impedance for test vehicles A and B. Test vehicle A uses a shared ground while test vehicle B uses split ground and hence transfer impedance is higher for test vehicle A where noise transfer happens through the common inductive impedance of the shared ground plane.

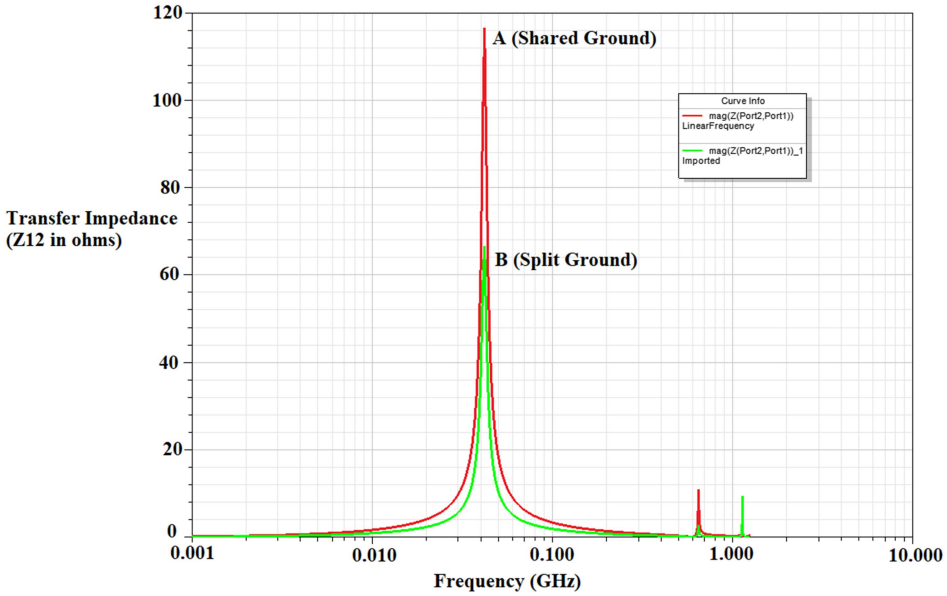


Figure 8: Transfer Impedance for A vs. B

Figure 8 shows a peak in transfer impedance at around 40MHz which corresponds to the resonant frequency of the PDN. A step current stimulus is applied on the digital PDN as aggressor and coupled noise on the analog PDN is observed and plotted in figures 9, 10 for the shared ground and split ground scenario. The package PDN and board level design has some minor differences between test vehicle A and B in terms of analog/digital layout which could impact the effective parasitics to 2nd order, to first order they are similar. As expected when ground is shared for sensitive analog block with digital block more peak to peak noise (~52mV) is seen at the resonant frequency of the PDN whereas in case of the split ground design the coupled PDN transient noise is ~3x lower (around 17mV).

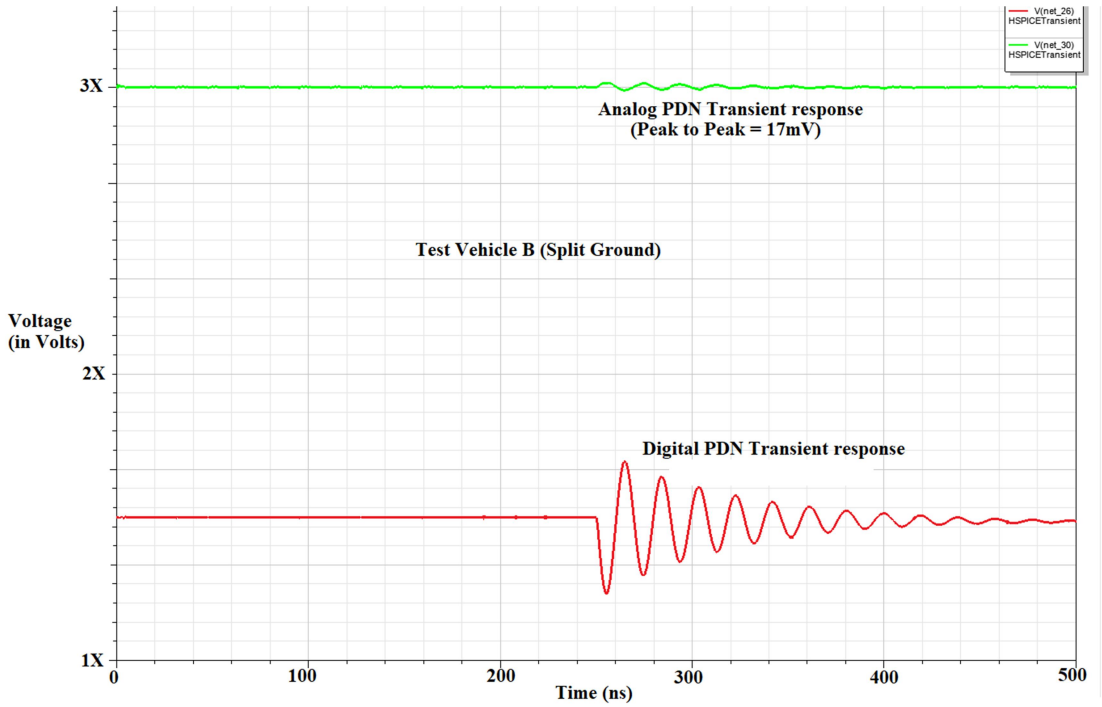


Figure 9: PDN transient noise for Split ground design

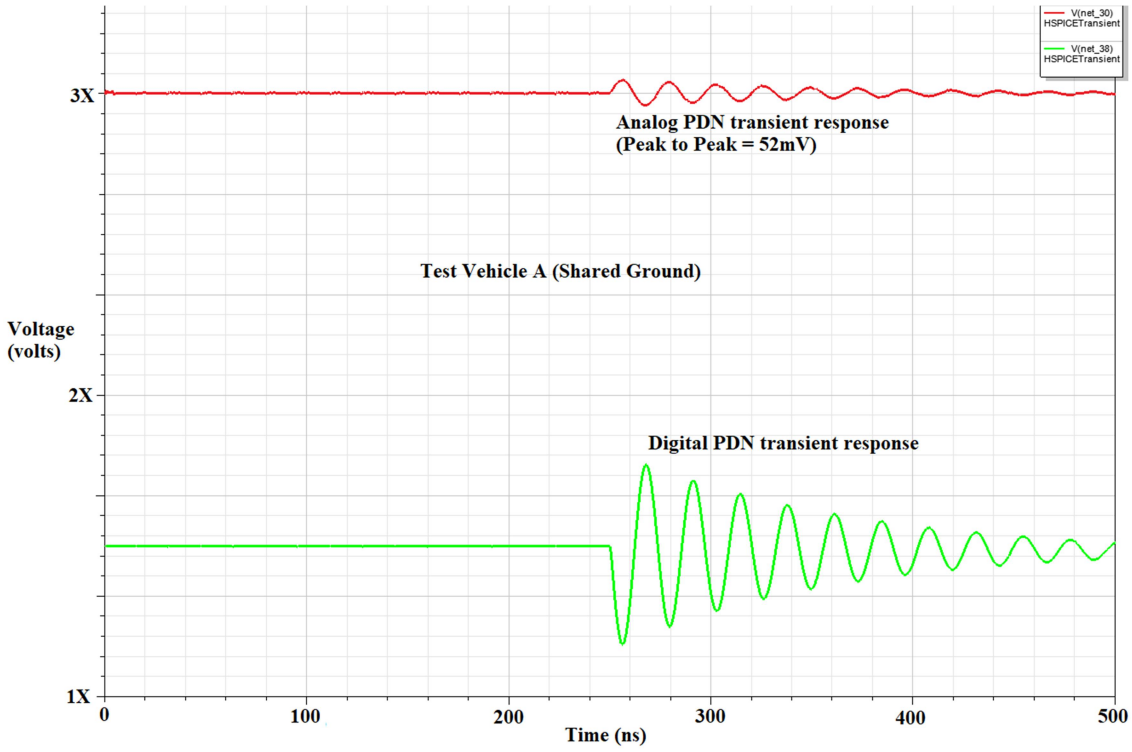


Figure 10: PDN transient noise for Shared ground design

The analog block in this case was a PLL and it was computationally expensive to do full-fledged time domain SI/PI co-simulations for many scenarios to directly look at performance impact on the parameter of interest which in our case was clock disturbance (TIE Jitter) on output clock of the PLL. Instead we relied on qualitative results from PDN simulations to correlate PDN noise with TIE jitter.

3. Case 2: Impact of SI/PI interactions between analog/digital blocks on Analog Oscillator block performance

In this section we focus on an oscillator block on the same test vehicles discussed in the previous section. Proper insight into the interactions of analog and digital domains on die can be gained through spice simulations. The ultimate goal was to model observations in the lab and uses the correlated spice test bench to qualitatively assess digital and analog isolation impact on our designs. The modeling begins with understanding all aspects of the system knowing the critical pieces necessary to capture the appropriate behavior. Specifically the pieces are, the digital domains which are understood to be generating a certain noise signature and negatively impacting the sensitive analog circuits, and the analog domain which is a victim in this regard. To minimize modeling complexity and simplify the spice deck for solving, the detailed modeling of the digital domain is omitted. This is replaced with a disturbance of the digital supply as would be expected in the system. The analog domain, which is the circuit of interest, is modeled with as much detail as possible for the chosen simulation environment. The simulation setup presents itself as a typical signal & power integrity setup to investigate signal quality on die to power supply disturbance.

3.1 Power Integrity: Digital and Analog supply disturbance due to SSO activity

Power integrity of the digital and analog supply was first modeled to understand the noise generated by the digital switching and its effect on the analog supply. For this study s-parameter model of each completed system is extracted. The PCB along with each package design is simulated using s-parameters. A current step is applied on die on the digital domain to simulate SSO activity. Voltage induced on the analog supply due to coupling of the analog and digital domains is probed for comparison among the sample package designs. Table 3 shows the data collected among the two packages observed in simulation. Package sample B with isolated digital and analog gnds produces the lowest coupling of the digital noise onto the analog supply while the shared gnds package (sample A) shows the most noise on the analog domain. This simulation setup is further improved when details of the analog circuitry is added to determine the impact of the noise coupling.

Design Sample	Noise on Digital Supply (mV)	Induced Noise on Analog Supply (mV)
A	181.5	10.5
B	181.0	0.5

Table 3: Comparison of Analog supply noise due to digital switching/noise

3.2 Signal Integrity: Analog output jitter due to supply disturbance

The results of the non-ideal power were merged with a signal integrity simulation to capture the effects of the noise on the output of the analog circuitry. This is accomplished by inserting the analog circuit in a signal and power integrity simulation environment. This feeds a non-ideal power, due to the disturbance of the analog supply, to power the circuit under simulation. The co-simulation of signal integrity and power integrity was accomplished using extracted broadband spice (BBS) model that isolates the analog ground connection on die. This is important as it enables the analog circuitry to connect to the appropriate power and grounding structures. Likewise the digital block grounding was also isolated using the BBS model. Figure 7 shows the connection setup on the die employed in the SI/PI co-simulation. The transient noise event for the simulation is applied after steady state is reached for the analog circuit. Cycle-cycle jitter at the output of the analog circuit is used as criteria to gauge the impact of the supply disturbance on the analog circuits. Figure 11 shows the measured cycle-to-cycle jitter for each of the sample package designs.

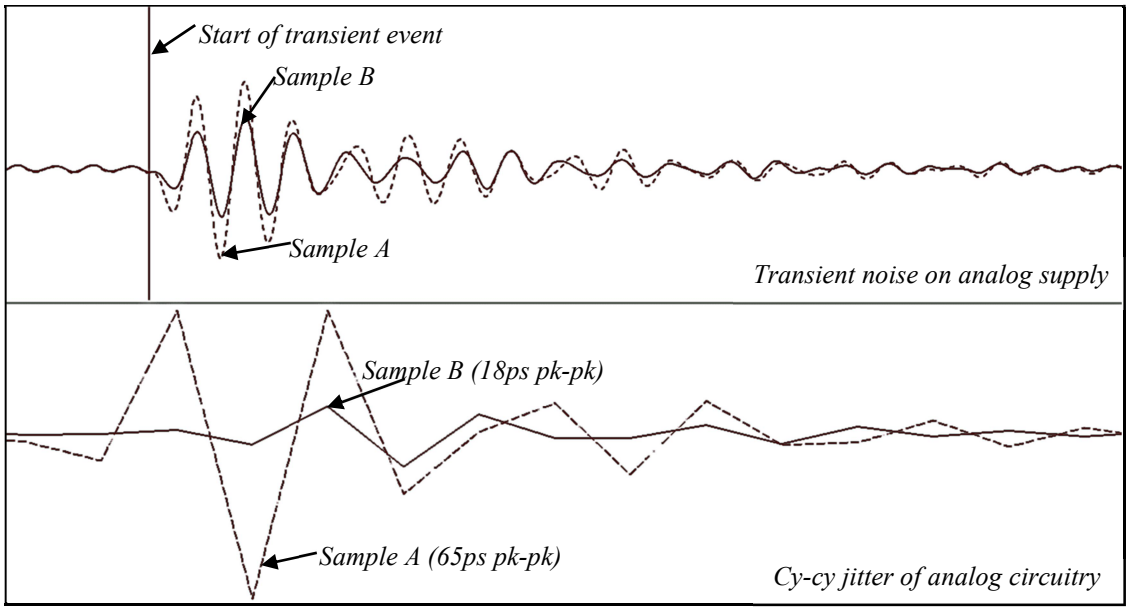


Figure 11: Comparison of cy-cy jitter due to digital switching/noise

The impact of the noise on the analog circuit output jitter is readily observed shortly after the transient disturbance. It causes a temporary shift in the cycle to cycle jitter of the analog circuit that is restored after the noise on the analog supply settles. Package sample A with a common shared ground shows a higher transient disturbance of the analog supply. This translates into an increase in the cycle-to-cycle jitter observed at the output of the analog circuits. Package sample B with its isolated grounding structures on package show a smaller analog supply disturbance as well as cycle-to-cycle jitter. In the next section we discuss observations based on comparing measurements and simulations

for both the PLL and the Oscillator block after first briefly describing the measurement setup /techniques.

IV. Simulations vs. Measurement

1. *Clock Jitter measurements for PLL and Oscillator blocks*

Unlike simulation environment, measurement repeatability can be difficult in the lab environment. The test stimulus, test boards and measurement equipment needs to be the stable for meaningful measurements. Simple rule of changing one variable at a time is very applicable to lab measurements. If one is characterizing the package, only package should change and similar applies to die and PCB.

1. In our case, the measurement parameter is peak to peak jitter whose magnitude depends on peak current/voltage fluctuations. If the peak current depends on signal to noise ratio (SNR), then the jitter measurements will not be stable, so the test routine/parameters will need to be modified to decouple the SNR from the peak current.

2. The test outputs should be differential and connected to digital sampling scope with a high bandwidth differential probe. Single ended probes degrade the measurements due to ground loops, impedance mismatch and probe positioning.

Figure 12 shows a block diagram of the test setup used for measuring TIE jitter on the clock outputs for both the PLL and oscillator blocks.

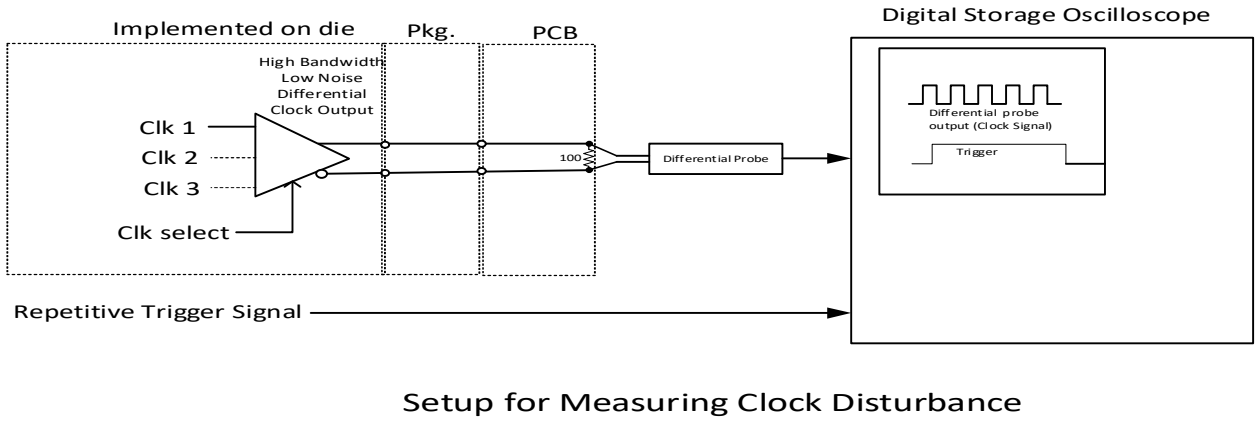


Figure 12: Block Diagram of test setup for measuring clock Jitter

Table 4 shows comparison/correlation between simulated PDN transient noise coupled from digital to analog domain (and) PLL Clock jitter. Qualitatively we observe that an increase in transient coupled PDN noise by ~3x contributes to a 2.77x increase in PLL jitter which is expected for the block under test which was more sensitive to PDN noise. It is expected that more focus on matching the bench current profile stimulus for digital domain would improve the correlation between simulation/measurement further. Also it is expected that improving the noise sensitivity of the PLL around the PDN resonance frequency range would make it respond less linearly to PDN noise even in the case of a shared ground design.

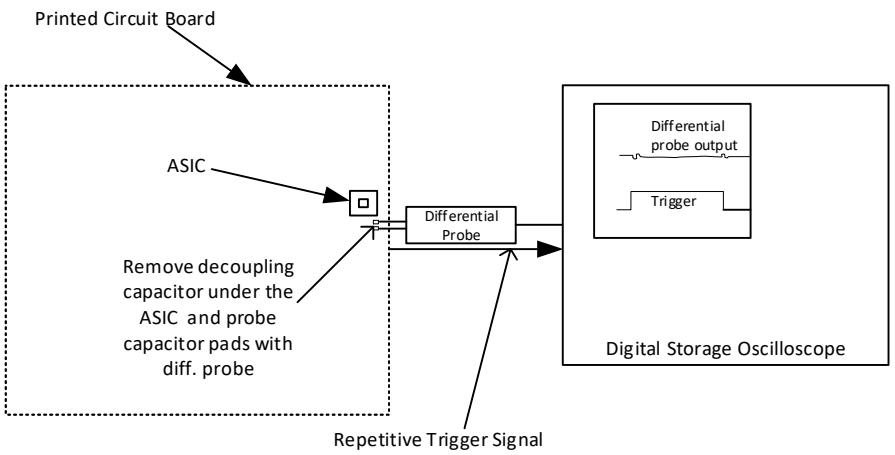
Test Vehicle	Simulated PDN coupled transient noise (mV)	Measured PLL clock Jitter (ps)
A	52 mV	"2.77X" ps
B	17 mV	"1X" ps

Table 4: Qualitative comparison between simulation/measurement for PLL

The oscillator block also showed a similar trend where there was strong correlation between the PDN noise and the cycle to cycle jitter. Drawing a precise conclusion was tough because there were some other variables in the test vehicle design as well beyond the scope of this paper.

2. PDN noise measurements on Package/PCB

In addition to measuring clock disturbance we also looked at digital PDN noise on the Package/PCB test points for the shared ground vs. split ground design to understand the noise aggressor better for framing our simulations. While it was hard to draw quantitative conclusions from this exercise it was useful in validating characteristics of the digital PDN such as resonant frequency, impedance peak, current magnitudes for the stimulus etc. and improved our overall modeling accuracy. Figure 13 briefly describes a sample setup for measuring PDN noise on the PCB and figure 14 includes a sample scope shot of digital PDN response from lab measurements.



Setup for PDN Probing on PCB

Figure 13: Test setup for PDN probing on PDB

To measure PDN noise on PCB, a decoupling capacitor associated with the power domain should be removed and differential probe soldered to vacated PCB pads. The removed capacitor however can be added on top of another nearby capacitor to maintain the total capacitance on the board. Probing package/substrate can reveal resonances related to substrate/die combination. The setup to measure PDN noise on package is similar to PCB except its difficulty in finding the probing points and nearby ground. Initial package observation may not look very interesting however after some low pass filtering and averaging the PDN picture starts to emerge. For example, in the pictures below, yellow trace shows PDN noise capture with 16GHz diff probe connected to a Digital Sampling Scope. After 200MHZ low pass filtering and averaging the following can be observed:

a. Envelop of the IR drops on PCB and VRM response
b. Transients related to on die activity
c. Substrate/Die resonance observed during load changes

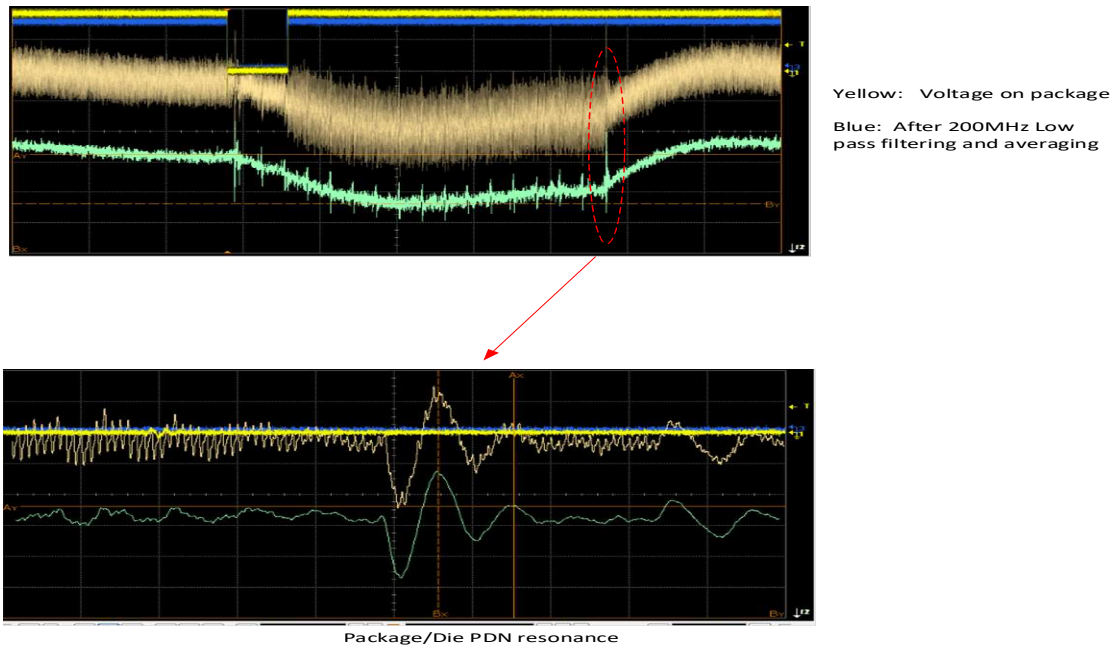


Figure 14: Sample Digital PDN measurement scope shots

V. Conclusion

Every SI/PI engineer goes through debates on whether to share or not share the ground on die/package/pcb for different sensitive analog blocks and there is no reliable EDA tool based systematic step by step modeling approach to aid in decision making and in general decisions are ad-hoc based on prior silicon data or approximated models which are not very accurate. This work shares specifics on modeling approaches which work for different types of analog/digital coupling scenarios. We share case studies on simulating analog/digital coupling with qualitative correlation between simulation/measurements on metrics such as cycle to cycle jitter, PDN noise to guide the practicing engineer in debugging similar problems successfully and to make the correct tradeoffs for their design without being too optimistic or overly pessimistic.

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