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A System-Level Power Integrity Study of Multi-Domain Power Supply Noise Coupling

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Abstract

This work presents a system-level study of power supply noise coupling between different power distribution networks (PDN). Our subject system is built around a large programmable SoC device. Such devices are used in a variety of cutting-edge applications: AI, Cloud, IoT, etc. An SoC chip hosts many different blocks with different power demands, restrictions, and requirements. Different blocks need to operate side by side and interact with each other. Insuring power integrity of such a system becomes challenging. It is particularly difficult to manage noise coupling via shared return path. Such coupling mechanism is sometimes referred to as 'ground bounce'. Our study includes pre-silicon modeling, hardware verification, and correlation steps.

Author Biographies

Dmitry Klokotov is a Staff Signal and Power Integrity Engineer at Xilinx Inc. He specializes in modeling and validation of system level power delivery networks, and characterization of crosstalk and power supply noise induced jitter in high-speed I/O interfaces. He received his MS and PhD degrees in Electrical and Computer Engineering from the University of Illinois at Urbana-Champaign, and BS degree in Physics from Saratov State University, Saratov, Russia.

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Ana Wong is a Senior Engineering Manager at Xilinx Inc. responsible for interposer design/modeling, jitter methodology/validation and PI characterization. Prior to that, she managed a team in Xilinx Inc. that delivered PLL IP blocks for various advanced process nodes including 20nm and 16nm FinFET. She received her MSEE design from Stanford University.

Dawn Graves is a team lead for electromigration and IR drop analysis within the Xilinx Integration Group, supporting analysis from subblock to fullchip level. She has had several other roles at Xilinx, verification and characterization of new parts, Verilog simulation, investigation of customer issues, and test board design. Prior to joining Xilinx, she did FPGA design for military vehicles, was a member of the ESTL lab at

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Johnson Space Center testing Space Shuttle communication systems and payloads, and designed and supported custom test equipment. She has a BSEE from Washington University in St. Louis.

Srinidhi Narasimhan is a Senior Design Engineer at Xilinx Inc. He specializes in modeling, validation and characterization of simultaneous switching noise and power supply noise at system level. He is also responsible for electron migration and IR drop analysis at full chip level. He received the B.S. degree in electronics and communication engineering from Visveshwaraiah Technological University, Karnataka, India and the M.S. degree in electrical engineering from San Diego State University, San Diego, CA.

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Introduction

Our study was driven by necessity. Previously Xilinx's sole focus was producing Programmable Logic Devices (aka FPGA). Lately however there is an increasing demand for System-on-Chip (SoC) or rather Multiprocessor System-on-Chip (MPSoC) type of products. In such products Xilinx tries to combine the best of both worlds: the flexibility of Programmable Logic and the performance of hard ASIC-style blocks. Insuring power integrity of such complex heterogeneous devices is a major challenge.

Different blocks can share the same power supply. Finding the worst-case scenario in terms of power supply stress and making sure the system is robust enough to survive that event is far from straightforward. On top of that, interaction between blocks powered by separate supplies can no longer be ignored.

One particularly stressful scenario is a complete power-down of a major power supply. In older heterogeneous systems a power-down event in a major supply also meant a complete system shutdown. We did not have to worry about the system's performance after such an event. That is no longer true. In a complex MPSoC system a large block can be turned off while the circuitry in the other blocks (powered by a separate supply) must continue functioning.

Different blocks are usually designed separately by specialized teams and must be carefully integrated together. Therefore, it was important for us to perform a system-level study which identified potential aggressors and victims. Then we had to make sure that even in the event beyond normal function of the aggressor circuitry (such as a shutdown) the voltage noise coupled to the victim supply did not exceed safe limits.

To model voltage noise coupling between different power domains we had to develop an appropriate methodology. The study had to account for coupling at all levels of the system: die, package, and PCB. In some cases, when sensitive supplies had very good isolation in silicon, we could use simplified lumped models for on-die Power Distribution Network (PDN). However, in other cases we had to adopt ANSYS Chip Power Model (CPM) to capture die-level noise coupling between large distributed supplies that could not be completely isolated and had a lot of shared ground.

System-Level PDN Modeling Methodology

There are three main parts in our system-level power supply model [1], [2], [3]: board, package, and die. We leave the modeling of a voltage regulator outside of the scope of this paper. Each part of the model contributes to different components of the power supply noise and requires somewhat different treatment. However, the overall approach is based on representing every component with a behavioral (s-parameter) model or an equivalent circuit (where appropriate); and on combining the elements into a system-level model that can be used either for small-signal or transient analysis. Figure 1 shows a general setup of a system-level PDN model.

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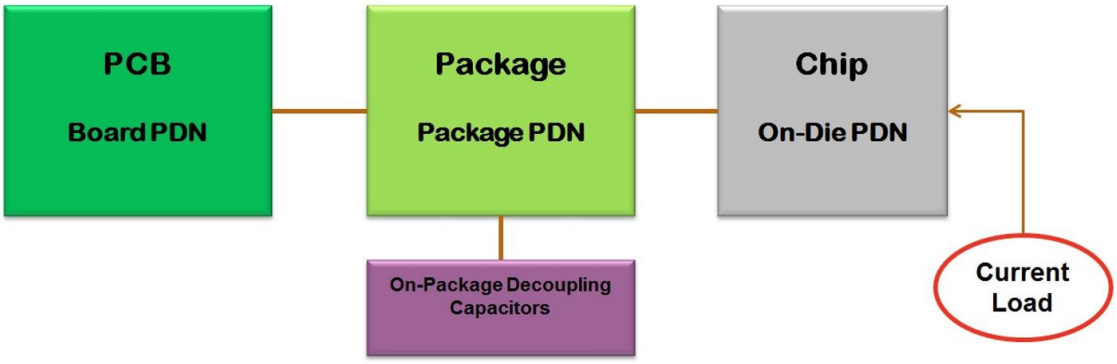

Figure 1. General setup of a system-level PDN model

It is (or it was) common to use s-parameters for PCB and package-level power supply models while representing the die PDN with a lumped RC circuit. Recently that methodology is considered overly simplistic and in general is frowned upon. Nevertheless, we will later demonstrate that the lumped approach is still good enough even for study of voltage noise coupling. It works for smaller power supplies in cases when the die-level coupling is negligible.

In cases when we have reasons to suspect that on-die PDN can make a significant contribution to the overall level of coupled supply noise, lumped RC models are no longer useful. An appropriate model must be distributed and must be able to capture the noise coupling due the shared return path. There is obviously more than one way to develop such a model. We ended up using ANSYS CPM flow for our distributed die-level PDN models.

In this study we focus on time-domain characterization of power supply noise. The transient analysis, requires an appropriate transient current load to induce voltage noise in a PDN system. In many cases it is difficult (if not impossible) to obtain a detailed current profile for a system-level event. Trying to define a reasonable realistic worst-case scenario even for a single block of a programmable MPSoC is a serious challenge. Once the number of aggressor blocks is larger than one, the task becomes daunting. In the subsections below we discuss some details of the current load configuration, but in many cases, we settled for simple models based on a step function.

A. A Case of a Sensitive but Well Isolated Power Supply

Our first case study considers a very noise-sensitive analog system. A common practice is to try to completely isolate the power supply for such a system from any potential aggressors.
The system's supply has four different segments. For simplicity we will call the victim supply "supply A". In silicon the power traces of the supply A are kept at a large enough

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distance from all other power distribution networks to prevent any power-to-power coupling. On top of that, the ground associated with the supply A is separated (trench isolation) to prevent sharing of the return path with other supplies. With all those measures in place it is safe to assume that there is not going to be any voltage noise coupling between the supply A and any aggressors on the die level. Also, A is small enough for us to not be concerned with any distributed effects. In such situation we can use a lumped RC model to represent the on-die portion of the A PDN.

Owners of the sensitive analog block are naturally worried about any potential coupling from large noisy supplies of other blocks. The designers can make sure there is no coupling in the die, however package and PCB is a different story. It is possible to reduce or effectively eliminate power-to-power coupling in package and board by careful layout planning and maintaining required separation between power planes. The ground on the other hand tends to be common to insure low inductance of the return path.

The most dangerous aggressor for supply A is supply B, the largest power domain in the system. Supply B powers multiple blocks. We include two blocks into our model based on the size and proximity to the victim supply. Supply B is large and distributed, but since we use lumped RC model for the victim supply, it makes sense to do the same for the aggressors. The model setup is shown in Figure 2.

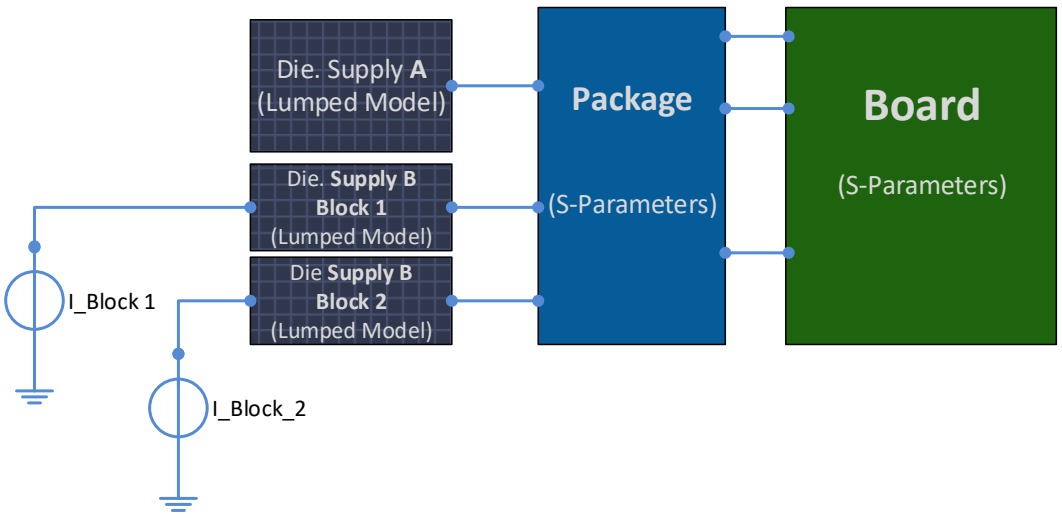

Figure 2. System-level PDN model for supplies A and B. Assuming perfect on-die isolation between the two.

Blocks 1 and 2 are very different. Block 1 is a “hard” ASIC-like block, so it is relatively easy to obtain a reasonable realistic worst case current pattern for the I_Block 1 model in Figure 2. In fact, we use two scenarios in our study: a more reasonable realistic one and a synthetic synchronized case that induces more transient noise. Block 2 is a flexible programmable block. Designing a current profile for such blocks is always challenging. In our study we use a simplified two-stage step-like profile. The shapes of the current profiles used in our simulation are shown in Figure 3.

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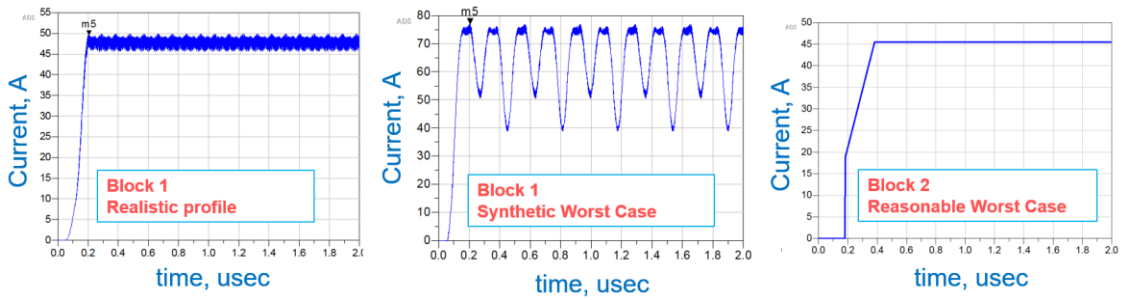

Figure 3. Current profiles for two aggressor blocks in supply B

Current profiles of the two blocks are aligned in time to achieve the largest voltage noise event in supply B.

Package and board-level power distribution is modeled with layout-based s-parameter blocks (Figure 2).

A proposal was made to take additional steps to reduce the coupling through the shared return path. To further isolate supply A from the aggressors in supply B the ground planes in the package can be slotted along the border of supply A as shown in Figure 4 with read lines. Slotting the ground through the entire package will lead to increased inductance of the return path for A. Instead the isolation can be created in the package layers above the core.

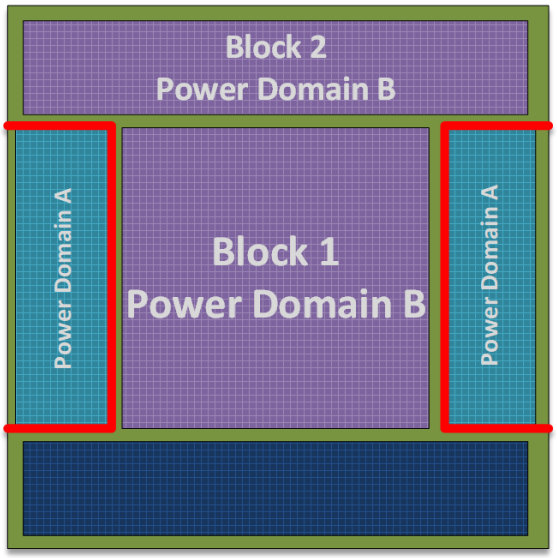

Figure 4. Simplified representation of a package with slotted ground planes

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Then the grounds are tied together below the core. In our study we evaluate the impact of the slotted ground on the amount of coupling between A and B.

The results of our simulations are shown in Figure 5. We have two cases: package with combined ground planes, and the one with slotted ground in the package layers above the core. In both cases we first apply realistic current profile for Block 1, then test with the Synthetic Worst Case.

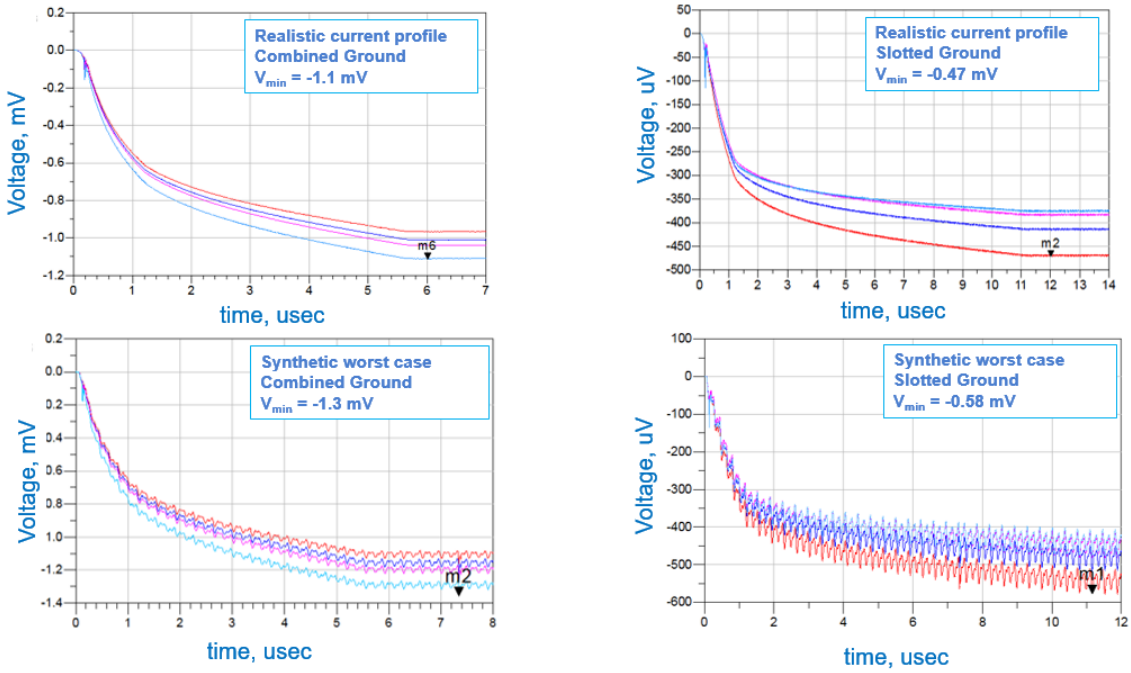

Figure 5. Coupled voltage noise. Simulation results for the case of well isolated supply A

As can be seen from Figure 5 the large transient current that corresponds to the initial ram-up in all current profiles, only creates a small voltage droop on the order of 150 – 120 uV in supply A. The lowest point in all cases happens once the supply settles and corresponds to the static IR drop due to a large current flowing through a common return path. There are minor variations between different segments of supply A. We consider the worst-case numbers. The results are summarized in a table in Figure 6.

	Real App Case		Worst Case	
	Combined GND	Slotted GND	Combined GND	Slotted GND
Noise on Supply A, mV	1.1	0.47	1.4	0.58

Figure 6. Summary of the coupled noise numbers for supply A

The absolute magnitude of the coupled noise is low. However, in relative terms splitting the ground in the package lowers the coupling by more than 50 percent.

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B. A Case of a Large Distributed Power Supply

The problem of isolating small sensitive power supplies from large noisy ones is relatively common. However, the development of large SoC devices brings a different challenge. Now we have several distributed supplies capable of creating large transient currents. Each supply powers multiple blocks in different areas of the die. In such cases it is not possible to arrange a dedicated return path for each supply in any part of the system. We must use a distributed model for the on-die portion of the PDN, a model that captures the coupling between different supplies, particularly the voltage noise coupling through the common ground.

In our study we used ANSYS Chip Power Model (CPM) to model the die-level PDN. ANSYS CPM leverages full-chip time domain and AC analysis technologies to create a compact and highly accurate electrical representation of the chip in various operating modes. It models the entire die power delivery network (PDN) including device level (switching, leakage) and parasitic information to create a SPICE-based model with ports at the die level bumps or pads. It accurately represented the electric response of the chip for a wide range of frequencies from DC to multi-GHz.

Once again, we can treat one power supply as a victim (call it “supply A”) and another one as an aggressor (“supply B”). We use ANSYS RedHawk tool to extract the CPM for supplies A and B from the chip layout. The result of the extraction is a distributed SPICE-compatible netlist. There is no absolute global ground node defined in the extracted equivalent circuit. The model maintains localized power and ground ports for supplies A and B.

We want to stay within the general framework of our modeling methodology described in the earlier subsection. The methodology relies on using S-parameter based models for package and PCB. All component models are assembled in Keysight ADS tool and the system-level transient simulation is performed. To preserve the same flow, we translate our die CPM into S-parameters. In the S-parameter format the die PDN model acquires the global absolute ground reference that is common with the rest of the components of the system-level model. The coupling path through the shared ground is retained but now all voltage noise manifests itself as power noise. The system-level model setup is shown in Figure 7.

We are interested in modeling a specific high-current event in supply B. The architecture of the system allows a complete shutdown of all blocks in the domain B while the circuitry supplied by A must remain functional. We identified a possible (however unlikely) scenario in which power supply B would transition from high activity (high current) state straight into shutdown in a very short time. A shutdown like that will produce a large transient current spike in the supply B. While the performance of the circuitry in B is not a concern, the event in B can introduce voltage noise into supply A and potentially. We must verify that the coupled noise that appears in supply A does not exceed established safe limits.

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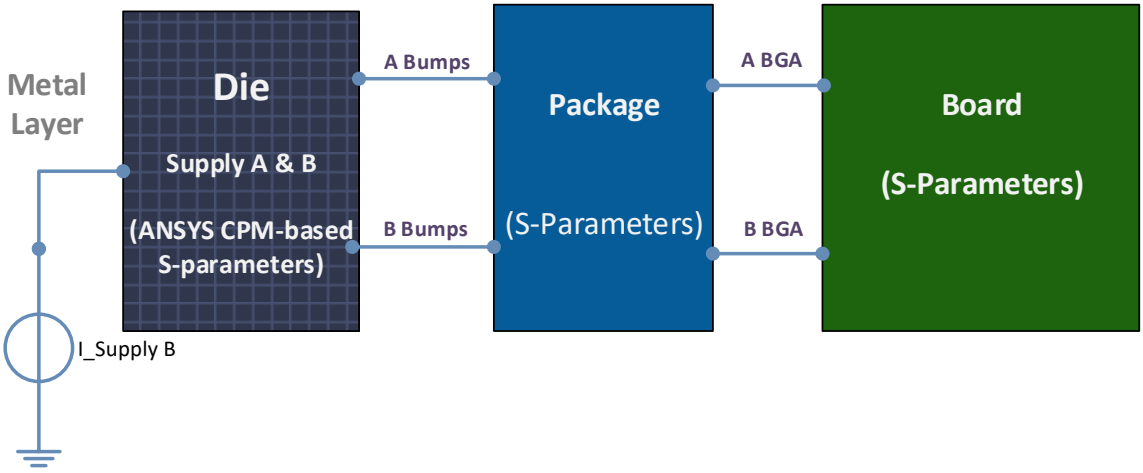

Figure 7. System-level model setup for the case of two large distributed supplies A and B

Supply B powers a lot of programmable logic. The exact use case depends on application. It is difficult to predict the detailed current signature of the event under consideration. We simplify our model to represent a current ramp-down from 110 A to zero in 10 ns as shown in Figure 8.

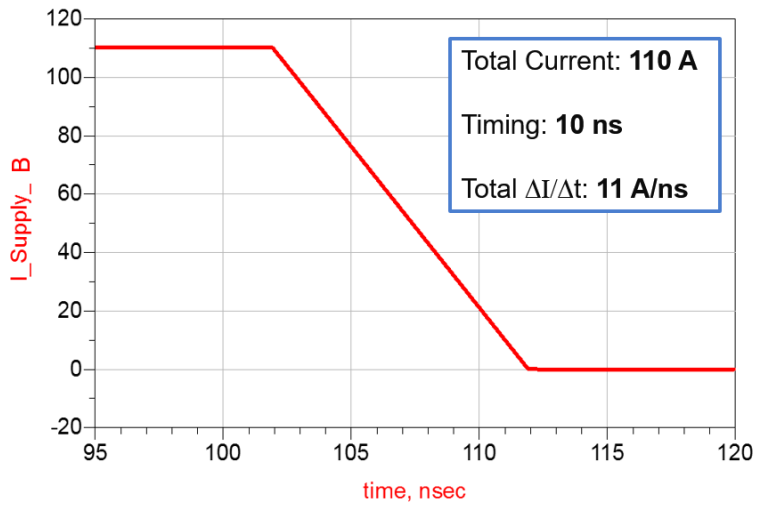

Figure 8. Current profile for the shutdown event in supply B

Results of the system-level simulation are shown in Figure 9. The coupled noise is measured at the die bump level. Since there is no VRM in the model, the PCB IR drop is included in the measurement. In the actual system regulator compensates for the board drop at the package BGA level.

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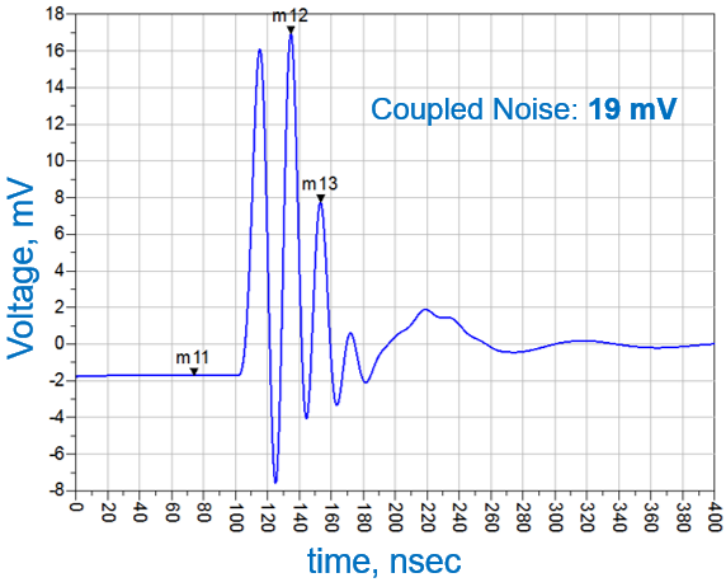

Figure 9. Coupled voltage noise in power supply A

We would like to understand the contribution to the overall noise from each component of the system. We created additional models in which supplies A and B are decoupled either at the PCB level or both in package and PCB. The results of that study are shown in Figure 10.

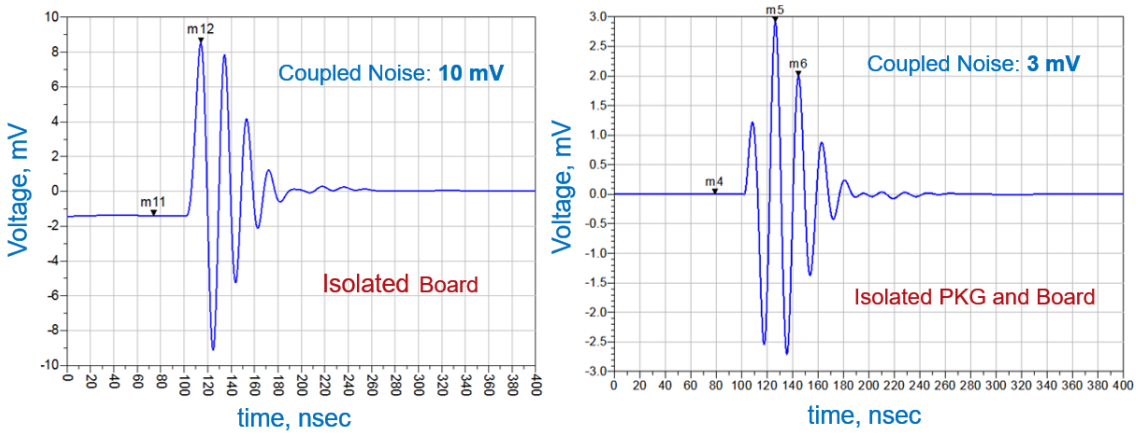

Figure 10. Coupling noise contribution from different components of the system

From the results in Figure 9 and 10 we can derive the contribution of each component of the system to the overall value of the coupled noise and put together a summary shown in Figure 11. Obviously, we are assuming (for simplicity) that the superposition principle holds for our system. From the summary in Figure 10 we can see that PCB and package are the main sources of coupling and contribute approximately equal amounts of noise. Coupling in the die is not insignificant, but the die is only responsible for 16 percent of the overall noise.

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	Die	Package	Board	Total
Coupled Noise in Supply A, mV	3	7	9	19

Figure 11. Summary of noise contributions from different components of the system

Power Supply Coupled Voltage Noise Measurements

Once we received back the actual parts we performed laboratory measurements of the coupled noise. We used dedicated probing points at the top of the package [1] and a real-time oscilloscope to capture the noise waveforms.

A. A Case of a Sensitive but Well Isolated Power Supply

In general, setting up to capture just over 1 mV of power supply noise (predicted in the simulation) is a rather ambitious task. In the simulation we assumed a large delay between the two aggressors firing up. By doing that we tried to push the coupled noise waveform to the lowest point.

In the actual system trying to time the aggressors from two very different blocks proved to be impractical (if not impossible). Instead we ended up simplifying the event in the aggressor supply to a single-shot large transient current ramp similar to the one used in the simulation for a distributed victim supply case. The total current was tuned to be approximately equal to the sum of the two separate current profiles from Figure 3. The direction of the current was the opposite of one in Figure 8. Instead of stopping circuitry in power domain B and looking for the overshoot, we started large-scale activity in B and looked at the response in A. The results are shown in Figures 12 and 13.

In all of our measurements we used high-bandwidth DC blocking capacitors at the inputs of oscilloscope channels (AC coupling). That was required to get the necessary resolution (in single mV range) on the noise waveform. With the DC blocked, the reference level becomes zero and the measurement only contains the AC noise.

The results in Figure 12 are obscured by the VRM noise. Unfortunately, the VRM we have on our test board has +/-3 mV swing without any load. If we take away the VRM noise and the high-frequency spikes, we get just over 2 mV of low-frequency board-level noise. Which is consistent with the simulation.

We tried to get rid of the VRM spikes by using an external supply. In Figure 13 the noise waveform is clean. Unfortunately, the connector for an external supply is located at the edge of the test board. Additional parasitics associated with an external power source increase the noise magnitude to 3 mV.

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The timing of the waveforms in both figures suggests that most of the noise is likely coming from the low-frequency coupling through the shared ground in the PCB.

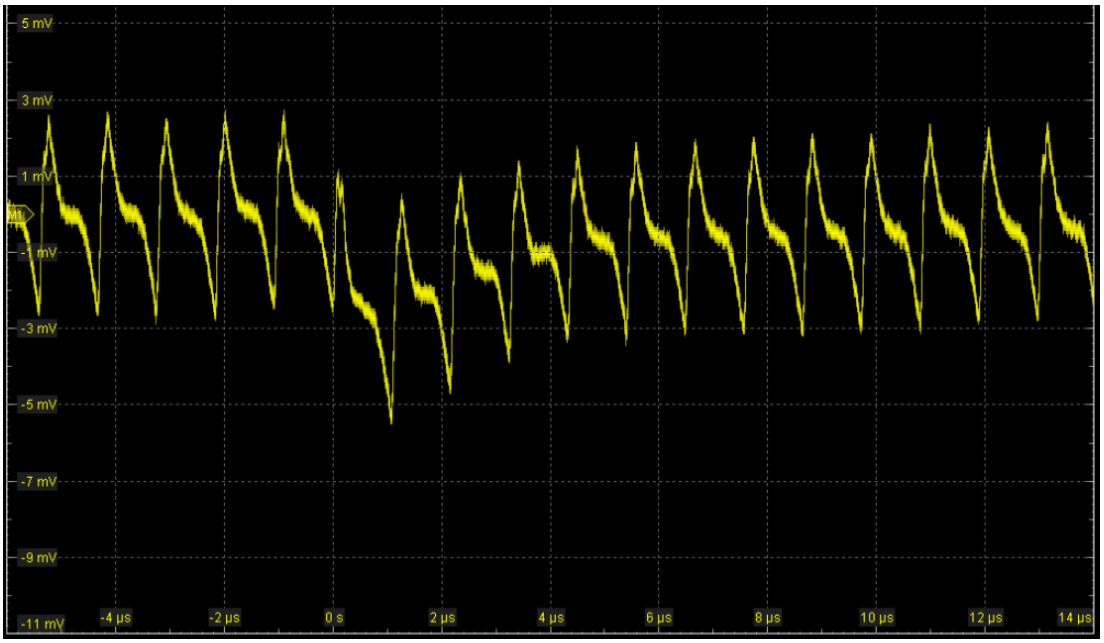

Figure 12. Measured noise in the victim supply A. Using on-board power supply.

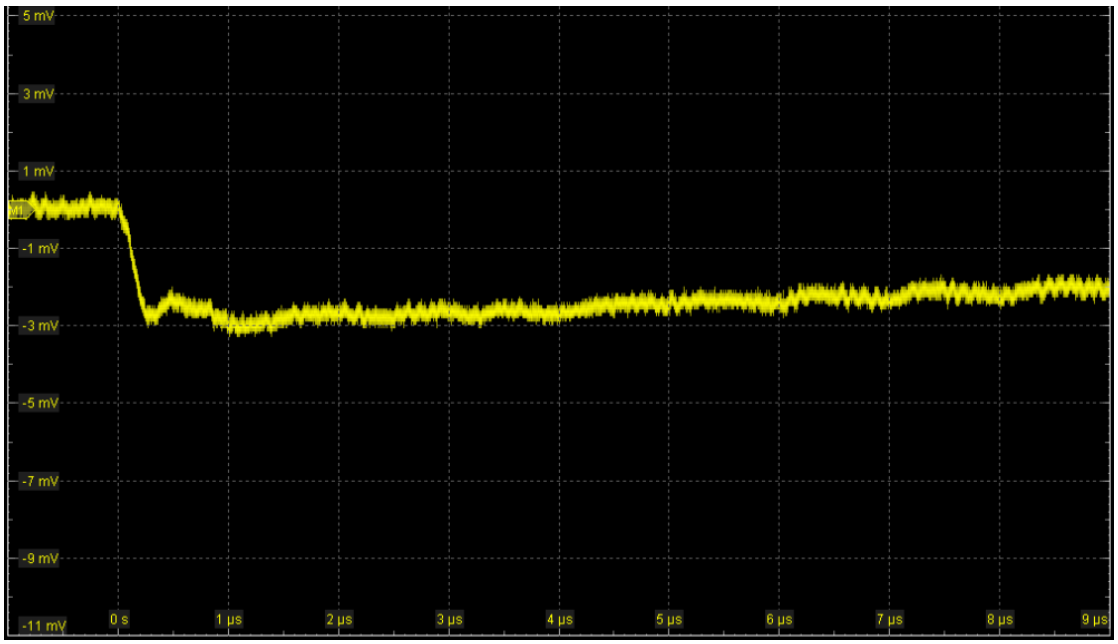

Figure 13. Measured noise in the victim supply A. Using an external lab supply.

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Additional measurements are required to explore the case of two different blocks acting as aggressors. In this work we did not try to study the effect of several transient current events happening in the system at various timing intervals.

B. A Case of a Large Distributed Power Supply

Similar to the case of a small isolated supply our measurement was again somewhat limited buy the VRM noise. We could not observe the long-term settling of the supply with on-board regulator while adding an external supply created excessive parasitics. However, we were able to capture the high-frequency portion of the coupling noise waveform. The results are in shown Figure 14.

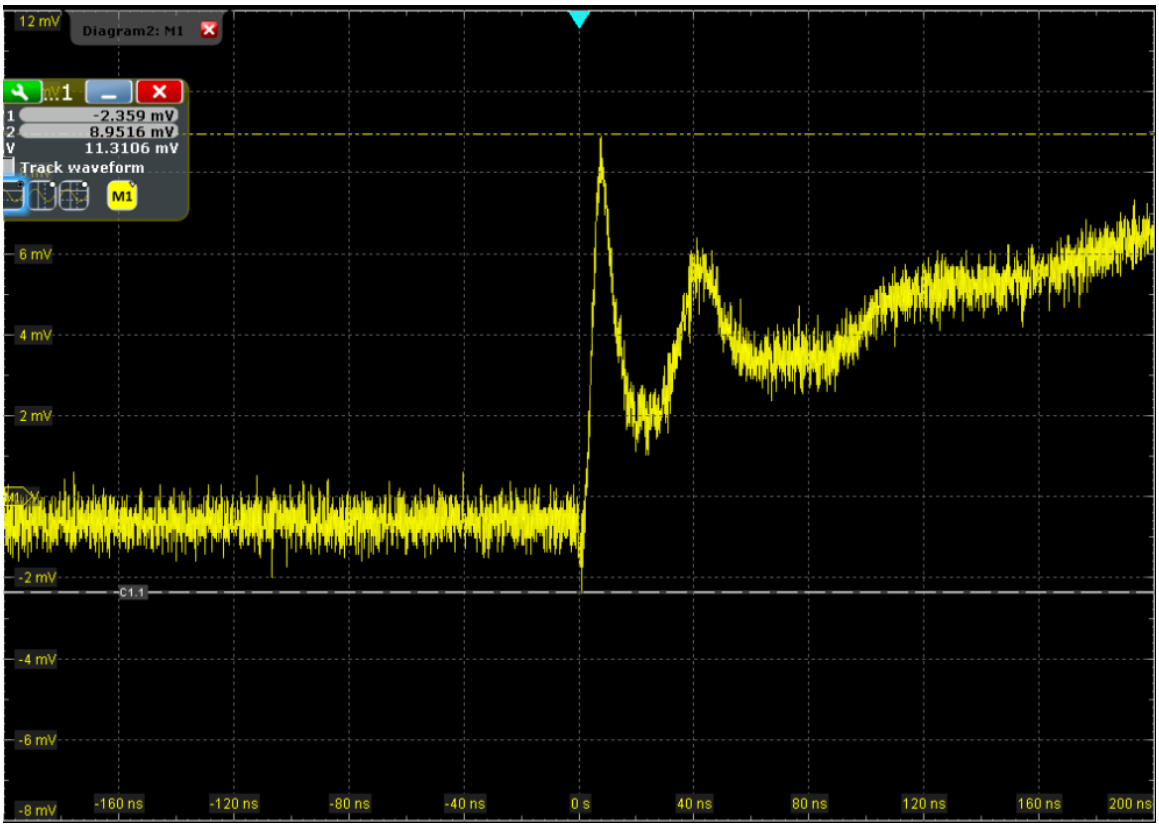

Figure 14. Coupled noise waveform in the large distributed victim supply A

The magnitude of the overshoot in Figure 14 is approximately 11 mV. Compared to the simulated results the measured noise is smaller and does not have a lot of high-frequency ringing. The measured waveform looks more dampened compared to the simulated one. It is likely that our model underestimated the on-die capacitance and the resistance of the system. A more careful extraction of the CPM with better knowledge of the silicon process parameters should help to achieve a better correlation.

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Summary and Conclusions

We performed a system-level analysis of power supply noise coupling between different power domains in a system built around a large programmable Xilinx MPSoC chip.

A case of a small sensitive but well isolated supply was considered first. A traditional approach to system-level PDN analysis was employed for the well-isolated supply case.

In the second case we studied a large distributed supply. The large supply provided power to multiple blocks in different locations on the chip. Because of the distributed nature of the supply it could be more susceptible to voltage noise coupling. A different methodology was used to capture the distributed nature of the large supply. It was shown how ANSYS CPM can be applied to build a distributed die-level PDN model that captures the voltage noise coupling via a shared return pass.

We performed lab measurements of the coupled noise for both simulated cases. The correlation proved to be rather challenging due to setup limitations. However, in general, measured results did agree with the simulation. The overall conclusion was that while the coupling between different supplies was not negligible, the noise that we observed in our system stayed well within the acceptable limits.

References

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