DesignCon 2019

EDA Tool-based Methodology for accurate extraction of On-die Capacitance and Resistance

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Abstract

On-die capacitance (ODC) is important in the design of robust power distribution network (PDN) by providing a means to minimizing the high-frequency PDN impedance. ODC is critical to mitigate high-frequency noise when other types of decoupling capacitance cannot provide the necessary charge. It is challenging, however, to predict ODC and on-die resistance (ODR) accurately at full-chip level where various types of ODC including intrinsic gate capacitance and signal interconnect capacitance are a significant contributor. This work provides insights to power integrity engineers in determining ODC and On-die resistance (ODR) more accurately at different stages of the design with minor adaptations to existing CAD flows, leveraging industry standard tools.

Author(s) Biography

Karthik Chandrasekar currently works at Intel Programmable Solutions Group as a Signal/power integrity engineer in a silicon hardware team. He has 16 years of combined industry and research experience as a hardware system engineer with expertise in Package design, IO padring design, Signal/Power integrity, Full chip power analysis, 2.5/3D IC integration and CAD flows for analog circuit simulation/multi-die integration.

Guang Chen is a design engineer with Silicon Systems Development Department at the Programmable Solutions Group (PSG), Intel Corporation, where he is responsible for driving signal/power integrity co-design effort for the key FPGA products with focus on both silicon and system level power integrity solutions. Prior to this, he was with Technical Service Dept. at Altera Corporation, providing system SI/PI solutions for customer Altera FPGA applications. He holds a Ph.D. in Electrical Engineering from University of Arizona. His professional interests include power integrity and signal integrity, high-speed interconnects and channel modeling.

Wendem T. Beyene received his B.S. and M.S. degrees in Electrical Engineering from Columbia University, and his Ph.D. degree in Electrical and Computer Engineering from University of Illinois at Urbana-Champaign. In the past, he was employed by IBM, Hewlett-Packard, Agilent Technologies and Rambus. He is currently with Intel Corporation working on modeling and analysis of power delivery and signaling systems of core and I/O subsystems for FPGA chips.

Shaan Awasthi is a senior manager of Design Automation & Methodology in Intel's Programable Solutions Group, his expertise is in chip package co-design and system level analysis and verification. At Intel he is responsible for driving the methodologies and CAD/EDA flows for circuit simulation, reliability and Power and Signal Integrity. His research interests include Machine learning and big data technologies to augment the EDA flows in solving the challenging problems in the IC design world. Prior to this he had various strategic roles at Ansys and Sun Microsystems.

Anil Gundurao works on System Reliability flows in the Design Automation group at Intel PSG in San Jose. Anil has over 25 years' experience in full chip reliability signoff and in development of power integrity flows and methodology. He holds a master's degree in computer science.

Ying Fei was an engineer in the package design group at Intel while this work was done

I. Introduction

On-die capacitance (ODC) is important in the design of robust power distribution network (PDN) by providing a means to minimizing the high-frequency PDN impedance. Figure 1 shows a simple die/package lumped PDN model with the PCB PDN ignored. Here we break the On-die resistance (ODR) into two components: global ODR and local ODR. Global ODR is defined as the effective on-die resistance from the transistor all the way to the bumps while local ODR is in some sense the effective ESR of the decoupling capacitors due to local on-die resistance from the transistor diffusion regions up to local ports defined on lower level metal layers such as metal2 on the die. The assumption is that the circuits don't have time to find charge at a point farther way than this when we are dealing with fast rise times less than 50 picoseconds.

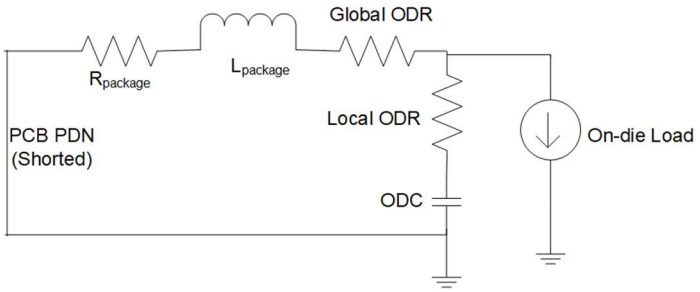

Figure 1: Representative System PDN Lumped model

PDN impedance in the frequency domain and PDN transient response are plotted in figure 2 for different values of ODC with fixed representative values for other parameters in the lumped model. A triangular current step waveform with peak amplitude of 1A is the input for PDN transient simulations. Similar plots are shown in figure 3 for 3 different values of local ODR with other parameters fixed. It is noted from figures 2 and 3 that the properties of the PDN in the time domain and frequency domain change significantly as a function of ODC, ODR and the metrics can be captured as below from [1]:

1. Voltage dip (time domain) defined by Q=CV and RC time constant
2. Resonant frequency = $1/2\pi\sqrt{LC}$
3. Impedance Peak = (L/C)/R
4. Q-Factor = $\sqrt{(L/C)}/R$ (defines if the system is under-damped/over damped or critically damped and impacts settling time/ringing of transient response)

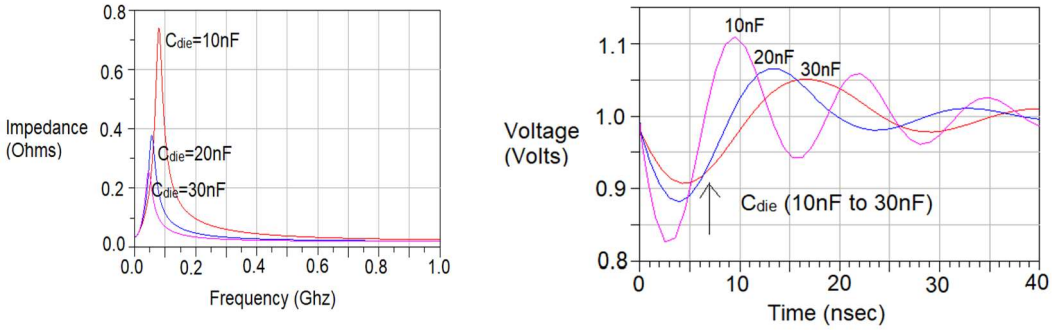

Figure2: PDN frequency response and transient response (for different ODC values)

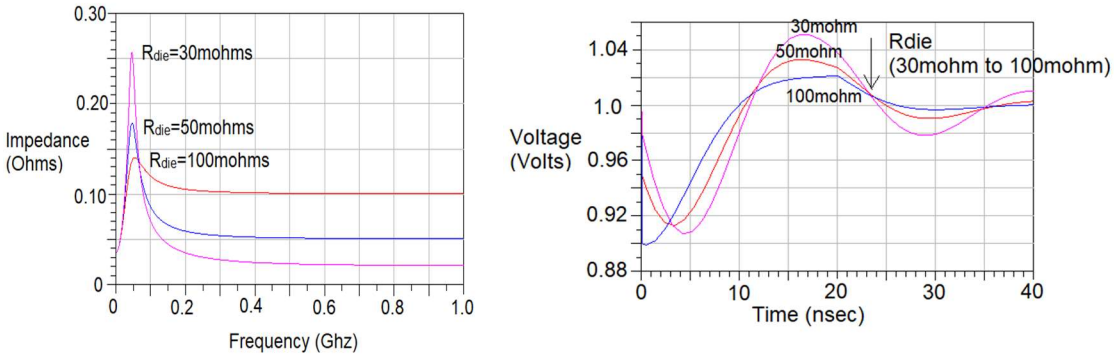

Figure 3: PDN frequency response and transient response (for different local ODR values)

The curves in figure 2 and figure 3 are from the perspective of an on-die load looking outward. As the ODC values increase from 10nF to 30nF the resonant frequency moves downward, impedance peak in frequency domain moves downward while the voltage dip noise in the time domain reduces as well. As ODR values increase from 30mohms to 100mohms the impedance peak in the frequency domain moves downward due to increased damping while the signature of time domain noise changes as a function of Q-factor of the RLC circuit. Low values of local ODR are desirable from DC IR drop perspective, however it is not necessarily beneficial from perspective of dampening mid-frequency AC PDN resonance noise. While frequency-domain (VNA) and time-domain based measurements have been used to predict ODC with reasonable accuracy, it is still particularly challenging to predict the total available full-chip ODC accurately with software techniques before silicon hardware is available for FPGA designs. Various papers have discussed some of these challenges briefly in previous publications [1,2]. The key takeaway is that significant portion of total ODC at full-chip level can come from intrinsic device capacitance due to redundant non-switching gates in FPGA's. While various prior work addresses ODC estimation and measurement correlation, they don't provide insights into how to estimate ODC accurately at different stages of the design based on available

collaterals (pre-layout, post-layout etc.). For example, circuit toggling factor, signal loading, types of logic (core vs. IO), and layout techniques impact the ODC values extracted from CAD tools significantly and the practicing power integrity engineers need to be cognizant of these nuances to design the PDN accurately without over-design. This work provides insights to the practicing power integrity engineers in determining ODC for different applications more accurately at different stages of the design with minor adaptations to existing CAD flows, leveraging industry standard tools. Tradeoffs of different approaches are discussed to avoid common pitfalls and to ultimately design a robust PDN which evolves progressively as a chip design progresses from early planning phase to final tapeout. The paper is organized as follows: section II discusses various EDA flows for PDN analysis to give the reader a quick primer on the various stages involved, section III provides comparison of SPICE based approaches for ODC extraction with Industry standard tools, section IV discusses Silicon correlation of ODC with EDA tools, section V provides recommendations to PDN designer on EDA approaches for ODC estimation at different stages of the design, section VI discusses ODR extraction challenges and section VII is the conclusion.

II. EDA Flows for PDN Analysis

1. Sources of ODC

An excellent discussion of sources of ODC is found in [1]: Diffusion capacitance from reverse biased p-n junctions, power/ground mesh metal capacitance and intrinsic gate capacitance from non-switching gates. However, it does not specifically mention signal interconnect capacitance as a contributor which was noticed to be important from this work. Essentially the interconnect capacitance can create a path from power node of a MOS device to ground to act as decoupling capacitors and in FPGA custom architectures where there is a lot of redundant routing between blocks this cannot be ignored particularly for the core fabric. Figure 4 shows the different sources of ODC including signal interconnect capacitance. Intrinsic gate capacitance can also arise from MOSFET gate to drain capacitance and gate to bulk capacitance, but only gate to source capacitance is shown in the picture as it is a major contributor.

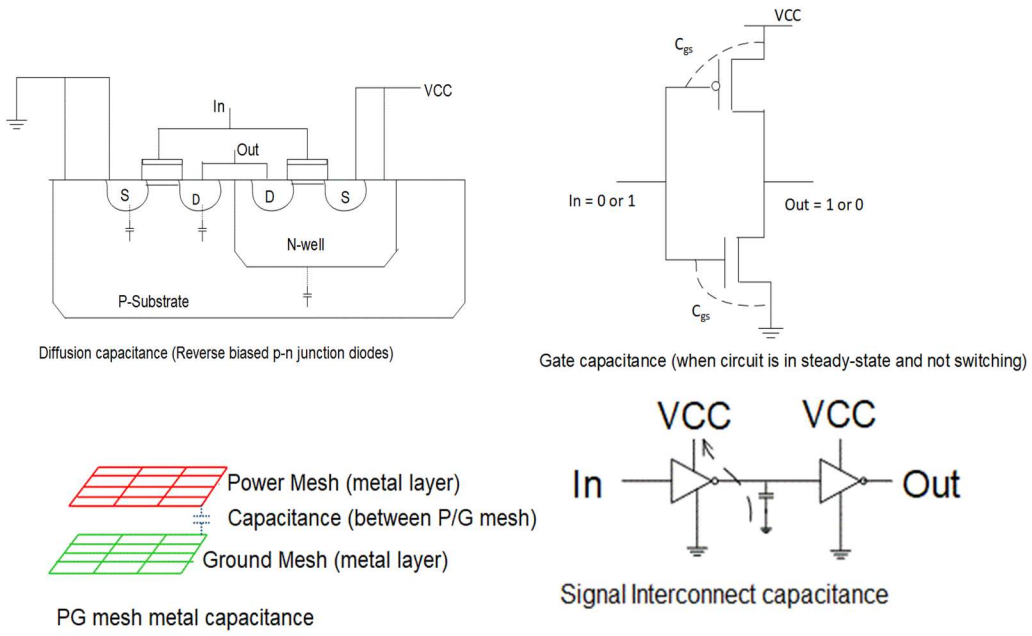

Figure 4: Sources of ODC in FPGA Applications

Gate capacitance includes both intrinsic and intentional MOS decoupling capacitance while power/ground (PG) mesh capacitance also includes metal-insulator-metal (MIM) capacitances which could be added on higher metal layers in the layout with special intermediate metal/dielectric layers. Signal interconnect capacitance comes from wire loading and varies based on routing density and block type.

2. EDA Flow stages for PDN analysis

EDA flows for PDN analysis from a system designer's viewpoint can be broken down at high level into 3 successive stages with some iterations between them: (i) IP block level ODC/ODR extraction (ii) full-chip dynamic IR + chip power model generation (including current profile info) (iii) chip/package/PCB +multi-die PDN co-simulation. This paper focuses more on the first stage of IP block level ODC/ODR extraction to improve accuracy as this is the foundation on which the successive stages rely heavily on. Figure 5 shows a drawing to illustrate the 3 stages. Some of Intel's products include heterogeneous integration using technologies such as EMIB [3] and hence the system PDN flow shows this component as well with tiles referring to any die integrated with FPGA. Embedded interconnect bridge (EMIB) enables high density integration of silicon tiles built in different process nodes by embedding silicon wafers with high density interconnects in package.

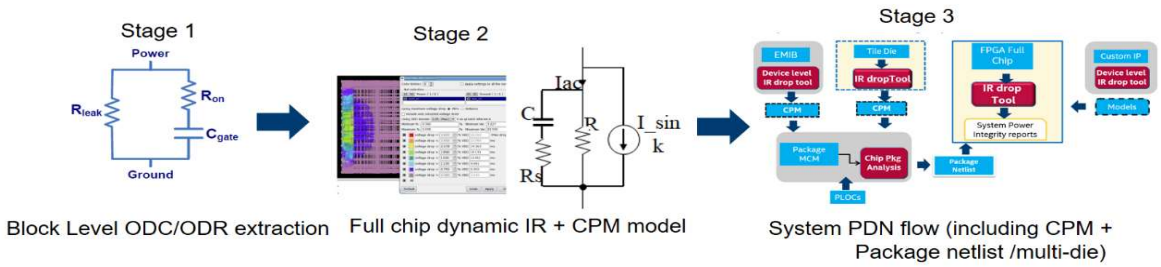

Figure 5: EDA flow stages for PDN Analysis

Figures 6 and 7 show typical plots a system PDN designer generates with these flows for a representative FPGA Core PDN including die and package. For example, as shown in figure 6, in stage 1 typically block level ODC vs. frequency is extracted while at stage 2 when full-chip database is available PG mesh metal capacitance is extracted among other things. PG mesh capacitance tends to be small and is not so important to consider at initial stages and is adequate to model at a full chip level once. On the other hand, intrinsic capacitance is easier to extract at a block level and then roll-up to full-chip level iteratively. Figure 7 shows sample system level PDN plots in both frequency domain and time domain as seen from a point on the die. The frequency response shows the classic mid-frequency PDN resonance from die/package interaction while the time domain response at different probe points on the die reveals the distributed nature of the die. Current profiles are typically read in from block level SPICE test benches into full-chip runs for all the circuit blocks and is not shown here. In cases where detailed vectors are not available EDA tool provided options are used to generate stimulus based on type of design. Once all block level characterization is complete, full-chip runs are used to generate a chip power model which then gets combined with package layout files to plot frequency domain and time domain response of the PDN.

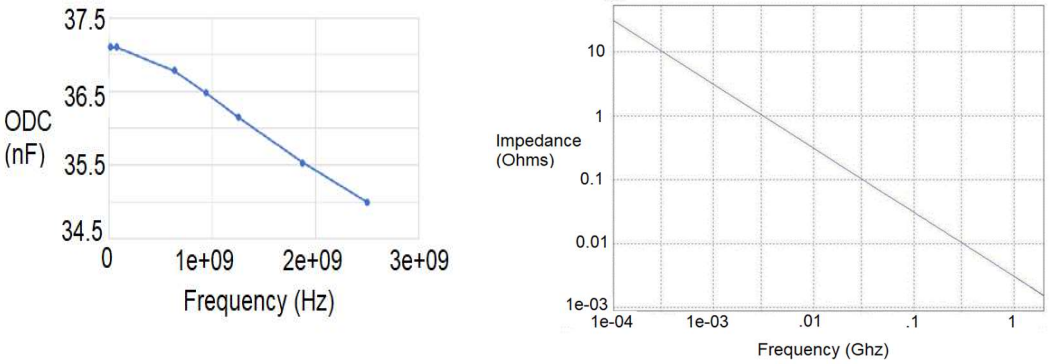

Figure 6: Typical plots generated in stage 1,2 of PDN flows

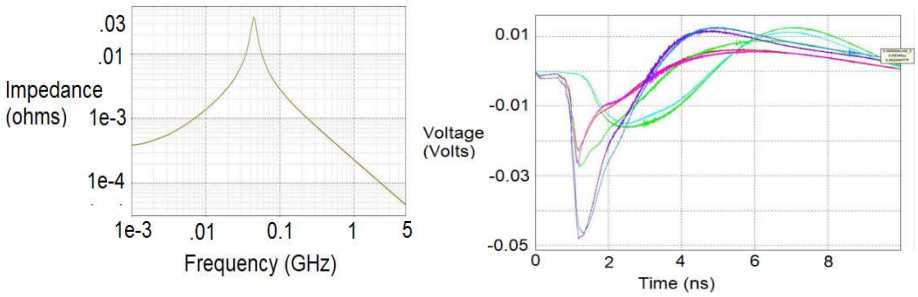

Figure 7: Typical plots generated in stage 3 of PDN flows

Different EDA tools are available to the end-user and the choice of tool depends on what type of PDN analysis is being done (low frequency or high frequency). It is important for PDN designer to keep in mind that PDN noise has both low frequency components and high frequency components and it is required to use different tools to sign-off based on strengths/weaknesses. For example, typically die level analysis tools are more efficient for high frequency PDN noise analysis while system level analysis tools are more efficient for low frequency PDN noise analysis [4,5,6]. In addition, planning phases of a design typically needs niche power planning tools [4,5,6]. Figure 8 shows a plot to explain PDN low frequency vs. high frequency noise. PDN high frequency noise can only be addressed adequately by adding more local decoupling capacitance close to IP block being analyzed on the die while PDN low frequency noise can be addressed through combination of budgeting techniques and exploring decoupling solutions across the entire PDN eco-system [7]. It must be pointed out here that some literature regards the first dip noise as high frequency and only the PCB/package/die related resonant frequencies are considered as low frequency. However, we deviate a little from this and categorize first dip noise as also low frequency in the drawing and only refer to multi-GHz high frequency switching noise as high frequency PDN noise.

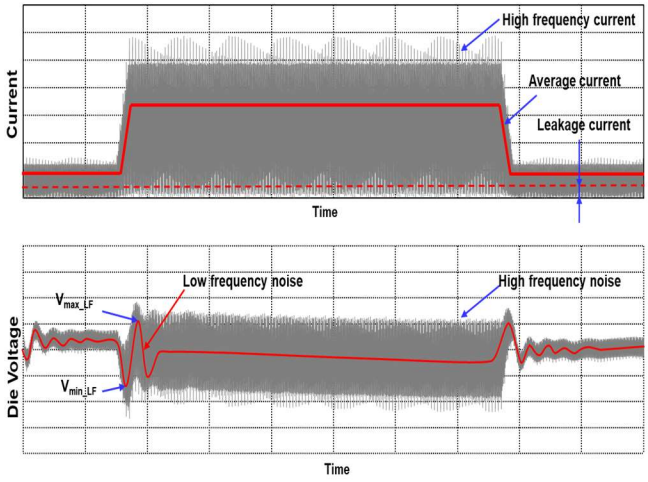

Figure 8: PDN Noise (Low frequency and High frequency)

III. Comparison of SPICE based approaches for ODC extraction with Industry standard EDA tools

SPICE based AC analysis can be used on basic building circuit blocks in a FPGA design to extract ODC/ODR from first principle equations on charge, current and ohm's law:

$$Idt = CdV;\ C=I/(\Delta f)\ (\Delta V);\ V=IZ$$

Circuit operating condition needs to be set at fixed steady state condition based on realistic use-case in SPICE, values are derived based on model fit across many frequency points. It should be noted that value of ODC/ODR extracted is a strong function of circuit operating state. Figure 10 shows SPICE results from a basic FPGA logic element block which was represented by a first order RC network in parallel with a leakage resistance as shown in Figure 9. Here the block's impedance response was fitted to a lumped model shown and values extracted. At low frequencies the Z11 of the PDN looking into the power node is determined by the leakage resistance (R_{leak}) primarily as the gate capacitance is an open circuit, after the lower corner frequency gate capacitance takes over and at higher frequencies the curve flattens out to the value of R_{on}. The effective decoupling capacitance of the block is determined by applying a .ac analysis in the sloped region of the impedance curve and by looking at real and imaginary parts of impedance. In reality, a logic circuit has several possible paths between power and ground and it is hard to model accurately with a simple lumped circuit beyond a certain frequency range. Also, statistical analysis is needed for understanding probability of different states in the computation as discussed in [2]. In this work the intent behind SPICE based analysis to extract ODC and correlating with EDA tools is to help understand in depth the underlying algorithmic assumptions under the hood used by various CAD tools and use the insights gained to drive methodology changes. Obviously, silicon correlation of ODC from measurements with EDA tools is the end-goal and that is briefly touched upon in later sections.

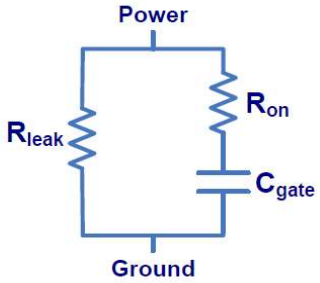

Figure 9: First order RC model for a logic circuit at certain operating state

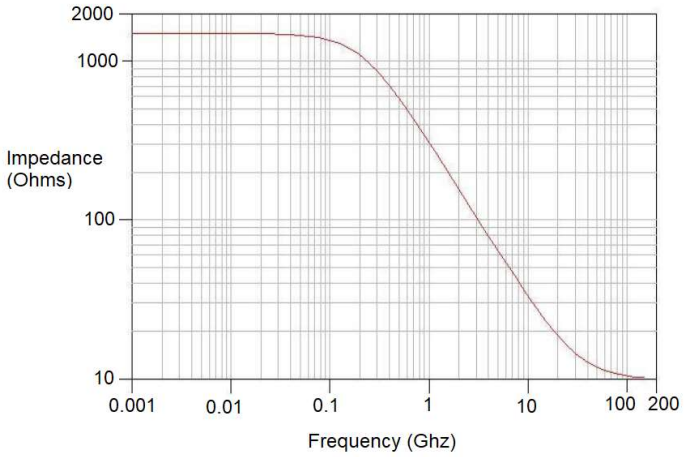

Figure 10: Z11 for a FPGA LE block when R_{leak}=1500ohms, R_{on}=10ohms and C_{gate}=0.5pF

The plots in figure 10 were just aimed at giving an example of general approach for SPICE based ODC estimation. A FPGA core building block was picked for studying in more detail thereafter. Table 1 summarizes the comparison of ODC extracted for this block using SPICE based approaches vs. EDA tool-based approaches.

ODC	EDA Tool	SPICE
PG Mesh metal cap	~3pF	~3pF
Intentional Gate decap	~18pF	~18pF
Intrinsic Gate decap	4.9pF	14pF
Total ODC	~25.9pF	~35pF

Table 1: ODC Comparison - SPICE vs. EDA tool

From table 1 we see that PG mesh metal capacitance and intentional MOS decoupling capacitance correlate accurately as expected since SPICE analysis included power grid mesh from post-layout. But we notice that intrinsic gate capacitance is significantly off by 2.8x with EDA tool reporting a smaller value. Initially, the suspicion was that this was

because of SPICE using ac analysis to estimate ODC which implies 0% toggling. To validate this, experiments were performed to vary toggle factor in EDA tool with custom approaches and data is reported in table 2. The precise numerical value of toggling factor can change depending on the customer application and trends are shown qualitatively in table 2 by using a variable X for the toggling factor percentage. EDA tools tend to use one fixed pessimistic toggling factor to estimate ODC. This is because as toggling factor increases the percentage of quiet logic reduces and consequently the effective intrinsic gate capacitance available for decoupling reduces. This forces designers to take more caution in PDN design which is good in many situations, however it can also lead to overdesign when you are working with challenging product spec goals with minimal available resources. So, it is important to sweep toggling factor for different applications. For example, FPGA's are used in wireline, wireless, datacenter, military etc. and deep dive on different end-applications is necessary and a prerequisite to arrive at realistic assumptions.

ODC	Toggle Factor
6.4pF	0 %
5.6pF	X/2 %
4.9pF	X %

Table 2: ODC vs Toggle Factor

While Table 2 only shows ODC variation across toggling factor for the block of interest chosen for correlation here a larger subset was studied which included both core and IO logic circuits. The general trend and observation was that change in toggling factor could lead to about 28% variation in ODC extracted from EDA tools. This is important to consider in the design process to avoid PDN overdesign or under-design. Comparing the EDA tool extracted ODC value at 0% toggling of 6.4pF to 14pF from ac analysis now indicates a discrepancy of 2.18x which is some improvement from before, but still significantly off. On closer examination of SPICE setup, the test bench also included wire loading from signal connections and while industry standard parasitic files (SPF) were provided to the EDA flow it was noted that in some types of custom block analysis the SPF was not used as contribution of signal loading to PDN decoupling capacitance was thought to be insignificant. While this may be true in some designs a deep dive into FPGA fabric routing interconnect loading and patterns revealed that this could be a big number leading to significant underestimation in this scenario. Thereafter experiments were done to include

signal interconnect loading in the EDA tool simulation and data was regenerated at 0% toggling factor to match closer to SPICE setup. This data is reported in table 3

ODC	Core Block	IO block
w/o signal cap	6.4pF	887fF
With signal cap	13.46pF	1.53pF

Table 3: ODC with and without signal interconnect capacitance for different block types

The value of 13.46pF for ODC (when signal capacitance is included) for the FPGA core block chosen in our study matches much closer to SPICE value of 14pF (within 4%). The EDA tool does not capture diffusion capacitance while SPICE is capturing the impact of well-capacitance and using diode models to capture area/perimeter contributions of ODC and hence the value is a little higher compared to the EDA tool. Diffusion capacitance arises from reverse biased p-n junctions in MOS transistor layouts as shown in figure 4 and is a function of DC bias and layout approaches. Industry standard post-layout RC extraction tools can be used to generate accurate reports which can be consumed by SPICE to estimate this reasonably accurately. Since this is a small contributor to total decoupling capacitance we did not scrutinize the accuracy of this value further. It was surprising to see signal interconnect loading contributing 2x delta in PDN decoupling capacitance but later it was understood to arise from FPGA core fabric routing architectures. Figure 11 shows typical FPGA routing architecture from previous generation of Stratix products. Routing is organized in rows and columns through horizontal(H) wires and vertical(V) wires. The routing architecture guarantees connectivity between any set of chosen logic cluster arrays referred to as logic array blocks (LAB's) and efficiency is measured by the number of hops it takes to traverse from one logic cluster array to another.

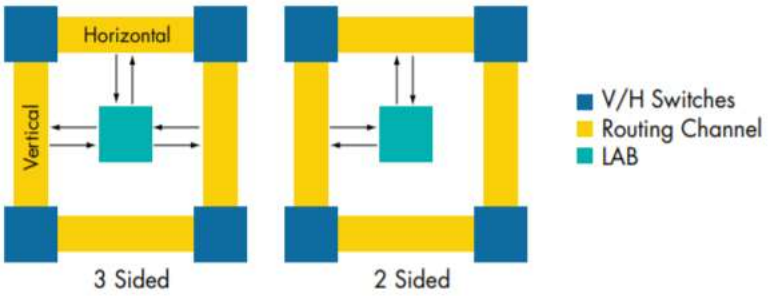

Figure 11: 2-side and 3-sided routing architecture ([8])

For custom IO blocks, we noticed a wider spread in terms of contribution of signal interconnect loading to effective decoupling capacitance. While for "FPGA core blocks" we noticed a consistent trend of 2x variation in ODC estimate coming from signal interconnect loading, for custom blocks we noticed 73% variation for the case discussed in table 3 and variation between 30 to 50% in other cases. The impact of signal interconnect loading in a specific design will depend on the routing architecture and whether the block is FPGA Core or IO block or custom analog or purely digital. In general, custom routing blocks like the ones found in FPGA's will have highest signal interconnect loading followed by custom IO analog blocks while pure digital blocks are expected to have less contribution to ODC from signal interconnect loading. This also explains why we haven't seen this mentioned in other literature on PDN analysis for SOC die. The big benefit of this is also that FPGA core architectures could potentially have higher PDN decoupling capacitance intrinsically compared to ASIC CORE's of similar dimensions.

IV. Silicon Correlation for ODC – Measurement vs. EDA

1. Silicon correlation for standalone ASIC IP block

Initially, the preference was to target silicon correlation for the entire FPGA Core as it has a lot of custom blocks and here impact of toggling, signal interconnect loading will be seen clearly. However, we encountered several roadblocks due to a variety of issues: 1) EDA flows in prior generations black-boxed many custom IP's to speed up run-time for IR analysis and this led to inaccurate ODC/ODR estimates and it was too cumbersome to recreate the needed collaterals at full chip level 2) too many unknowns with stimulus patterns used to mimic customer application scenario and 3) discrepancies in time domain vs. frequency domain approaches and several challenges seen in the past in [1] with capacitance variation with bias voltage for core power domain.

To avoid these issues, a standalone ASIC IP block which was operating on an independent power domain was picked to demonstrate basic accuracy of ODC EDA extraction flows with silicon measurement. ODC was extracted to be 188nF from vector network analyzer (VNA) measurements at fixed bias conditions. ODC was estimated by fitting a lumped model topology assumed in figure 12 to the VNA results.

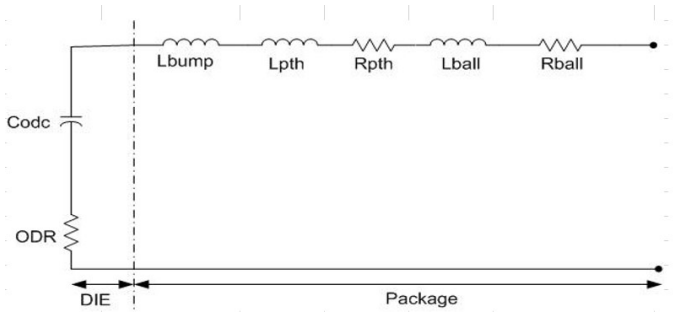

Figure 12: PDN model topology used to extract ODC from measured VNA data

Table 4 shows comparison of measured vs. EDA tool extracted ODC value. EDA tool shows 10% lower ODC from measured value which is expected as VNA measurements are done at 0% toggling which leads to slightly higher value. On the other hand, EDA tool typically uses a fixed pessimistic toggling factor assumption for ODC estimation.

ODC - VNA measurements	ODC - EDA tool
188nF	168nF

Table 4: Measured ODC vs. EDA tool extracted ODC

It should be noted that effective ODC extracted from EDA tool varies with frequency as well, but we noticed it to be within 1 to 2% in this case and ignored it for the summary here. Also, the chosen block for silicon correlation included MIM cap as well and the EDA tool predicts total decoupling capacitance including MIM contribution. This exercise established basic confidence in the default EDA flow and validated ODC value differences as a function of toggling factor, but we could not yet validate magnitudes and impact of signal interconnect loading. This led to next step discussed below.

2. Silicon correlation attempt for Core Power

Since detailed correlation of "core PDN" was not possible for the reasons mentioned earlier in section 1, a qualitative correlation was attempted with available data points. The purpose of this exploratory work was to prove that a big discrepancy would exist between ODC extracted from EDA tools using default flows (without considering signal interconnect capacitance) and measurement based ODC projections. The available data point was measured ODC from VNA for core power from prior generation FPGA product which was then scaled through back of the envelope area/process scaling manually for current generation. Since there are many unknowns, specific numerical values are not mentioned here. However, it was interesting to note that difference in default EDA tool based ODC

estimate (which did not include signal interconnect capacitance) vs. hand-calculations for Core power was of the order of 2.2X. In the previous section we noted that including signal interconnect capacitance increased the ODC predicted for FPGA custom core routing blocks of the order of ~2x and we believe this is leading to the big delta fundamentally. We must point out that some smaller deltas could also come from high switching assumptions on some custom blocks. Hence it is theorized that including signal interconnect capacitance contribution from custom routing blocks in FPGA fabric which are all over the chip would contribute to close the gap significantly. Also experiments with customer application toggling factor would help close the gap further between 0% toggling assumption of VNA measurement and the pessimistic assumptions of default EDA flows. Table 5 summarizes this discussion.

EDA Tool estimated ODC	Hand-calculation of ODC (projection)
1X	2.2X

Table 5: Qualitative comparison of projected vs. EDA tool simulated ODC

V.EDA approaches for ODC extraction in different stages of product execution

In general product execution is broken into 3 phases for chip design: Architecture, pre-layout and post-layout. At each of these stages we have collaterals of different maturity and one approach will not work in all 3 phases. For example, in the architecture phase of a design we must usually rely on estimating ODC from prior generation data with some process/area scaling by working with chip architects closely. In the pre-layout stages a lot more is possible. For example, we can use power planning tools to create a mock-up layout of the full-chip and use EM tools to extract power/ground grid metal capacitance contribution. Diffusion capacitance is hard to estimate in pre-layout phase as it heavily depends on MOS layout implementation and here we must use prior generation design data and process/area scaling, however the contribution is relatively small to total ODC from prior literature. The big contributor to total decoupling capacitance in FPGA core is intrinsic gate capacitance arising from both non-switching gates and signal interconnect loading. This can be captured and modeled at block level in SPICE test benches for all the key building blocks which are repeated across the chip and individual values can be added up to estimate full-chip level ODC. SPICE simulators have ability these days to predict impact of wire loading from post-layout to first order before a post-layout parasitic file is available. Since we already know from our experiments on SPICE vs. EDA tool correlation on how much difference in ODC arises from change in toggling factor, we can use this

information to scale the value from AC analysis based on FPGA application toggling factor provided by system application architects. This will ensure that as we go from pre-layout to post-layout that the discrepancies and inaccuracies are minimized. Figure 13 captures the EDA methodology to come up with a reasonably accurate estimate of ODC in the pre-layout stage of a product design.

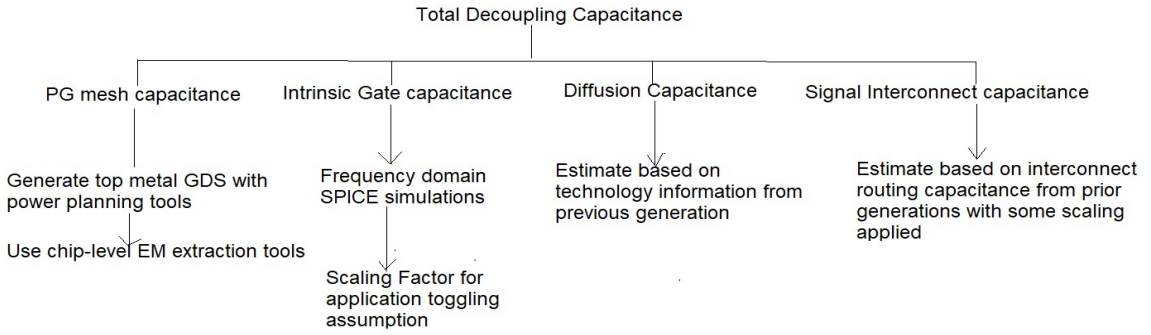

Figure 13: Pre-layout ODC extraction flow

In the post-layout phase, we have more mature collaterals available such as DRC/LVS clean database, IR drop spec compliant database, parasitic SPF etc. While these collaterals enable higher accuracy potentially, challenges of large run-times for analyzing core power forces users into various tradeoffs for black-boxing some contents before generating full-chip power model which is later an input to system PDN designer. At this stage it is important to explore all the knobs like tuning toggling factor, signal interconnect modeling considerations and inclusion of diffusion capacitance etc... to predict ODC more accurately through a combination of block level EDA flows and full-chip/system PDN flows. Figure 14 captures the EDA methodology to come up with accurate ODC estimate for final PDN sign-off

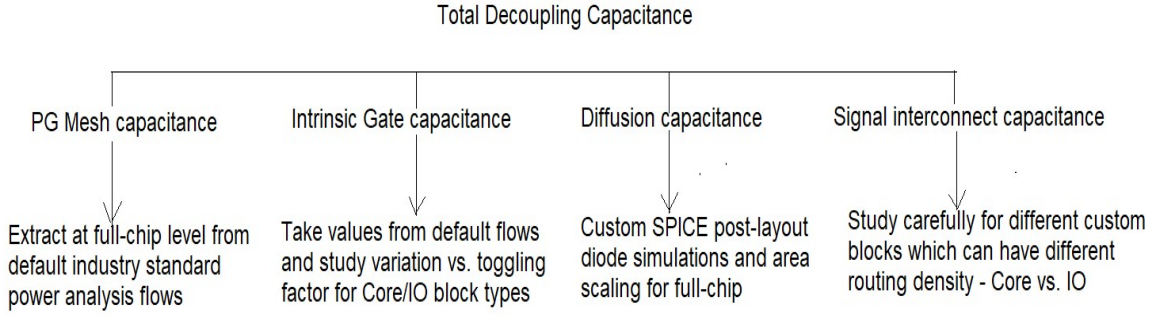

Figure 14: Post-layout ODC extraction flow

VI. Discussion of ODR extraction challenges

1. On-die resistance extraction challenges

On-die resistance extraction from EDA tools is more challenging than ODC as we must consider local resistance coming from decoupling capacitor hook-up (effective ESR for the capacitor) as well as global resistance all the way to bump from die level perspective. Since circuits are increasingly transitioning with fast rise times <=50ps, the RC time constant all the way to bump ports may be too large and we must consider local ports on metal layers closer to diffusion layer like M2 or M3. In addition, the problem becomes more challenging for Core PDN as impedance values are very small and could be <10mohms. Figure 15 shows simple lumped PDN topology for die/package to explain the difference between our definition of local and global ODR. Global ODR can be estimated reasonable accurately with simple traditional static DC IR drop analysis. Estimating local ODR is trickier and requires lot of experimentation with port location, port size in relationship to power hungry circuits which require them the most.

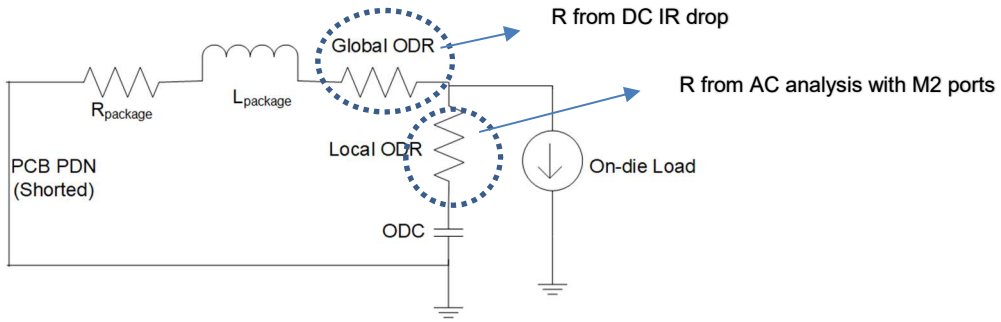

Figure 15: Representative lumped PDN model (showing local and global ODR)

2. Silicon correlation attempts for ODR

Identifying a block for silicon correlation was hard due to reasons discussed earlier in the ODC section. However, we attempted a qualitative correlation like the effort for ODC for core power domain using previous generation scaled measured data for ODR and comparing it with EDA tool extractions with ports set on bump layers and M2 layers. Table 6 summarizes ODR as function of frequency. We found out that the ODR value at 10MHz (which was our bench measurement frequency) was within 1% of the ODR values reported from EDA tool extracted ODR with M2 ports in table 6. This data, while encouraging is far from conclusive and is a start to more detailed deep-dive on this area in the future. Here we picked the value at 10MHz to match bench setup but picking a value close to 300MHz or so would cause greater deviation between measured ODR vs EDA tool extracted ODR.

Also, ODR from measurement is based on curve fitting to a lumped model topology and that could have some inherent inaccuracies as well. Another finding was that IO PDN is more sensitive than core PDN to choose port location/size as layout structures are more irregular compared to dense repeating power grid in core power domain. More distributed ports may be needed as mentioned in [9] for IO PDN ODR correlation. It is also noted from table 6 that ODR varies as a function of frequency and more analysis is needed on choice of frequency to pick for silicon correlation, whether it should be bench measurement frequency or frequency corresponding to low frequency PDN noise or high frequency local noise etc. Value of effective ODR reduces as frequency increases, since higher frequency implies smaller time for on-die load to traverse the local power bus to find charge from a local decoupling capacitor and hence less effective power bus resistance.

Port Location	ODR at 10MHz	ODR at 630MHz	ODR at 1.2GHz
Bumps	4.3mohms	1.2mohms	0.68mohms
Metal 2	5.2mohms	2mohms	1.5mohms

Table 6 - ODR extracted from EDA tool for FPGA building block (Using core PDN)

VII. Conclusion

SPICE vs. EDA tool correlation was discussed for ODC to gain deeper understanding of methodologies used by EDA tools for ODC extraction. Toggling factor, Signal interconnect capacitance are key contributors to total ODC in FPGA applications which need to be factored in through adaptation to EDA flows particularly for custom IP blocks. Diffusion capacitance (not a big contributor relatively speaking) is not typically modeled by EDA tools and post-layout SPICE simulations are needed for this for ODC correlation efforts. Pre-layout and Post-layout approaches to EDA flows are discussed to ensure accuracy of ODC extraction as we progress through different stages of maturity of a chip design. Silicon correlation is demonstrated for small FPGA IP blocks for ODC extraction while challenges and insights are discussed for FPGA Core PDN ODC extraction. ODR extraction challenges are discussed (particularly need to use ports on layers closer to MOS circuits for accurate extraction) and some encouraging observations indicate silicon correlation may not be too hard once all the collaterals are available.

VIII. Acknowledgements

The authors of this paper would like to think Veshal Sridar from Ansys, Patrick Ho from Sigrity for various useful technical discussions and Xiaoping Liu, Zhe Li, Sudhesh

Madhavan, Shishuang Sun for several useful inputs on collaterals, technical references and flow guides.

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