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A Novel Platform PI Isolation Design Approach, Upon IFPI with SPIM & UPIT

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Abstract

A novel platform power integrity (PI) isolation design approach is further developed, with Intel Fast PI, upon standard PI model (SPIM) and unified PI target (UPIT) to efficiently address HVM customers' largely design differentiation with power delivery network design & optimization including power rails' consolidation and isolation, and then design review & sign-off, to flexibly make trade-off between cost and performance, or between stack-ups and PD BOM cost. Such standardized design architecture has been adopted & deployed by leading EDA tools.

Author(s) Biography

Xingjian Kinger Cai is currently managing a power integrity team in client computing group in Intel Corp. Kinger acquired his Ph. D degree from Shanghai Jiao Tong University in 2001, and obtained MBA degree from W.P. Carey business of ASU. Kinger published more than 20 papers and holds 7 granted US patents.

Mohamad Shahrir Tamrin is a power integrity engineer in client computing group in Intel Corp. Shahrir acquired his Bachelor of Electrical Engineering from Stevens Institute of Technology, New Jersey. Shahrir has vast experience in designing power delivery network for both analog and digital domains.

Lun Foo Chee is a power integrity designer currently working in power Integrity team focusing on delivering PCH power integrity solution. Chee Lun has been working in Intel since year 2006, his first join work as validation technician. Chee Lun transition to a package power integrity engineer after completed BEE in year 2010.

Chi-te Chen is the Power Integrity Customer Support Lead in Client Computing Group in Intel Corp. Chi-te has more than 15 years technical experience in electrical analysis for system designs focusing on Power Integrity. She received BSEE from National Taiwan University, Taipei, Taiwan and MSEE from University of Washington, Seattle, WA.

I. Introduction

Platform power integrity (PI) design, has been facing the challenges of lacking efficient and effective EDA tool, shortage of Standardized PI Models (SPIM) and Unified PI Target (UPIT)[1], in order to flexibly design lower cost, higher performance, or smaller form factor systems on different stack-ups in client computing platforms. Conventionally system design customers had no other choice but to rigidly follow the single point PI solution with one set of PI PD BOM mostly on a particularly recommended stack-up, or "copy exactly" from the given customer reference board [2].

Intel developed scalable platform PI design approach iFPI (Intel Fast Power Integrity) to facilitate customers to quickly achieve platform level PI solutions for customized design differentiation, with SPIM and scalable UPIT for all particular power rails at client computing platforms. Such PI design approach has been successfully deployed for Ice Lake [6] products to Intel internal customers in reviewing and signing off Reference Validation Platform (RVP) boards design, and to external customers of OEM and ODM to help them making trade-off between PD BOM and PCB stack-ups, or between cost and performance, with lots of flexibilities, and then to automatically achieve PI design optimization and sing off, efficiently and effectively [3, 4].

Through co-engineering with commercial EDA vendors, scalable platform PI design architecture has been fully integrated into industry well known Cadence Sigrity iFPI-OPI flow for customers to quickly achieve PI solution satisfying the scalable UPIT with the flexibility of making trade-off among PD BOM of available capacitors in the industry, cost, performance, form factor including stack-up, board 3D size, as well as doing efficient PI design review and sign-off [5]. This iFPI-OPI flow has been deployed and well adopted by Intel customers from Ice Lake generation to timely address the MLCC shortage in the industry recently.

This iFPI-OPI flow consists of Standardized PI Model (SPIM) and Unified PI Target (UPIT), which covers both self and transfer impedance considering coupling noise from a major power rail to a noise sensitive power rail. While self-impedance is normally used as a benchmark for most of PI designs, transfer impedance is now becoming more crucial for sensitive analog rails like Clock, and PLL to meet very tight coupling noise requirements.

II. Methodology

A. Power Delivery Network, (PDN) and Impedance Profile, Z(f)

Platform Power Delivery Network (PDN) normally can be simplified into a cascaded RLC lump network, which consists of 3 major blocks: 1) on-die capacitors (MIM/MOS) 2) on-package capacitors (land-side/die-side) 3) on-board capacitors, which includes Voltage Regulator components. The corresponding impedance profiles, Z(f), of PDN without on-die capacitance, and of PDN without on-die and on-package capacitors are shown in Fig.1. As clearly shown in the Z(f) plot, platform level PI design which

generally covers up to approximately 20MHz, is mainly contributed by on-board and on-package capacitors, due to the closely interaction through BGA, pin or socket connection. Meanwhile, the contribution from on-die capacitor contribution is negligible to frequency range below 20MHz.

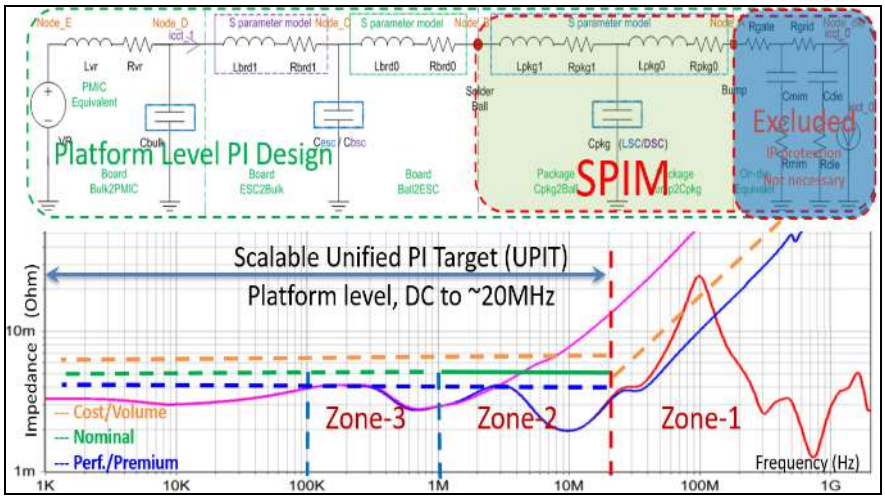

Fig.1 Platform PDN and Z profiles with different level Caps

B. iFPI - OPI flow:

On-die (Zone-1) and on-Package (Zone-2), PI designs are strictly governed by internal PI team. Once they are clearly defined, all PI collaterals of SPIM of package including all LSC and DSC, and the corresponding UPIT will be deployed to customers for platform PI design. Within iFPI-OPI flow, customers could quickly merge their platform design board database with a particular SPIM to automatically optimize, review and eventually sign off the PI design for any concerned power rail, against a desired scalable UPIT in Fig. 1 to satisfy budgeted cost, performance, and form-factor simultaneously as shown in Fig.2.

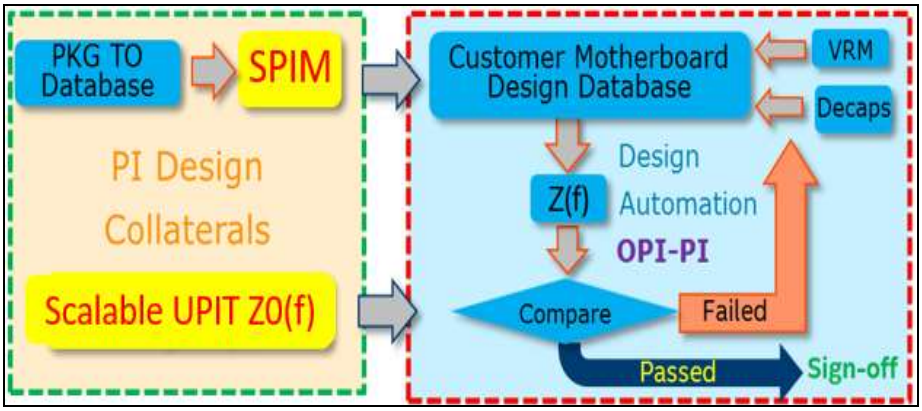

Fig.2 Scalable Platform level Power Integrity (PI) design architecture

C. Unified Power Integrity Target (UPIT)

Unified Power Integrity Target (UPIT) as shown in Fig.3 has been converged in frequency domain, covering both impedance requirements from Power Delivery (< 1MHz) and Power Integrity (<20MHz), focusing on platform with SoC usually having on-package capacitors. UPIT is scalable, and can be applied for both high-current compute domain, as well as I/O analog/digital domain. For high-current compute domains, like CPU Core, different UPIT values can be used to make trade-off between performance, power, and PI-PD BOM cost. Lower UPIT normally means CPU can achieve multiple-turbo at higher frequency, or both CPU and GPU concur at higher frequency for overall better performance.

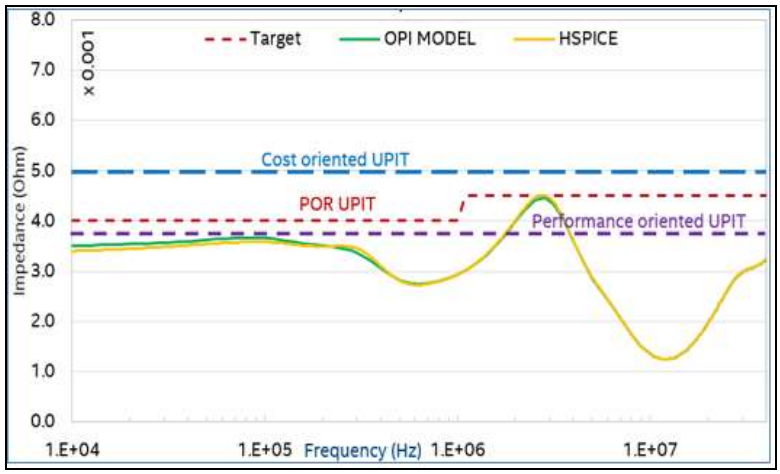

Fig.3 Scalable UPIT – Unified PI Target

Meanwhile, for IO interface power rails, higher UPIT will result in smaller PDBOM at expense of IO performance –running at relatively lower data rate. However, there are few sensitive analog rails like Clock and PLL which are sensitive to coupling noise, hence require very good isolation scheme. To address this isolation requirement, transfer impedance UPIT is provided, in addition to self-impedance UPIT, as shown in Fig.4, to ensure the functionality and performance of the interface.

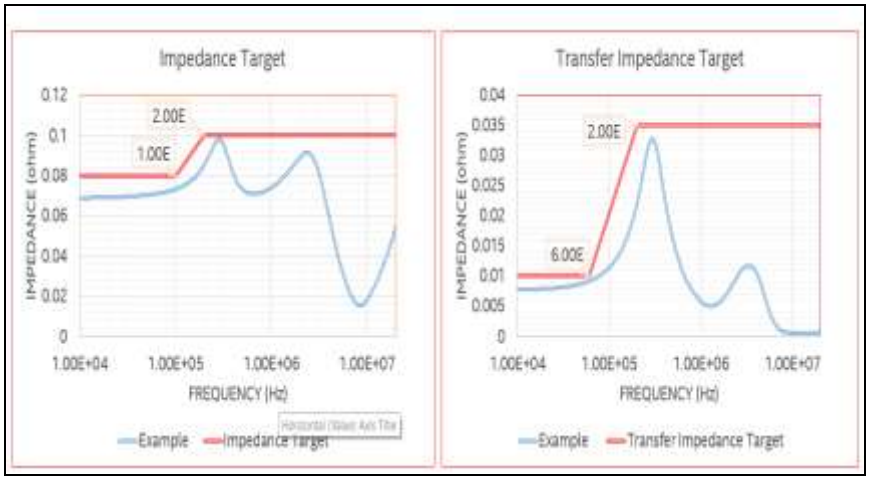

Fig.4 Self and Transfer Impedance UPITs

D. Standard Power Integrity Model (SPIM)

Standard Power Integrity Model (SPIM), as shown in Fig.5, covers all power rails with routing path going through board level, regardless voltage source originating from board or silicon. SPIM format has also clearly identified Stimulus and Observation ports. For Stimulus ports, AC current excitation, either uniformly or unevenly distributed, has also been defined to enable more accurate simulation results.

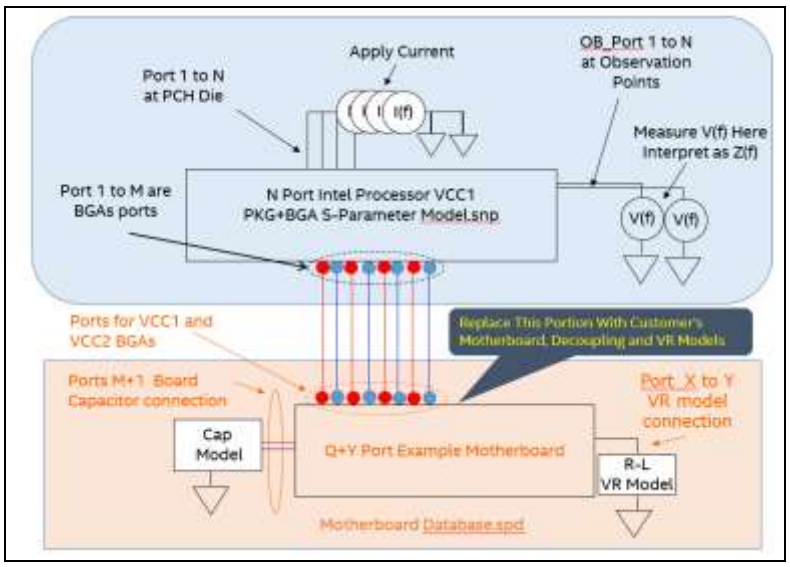

Fig.5 Standard PI Model (SPIM) Overview

For power rails with specific isolation requirements, special SPIM format is provided, as shown in Fig.6, for which an additional Observation Port is defined for transfer impedance plot. To avoid potential manual mistake, SPIM format also consists of pin information awareness for each power rails. Last but not least, SPIM has a wrapper including all pins information and all Stimulus and Observation ports information, on top of a standard touchstone s-parameter, which eventually makes it more meaningful and easy to use.

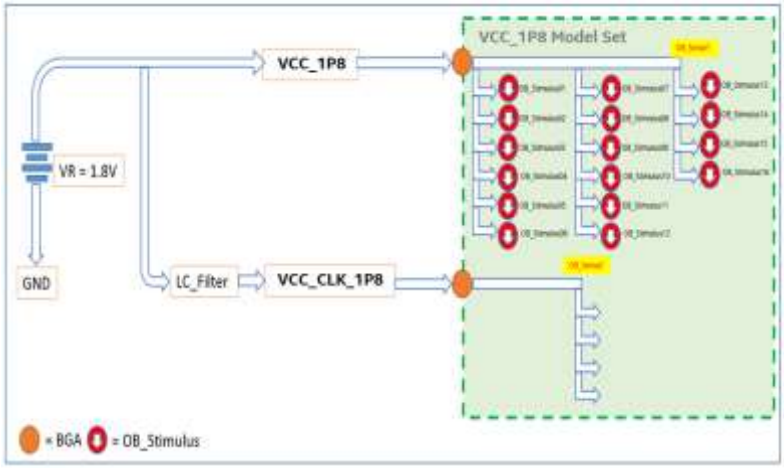

Fig. 6 Scalable UPIT with different PD BOM cost.

III. Results

Scalable Platform level Power Integrity (PI) design architecture iFPI in Fig. 2 has been first-time ever adopted and implemented in iFPI-PI with Standardized PI Model (SPIM) and Scalable Unified PI Target (UPIT) in industry well-known Cadence Sigrity Power Optimize.

As shown in Fig. 7, scalable platform PI design could be optimized for satisfying different UPITs on the same stack-up. Normally lower UPIT results in higher PD BOM cost, vice versa. Smaller Z-height results in thinner layer copper thickness degrading Z profile, which might be compensated by higher PD BOM cost. Finally the specific PI design settles down at minimum baseline BOM cost for load line (LL) UPIT1 of 4.5mO for Z-height of 0.8mm, and 153% more BOM cost for LL UPIT2 of 4.1mO for Z-height of 0.65mm, with both chip solder-down on 6-layer T3 stack-up. The design flexibility provided by this scalable platform PI design approach is very essential in enabling customers to differentiate their platform from the rest of their competitors.

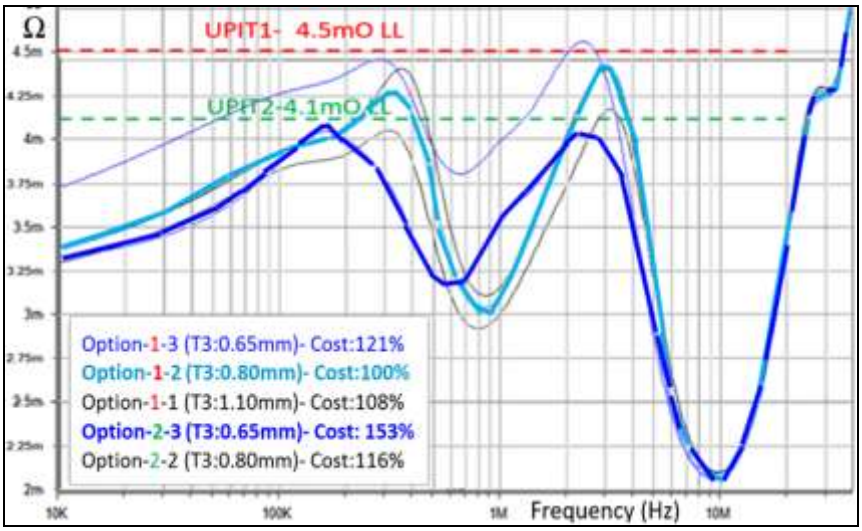

Fig. 7 Scalable UPIT with different PD BOM cost

In addition to that, this scalable platform PI design is also capable to take care isolation requirements. In this special case, PI designer will first decide which rails are to be considered as “aggressor” and “victim” rails. These selected rails will then have two sets of UPITs: 1) self-impedance target; 2) transfer-impedance target from “aggressor” to “victim”. The transfer impedance target can be used as isolation guidelines for customers to follow. As shown in Fig. 8, there are two separate board designs, named Option1, and Option 2. From the transfer impedance plot, customer can instantly know whether they are meeting isolation requirement or not. Besides, this new approach will also enable customers to conveniently debug their designs whenever they fail to meet specified UPIT. This scalable platform PI design approach is definitely better and transparent to customers as it can provide quantitative information and allow customers to make a data driven decision, unlike PI traditional isolation guidelines, which typically spell out rigid physical requirements for components placement and selection.

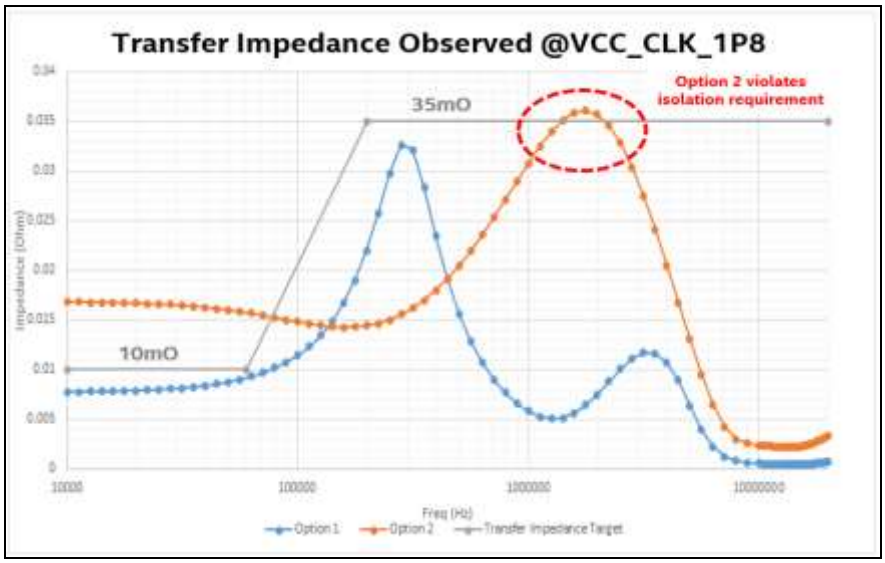

Fig.8 Transfer Impedance UPIT with different platform design

IV. Conclusions

For one client product supports 10+ stack-ups, with options of components stuffing and sockets, in order to support customers' High-Volume-Manufacture (HVM) largely platforms design differentiation, besides providing conventional platform design guideline with one set of PD BOM as a starting baseline PI solution, scalable platform PI design approach has been successfully integrated into commercial EDA tools, and deployed to both internal and external customers with SPIM and scalable UPIT, to enable platform PI design flexibility, considering PI isolation, with trade-off among PDBOM, stack-ups, cost and performance, to facilitate platform PI design review and sign-off efficiently, to reduce customer support effort, and to enable platform design innovations.

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