DesignCon 2019

Capacitor Insertion Methodology to Power Distribution Network for Improving Power Integrity

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Abstract

Power supply voltage noise mitigation techniques are becoming more and more important in order to improve stability and to realize high speed operation circuits. Stability of power supply is usually realized by lowering PDN impedance using decoupling capacitors. However, the relationship among number/kinds of decoupling capacitors, PDN impedance and power supply voltage droop distribution inside of an LSI chip is not yet clear. This paper evaluates the relationship in terms of its frequency characteristics as well as its time-domain waveforms. Not only with electro-magnetic frequency domain analysis and transient simulations, we designed and fabricated a prototype LSI chip assembled on an evaluation board to measure actual PDN characteristics and power supply voltage droop of the LSI chip.

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Toru Nakura received the B. S., and M. S. degree in electronic engineering from The University of Tokyo, Tokyo, Japan, in 1995 and 1997 respectively. Then he worked as a circuit designer of high-speed communication using SOI devices for two years, and worked as a EDA tool developer for three years. He joined the University of Tokyo again as a Ph.D student in 2002, and received the degree in 2005. After two years industrial working period, he is back to academia as an associate professor at VLSI Design and Education Center (VDEC), and Electrical Engineering and Information Systems, in The University of Tokyo. He is now currently working as an full professor in the department of Electronics Engineering and Computer Science in Fukuoka University. His current interest includes signal integrity, reliability, power supply, digitally-assist analog circuits, and fully automated analog circuit synthesis.

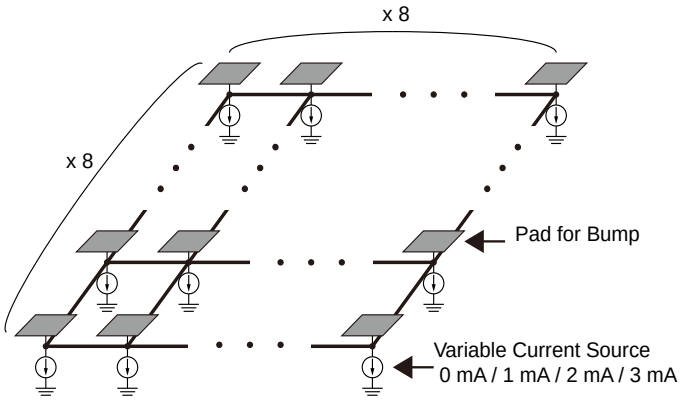
Introduction

Noise mitigation techniques for power supply are becoming more and more important in order to improve stability and to realize high speed operation of LSI circuits. Stability of power supply is usually realized by lowering PDN (Power Distribution Network) impedance by using decoupling capacitors[1],[2]. Moreover, [3] shows the total PDN design which means chip, package and board and cost-effective PDN design methodology to improve Power Integrity. However, the relationship among number/kinds of decoupling capacitors, PDN impedance and power supply voltage droop distribution inside of an LSI chip, is not yet clear. This paper evaluates the relationship in terms of its frequency characteristics and its time-domain waveforms, by simulation analysis. Mainly due to the inductance from the land side mounting capacitors to the power consuming circuit on the LSI chip as well as the resistance of the PDN of the LSI chip, our simulation results show that the power supply voltage droop distribution along the chip depends on the position/number/kinds of the land side mounting capacitors, and of course, the position of the power consuming circuits.

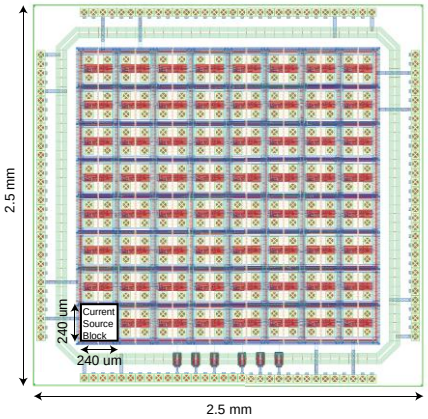
We have fabricated a prototype LSI chip using standard 0.18 um CMOS technology and an interposer on a PCB board with their detailed simulation models. We will show detailed simulation results of the power supply voltage fluctuation waveforms of various kinds of assembly and operating conditions. These results help us to estimate and find more efficient decoupling capacitor insertion to power distribution network for improving power integrity.

System configuration of the evaluation board

TEG IC design for observing power delivery network



(a) 8 x 8 variable current sources and power delivery network.



(b) Chip layout design of the TEG IC.

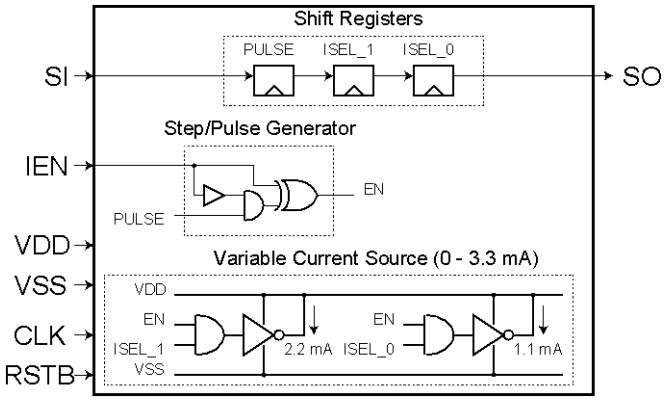
Figure 1 Overview of a TEG IC.

We design a TEG IC for observing the voltage droop distribution in various situations. As shown in Figure 1(a), we introduce a mesh structure of VDD/VSS network and an array of current sources to represent a PDN with an LSI chip. In the model, power is supplied from the interposer to the VDD and VSS mesh network through bumps and pads.

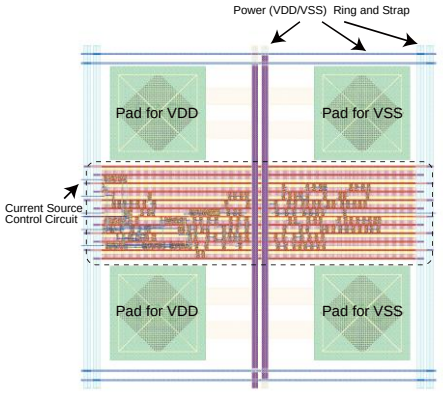
The current sources in the model can vary the amount of the current so that we can observe the voltage droop distribution under some spatial uniformity of IC operation. The current of each current source can be selected among four value, 0m A, 70m A, 140 mA, 210 mA. We designed the TEG IC chip by using standard 0.18um CMOS technology. Figure 1(b) shows the full chip layout of the TEG IC in which 64 (8 x 8) current sources, PDN mesh, and VDD/VSS pads for power supply. The size of each current source block is 240 um x 240 um and the total chip size is 2.5 mm x 2.5 mm.

Figure 2 (a) shows the circuit diagram of each current source block. VDD and VSS are connected to the interposer through pads and bumps. A clock signal CLK and a reset signal RSTB are used by digital control circuits. To control the amount of current, two registers, ISEL_1 and ISEL_0, are used. The register PULSE decides the mode of the current source, i.e. “PULSE” or “STEP”. By connecting all current blocks serially, in other words, by connecting SO of the previous block to SI of the next block, registers in all current source blocks can be set through the long shift registers. A signal IEN is distributed to all current source blocks simultaneously and the signal EN which drives current source is generated according to the value of the register PULSE. The current source is composed of two inverters (logical “NOT” circuits) whose output is connected to VDD. When the input of the inverter is logic “0”, the output is logic “1” and no current flows from VDD to VSS. On the other hand, when the input is logic “1”, the logic “0” output is connected to VDD and a fixed current flows from VDD to VSS. The two inverters have different drivability so that the amount of the current source can be four values. Figure 2(b) shows the layout design of the current source block. There are four pads for bumps of VDD/VSS. Current source and control circuits are placed at the center of the block. In addition, power (VDD/VSS) rings and straps are routed to make a mesh network.

Throughout the design, we use a typical digital design flow which exploits commercial logic synthesis tool (Design Compiler from Synopsys Inc.) and P&R tool (IC Compiler from Synopsys Inc.) to easily change circuit parameters such as circuit size, amount of current, etc. If we want to change some parameters, what we should do is only to modify script/configuration files which will be given to the tools. We extracted a transistor level SPICE netlist with parasitic resistance and capacitance of the whole chip from the final layout using an RC extraction tool, and following simulations use the SPICE netlist.



(a) circuit of current source block.



(b) Layout design of the current source block.

Figure 2 Design of the current source block of the TEG IC.

Test board design

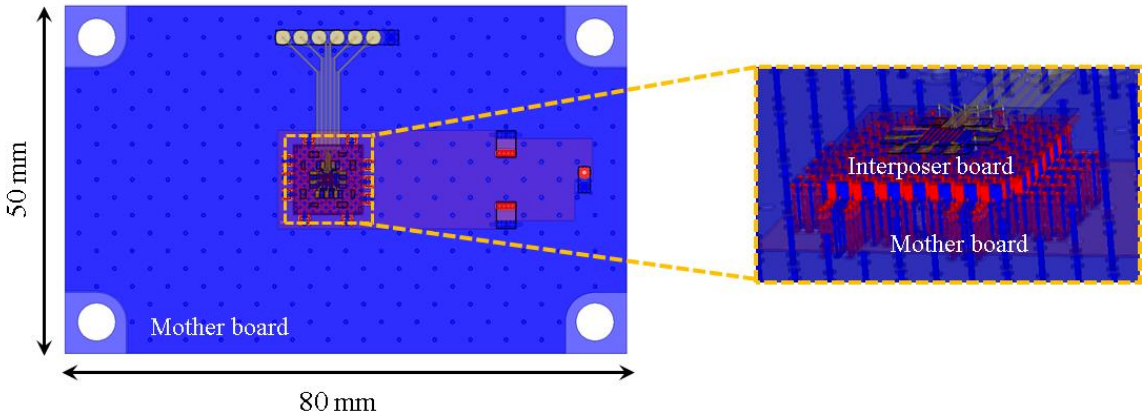
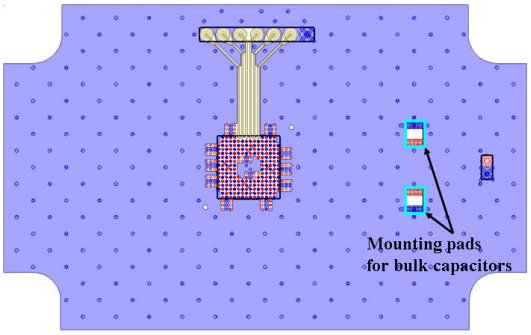
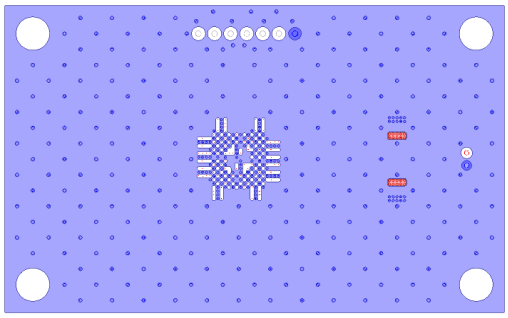


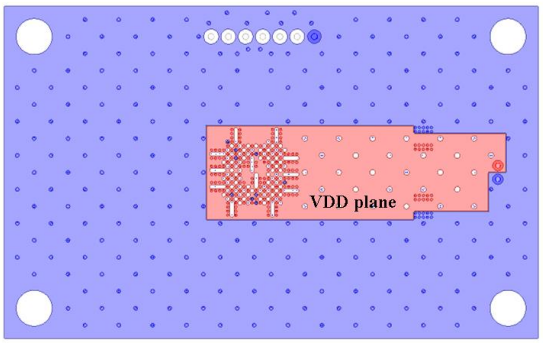
Figure 3 Structure of the test board.



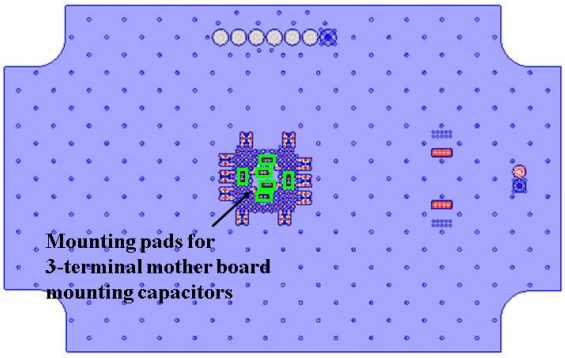
(a) Layer 1 of the mother board (top).



(b) Layer 2 of the mother board.



(c) Layer 3 of the mother board.

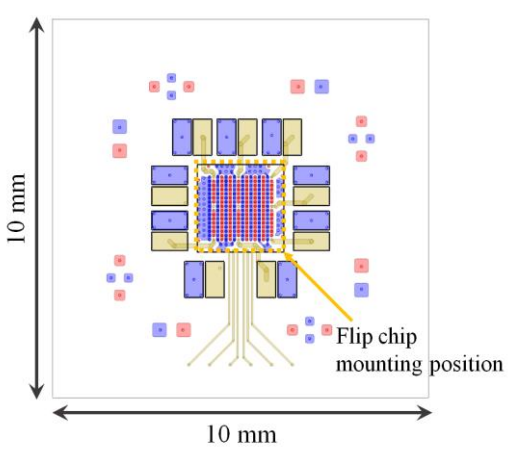


(d) Layer 4 of the mother board (bottom).

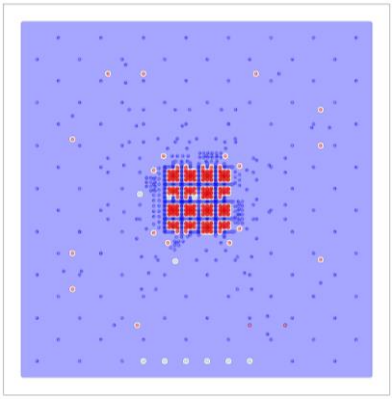
Figure 4 Each layer of the mother board and mounting locations of capacitors.

Figure 3 shows a structure of a test board which consists of an interposer and a mother board. The size of the mother board is 80 mm x 50 mm and the size of the interposer board is 10 mm x 10 mm. The thickness of the mother and interposer are 0.756 mm and 0.292 mm, respectively. We assume that the LSI chip is attached on the interposer which is assembled at the center of the PCB board that has power/ground connectors on the corner. We use three types of decoupling capacitors, land side mounting capacitors attached at the backside of the interposer under the chip, mother board mounting

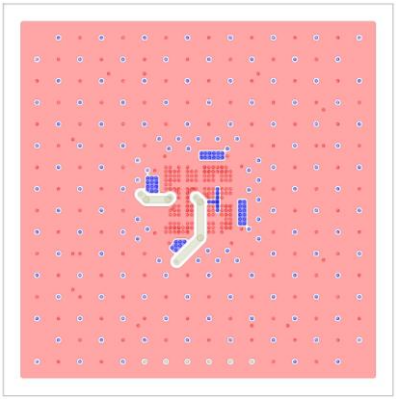
capacitors attached at the backside of the PCB board under the interposer, and bulk capacitors just next to the power/ground connectors. Figure 4 and 5 illustrate each layer of the mother and interposer board. In addition we use four kinds of capacitors as the land side mounting capacitor; general type capacitors, reverse geometry type capacitors, 3 terminal capacitors and silicon capacitors .



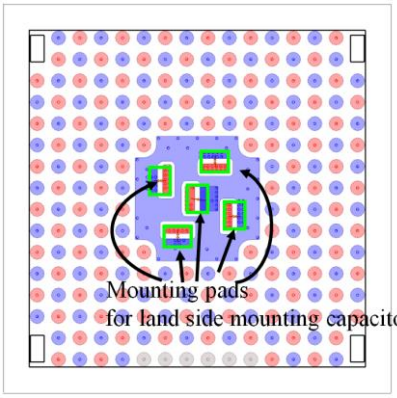
(a) Layer 1 of the interposer board (top).



(b) Layer 2 of the interposer board.



(c) Layer 3 of the interposer board.



(d) Layer 4 of the interposer board (bottom).

Figure 5 Each layer of the interposer board and mounting locations of capacitors.

Evaluation results

In this section, we verified accuracy of simulation results by comparing measurement and simulation results of the PDN impedance. After that, we evaluate PDN performance inside of an LSI chip, namely, seen from the metal layer of the chip. Particularly, we evaluate the relationship between PDN performance and the position/kind of decoupling capacitors in order for lower PDN impedance design. Finally, we conduct transient analysis to see the power supply voltage fluctuation waveforms to validate relationship between the PDN impedance design and operating position on the LSI chip and the power supply noise.

PDN impedance

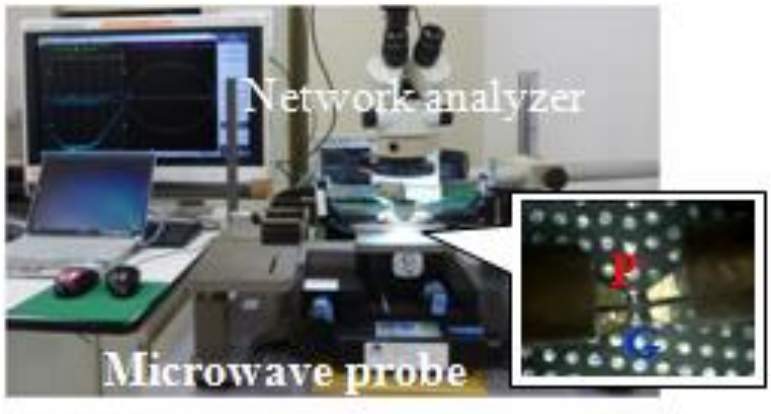


Figure 6 Measuring system for the PDN impedance.

We use vector network analyzer(Keysight Technology, E5061B) and a 50 Ω microwave probe (Cascade Microtec) to measure the PDN impedance of the test board. The measuring systems is shown in Figure 6 Moreover, we utilize an electro-magnetic simulator to extract the frequency characteristics of the interposer and the PCB board. In this experiment, the mounting condition of the mother board is always the same that 2 pcs. Bulk capacitors are mounted on the top side of the mother board and 6pcs. 3 terminal decoupling capacitors is also mounted on the bottom side of the mother board. Only 1 pc. of land side capacitor is mounted on the upper left corner of the interposer with changing its kind: general type, reverse geometry type, 3 terminal and Si capacitor. Figure 7 shows the PDN performances of the capacitors themselves. General type has the largest impedance over 200 MHz, followed in order by the reverse geometry type, the 3 terminal and the Si capacitor. Figure 8 shows simulation and measurement results of frequency characteristics of the PDN impedance of the interposer on the mother board with capacitors. As shown in Figure 8, the PDN impedances of the measurement and simulation are almost the same and that shows our simulation results are accurate enough and reliable. Hence, we will use only simulation results. We evaluate frequency characteristic of the PDN impedance seen from the LSI chip whose observing points are shown in Figure 9, and the AC simulation results are also shown in Figure 10. As noted in the previous section, the land side capacitor is mounted on the back side of the interposer board at the upper left corner. We focus the anti-resonance of PDN impedance peak, it is lowest seen from port 5, because the land side mounting capacitor is mounted at the backside of port 5 through the metal of the chip and the interposer board. Moreover, anti-resonance peak of PDN impedance becomes lower by mounting a Si capacitor. These results show that PDN impedance becomes lower by implementing a Si capacitor near the observation point. In addition, in order to evaluate the PDN impedance during the circuit operation, we also evaluate PDN impedance according to $Z(f) = V(f)/I(f)$ where $V(f)$ is the power supply voltage spectrum and $I(f)$ is the spectrum obtained from a transient simulation waveforms of composite current, and the results are shown in Figure. 11 where we can see that they have similar curves to the AC results of Figure. 10. Hence,

the lowest PDN impedance performance is achieved by mounting the lowest ESL Si capacitor.

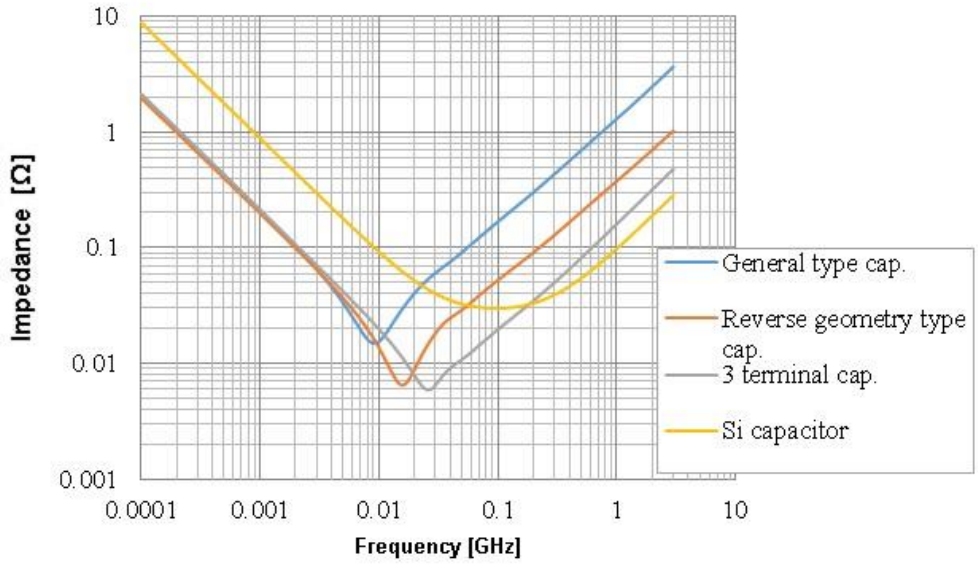


Figure 7 PDN impedance of capacitors themselves.

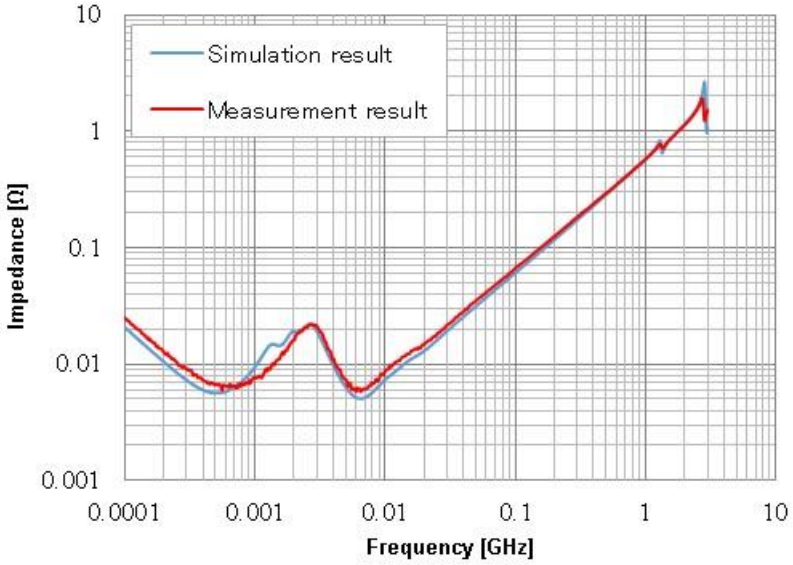


Figure 8 Measuring and simulation results of PDN impedance (with a general type capacitor mounted on the upper left).

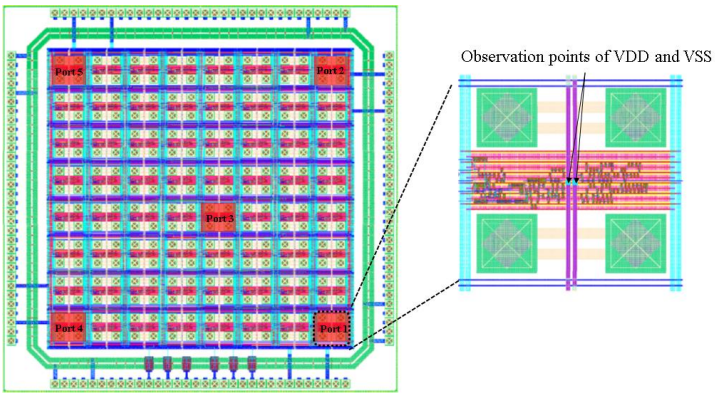
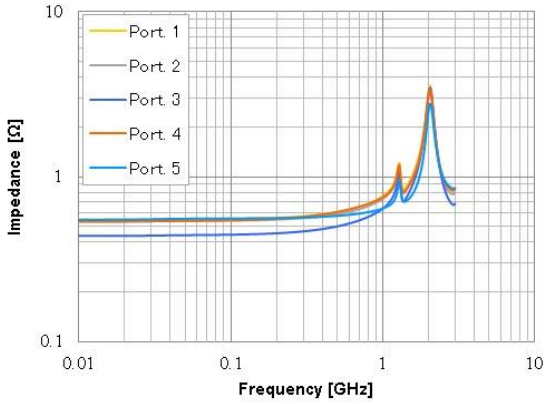
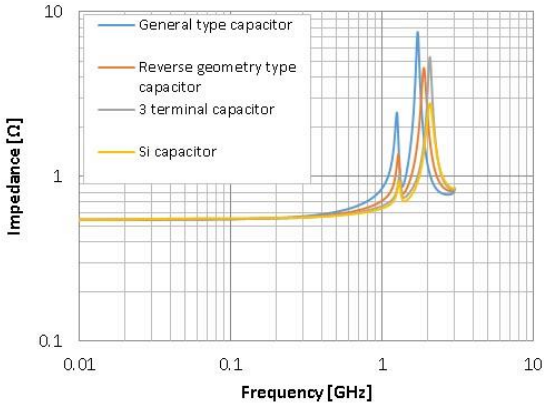


Figure 9 Observation points of the chip metal layer.

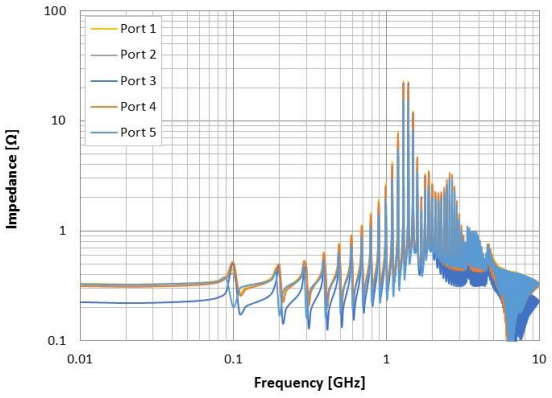


(a) PDN impedance seen from the chip metal with a Si capacitor mounted on the upper left corner.

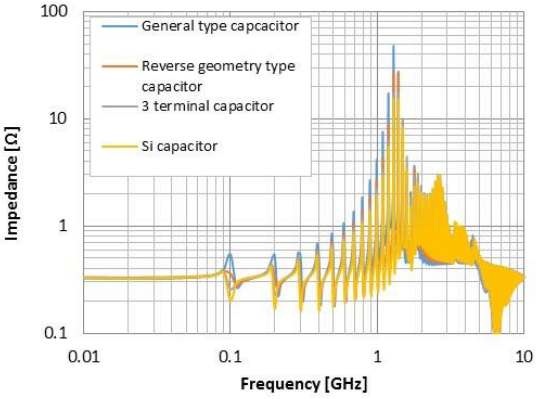


(b) PDN impedance seen from the chip metal at port 5 with 4 kinds of land side capacitors mounted on the upper left corner.

Figure 10 PDN impedance performances seen from IC metal layer.



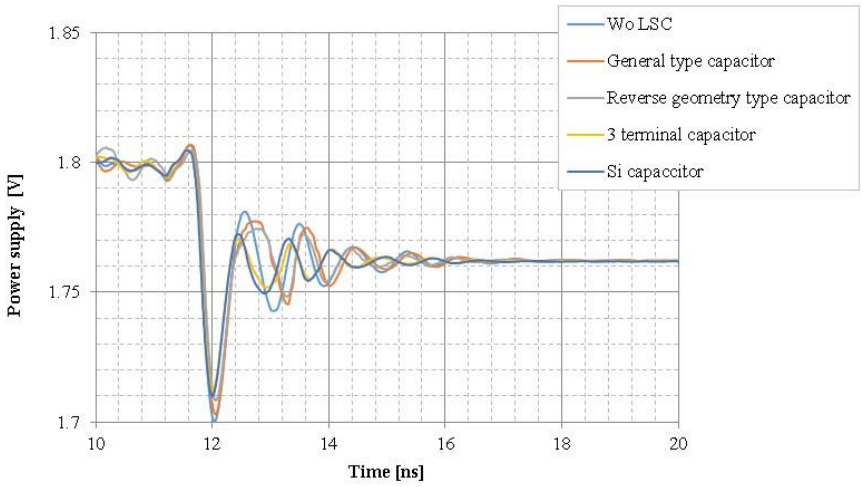
(a)PDN impedance seen from the chip metal with a Si capacitor mounted on the upper left corner.



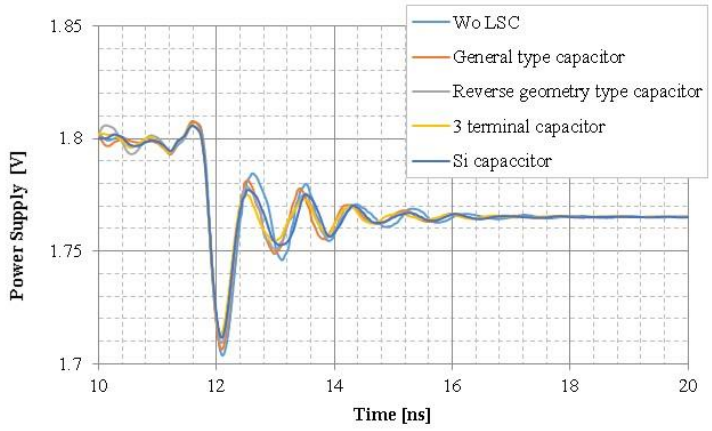
(b)PDN impedance seen from the chip metal at port 5 with 4 kinds of land side capacitors mounted on the upper left corner.

Figure 11 PDN impedance performances calculated from transient simulation waveforms.

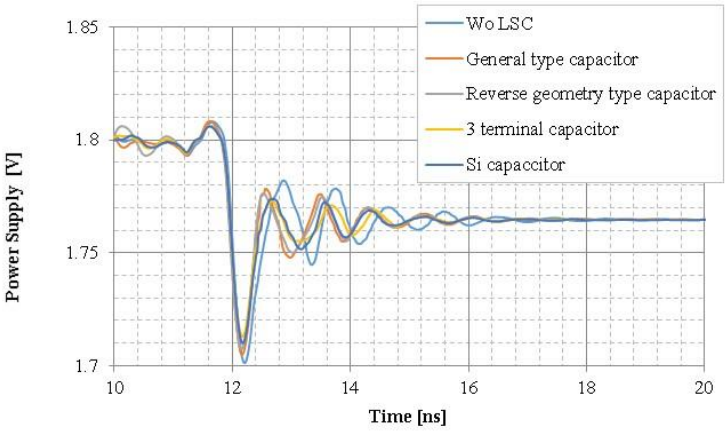
Voltage fluctuation



(a) Power supply voltage seen from port 5 when the upper left corner block star to operate.



(b) Power supply voltage seen from port 2 when the upper right corner block start to operate.



(c) Power supply voltage seen from port 4 when the upper right corner block start to operate.

Figure 12 Transient simulation result of the voltage power supply.

To validate the effects of the lower PDN impedance design by using low ESL capacitors, we evaluate the transient simulation waveforms of voltage power supply. Figure 12 shows transient simulation results which is only 1block (The operating block is changed from Figure 12(a) to (b) and (c)) is operated and 1pc capacitor is mounted as a land side mounting capacitor where the back side of port 5 (upper left corner of chip) through the metal of the chip and the interposer board. Also the mounting kinds of capacitors are changed. Table 1 summarizes the power supply voltage drop, where we divide the power supply voltage drop into DC drop and AC drop as shown in Figure 12(a). Here we pay attention to the AC drop since decoupling capacitor mainly affects the AC drop, not the DC drop. As shown in Figure 12 and Table 1, we can improve power integrity by mounting land side mounting capacitors. In particular, the AC voltage drop is decreased to 0.0499 V and 0.0518 V by mounting 3 terminal and Si capacitor. Moreover, the AC voltage drop is decreased by mounting a capacitor as close as the chip operating position.

	Vdrop-AC at port 5 (Upper left corner is operated.)	Vdrop-AC at port 5 (Upper right corner is operated.)	Vdrop-AC at port 5 (Lower left corner is operated.)
Wo LSC	0.0619	0.0615	0.0635
General type capacitor	0.0592	0.0588	0.0598
Reverse geometry type capacitor	0.0539	0.0559	0.0573
3 terminal capacitor	0.0499	0.0519	0.0518
Si capacitor	0.0518	0.0535	0.0546

Table 1 Transient simulation result of Vdrop-AC with the capacitors mounted at upper left corner through the IC metal layer and the interposer board.

Conclusion

In this paper, we evaluate the relationship among kinds of decoupling capacitors, PDN impedance and power supply voltage droop distribution inside of an LSI chip. As a results, the PDN impedance becomes lower by mounting a Si capacitor which has lower ESL than an MLCC. In addition, the degradation of voltage power supply can be suppressed by mounting a Si capacitor close to the operating positon of the chip.

Acknowledgments

This work has been supported by VLSI Design and Education Center (VDEC) in collaboration with ROHM Co., Ltd., TOPPAN PRINTING Co., LTD., Synopsys, Inc., Cadence Design Systems, Inc., and Mentor, a Siemens Business.

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