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Distributed decoupling capacitors application for PDN designs of fine pitch BGA products

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Abstract

The drive to reach low power, high-efficiency and fastest performance forces the designers to adopt fine pitch BGA, micro CSPs and micro BGAs technologies. Discreet decoupling capacitors under BGA area provided a suitable solution for controlling PDN impedance at MHz to GHz frequency band for many years. However, this is no longer a feasible solution for the new generation of products as the BGA pitch is below 0.8 [um]. In this paper we will examine the use of distributed capacitors based on thin and ultra-thin film laminates for controlling PDN impedance of fine pitch BGA designs, along with several other approaches such as Si based capacitors and distributed capacitor of standard laminates. The resulting power integrity simulation as well as PDN lab measurements are presented for the different options. Additional practical product design aspects such as manufacturability and reliability are discussed and the limitations for each solution are examined as well as its key benefits.

Author(s) Biography

Alex Manukovsky is a Technical lead of the Signal & Power Integrity team at Intel Networking Division, responsible for the development of indoor link simulator for high speed serial links, combining both traditional methods of frequency and time domain simulation along with machine learning capabilities. Alex focuses on simulation to lab correlation for high speed serial links for PCIe and Ethernet technologies and ML. His past work focused on channel modeling, robust deembedding and calibration techniques for VNA and TDR. His experience includes developing test equipment for compliance testing of serial I/O's as well as lab measurement methodologies for volume testing and Si/Pi simulations. Alex joined Intel in 2010 after receiving his BSc in Electrical Engineering from the Technion – Israel Institute of Technology. He is currently pursuing his Master's degree in System Engineering from the Technion – Israel Institute of Technology.

Igal Fridman is Senior Hardware Engineer with Infrastructure Networking Group, Broadcom Inc. His current role to design state of the art high speed SerDes test-board solutions and provide advanced PCB material selection that supports increasing signaling rates. In the past he provided complex SerDes via structures optimization, and led DDR4/GDDR5 post-silicon validation. Previously, Igal was with Intel responsible for SerDes pre-silicon simulations and Freescale post-silicon analog characterization. Igal has more than 10 years' experience with high-speed system design and simulations, PCB structure optimization, high-speed and analog validation. Igal graduated from Ben-Gurion University of Negev, Israel at 2003 and obtained M.Sc. at 2007 from the same university.

Shimon Morodooch is a R&D Project Manager, Harmonic Video Networks. He has over 24 years of experience of various hardware design aspects in the field of telecommunications and networks, covering design and managerial positions. Through the years he was involved in chassis designs starting as a board designer all the way to system level definitions of the whole chassis, its backplane, signal/power integrity and management. In recent years he is working in the cable edge industry and more focused on the hardware technological aspects, staring from in-depth characterization and selection of building blocks (e.g. PCB materials, high dense system design, etc.) through detailed SI/PI simulation analysis and at the end - full lab characterization of all hardware aspects of the System.
Specialties: Advanced High Speed Signal & Power Integrity analysis.
Extensive lab characterization of PLLs, SerDeses, Memories, PI, Chassis Hardware architecture mechanical & electrical design

Amiram Jibly is a System Engineer in the Network ASIC design team at Intel, has been with Intel in the last 7 years and is experienced in package and board design for high speed systems and signal integrity. His current work focuses on 100 Gb Ethernet validation systems and SI. His experience includes Si/Pi simulations for 25 and 56 Gb products and accurate measurement based modeling of passive interconnects. He received his BSc Degree from the Jerusalem College of Engineering in 2012.

Introduction

Industry Trends

During the past 50 years, we have witnessed a minimization in VLSI scale, well predicted by Moore law: the minimal switching part being decreased by a factor of approximately two every two years, providing a higher level of computational capabilities. As a result, the power density and requirements for power supply are increased as well.
Rapidly switching with high current transients VLSI circuitry requires available, nearby energy sources to allow sufficient current sources for MOSFET gate charging.
On the other hand, the products are being minimized, for example, smartphones, laptops, IoT devices etc. The VLSI components inside these products are minimized as well, including the smaller pitch of BGA. The recent BGA pitch of 0.3mm presents a multi-dimensional challenge, including power delivery and manufacturability. There are examples[1] of successful implementation, despite the lack of technology readiness and maturity. PCB (Printed Circuit board) assembly houses rely on previous generation methods to support advanced, denser designs. It includes a layout engineer using 0.5mm techniques ignoring the 0.3mm design introduced challenges.
The drive to reach low power, high-efficiency, and the fastest performance is forcing the designers to adopt fine pitch BGA, micro CSPs and micro BGAs technologies. Although reducing BGA pitch has many advantages, it introduces new challenges for the Power Integrity designers. One of those is associated with decoupling capacitors for PCB and package level PDN network design. While traditional techniques of locating decoupling capacitors under BGA area provided a suitable solution for controlling power delivery network (PDN) impedance at MHz to GHz frequency band for many years, they are impractical for the new generation of products as the BGA pitch is below 0.8 [um]. While the mechanical dimensions of electronic products decrease, the pin count remains unchanged, and for some market segments even increases, as there is no longer enough available area on PCBs to locate a sufficient number of decoupling capacitors due to the physical dimensions of the discrete components.

[1] "Taking on the 0.3 mm ultra-fine pitch device challenge in PCB design ...." 4 Oct. 2011, https://www.embedded.com/design/system-integration/4228981/Taking-on-the-0-3-mm-ultra-fine-pitch-device-challenge-in-PCB-design. Accessed 17 Dec. 2018.

PCB design aspects of fine pitch BGA products

Fine pitch BGA layout has some unique limitations, to address the challenges these limitations introduce several BKMs are adopted by PDN designers across the industry. Some of the most common ones are listed below.

- Two types of land patterns are commonly used for micro BGA pads – NSMD (non-solder mask defined pads) and SMD (solder mask defined pads).
- Traditional dog-bone fan-out pattern is not appropriate for a micro BGA due to its narrow pitch. Either via in pad or blind/buried vias are used.
- Avoiding high-end fabrication techniques along with minimizing the number r of layers is possible when a regular 6 mil via size is implemented for all fan-out/route of micro BGA pins.
- A common practice for decoupling PDN is to place capacitors on the opposite side of the PCB with respect to the micro BGA device and within the grid of vias and contact used to route signal traces to the micro BGA device.
- It is not feasible to use 0201 or capacitors with bigger packages directly underneath the device due to the small 0.4mm pitch micro BGA package size. Either a 01005 or smaller package is recommended.
- It is a good practice to keep all parts with 20 to 25mm clearance around the micro BGA facilitating re-work of the micro BGA without damaging nearby components.

Decoupling solutions for fine pitch BGA Designs

PDN includes VRM that provides desired stabilized DC voltage, printed circuit board (PCB) that conveys the electrical energy (voltage/current) towards the load, the load itself that consists of the package and die, Figure 1. Each of these stages has capacitance amount and frequency response. Closer to the load the capacitance decreases and the capacitor responsiveness increases. This paper is mainly focused on the PCB stage of PDN, which does not have the same scalability factor as VLSI circuitry.
While the need for a change in PDN design practices is becoming more obvious, no BKMs and widely accepted design practices have yet emerged across the industry. However, several technologies are to be considered when addressing these challenges.

PCB and Package mounted ultra-small size decoupling caps

Implementation capacitors under BGA with capacitors package dimensions below 0402, such as 0201, 01005 or even smaller, lead to a high-end assembly house, with potentially high cost, time and/or yield outcome. Any potential re-work will require just as much precise skills and equipment. The cheaper the components on PCB become, the more attention by perhaps the most expensive investment of the assembly process[2].
This solution is very unique and can rarely be implemented in customer and enterprise markets, where product cost and time are possibly the most important considerations. Several more aspects and challenges are presented further.

On-die capacitance

The implementation of on-die capacitance involves either Metal insulator Metal (MiM or MOM) capacitor or structures built in active silicon area MOS (Metal-Oxide-Semiconductor) capacitor.
The MiM capacitor is a plate capacitor between two metal layers with a dielectric in between, either a high-*k* material or silicon-oxide. In this technology, additional manufacturing process steps are introduced, and as a result there are cost implications.
MOS capacitor, or depletion capacitance utilizes an unused area of the die, as die area always has vacant zones. Therefore, there are no implications on die area, yield etc.
This approach[3] has several significant advantages: the connectivity parasitics between capacitor to load are minimized, as on-die capacitance is relatively evenly distributed all over the circuit. As a result, it has a very high bandwidth in the range of a few GHz. The obtained capacitance value depends on die size and effectiveness of area utilization and for large area dies (400 mm^2) can reach even up to few micro Farads.
These capacitive on-die structures have current leakage property, and have to be considered for static power analysis.

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[2] "Reliability challenges for CPU decoupling MLCC - ResearchGate." https://www.researchgate.net/publication/289371800_Reliability_challenges_for_CPU_decoupling_MLCC. Accessed 17 Dec. 2018.
[3] "Characterization of on die capacitance and silicon measurement ...." https://ieeexplore.ieee.org/document/7111108/. Accessed 14 Nov. 2018.

On-die capacitance availability depends solely on the silicon product design company, and in most cases it is unknown to the system company that it is required by the component vendor to keep the PDN impedance profile below a specific level.

Ultra-Thin Laminates

The ultra-thin core material (< 1mil), also called “embedded capacitance material” (to be distinguished from “embedded capacitor”), has significant advantages of low impedance and low inductance. The material provided by few vendors known for decades for their capacitive material products.

Ultra-thin laminates can replace one or few laminates in PCB stackup, such as the standard core layer which is of 2-4 mils thickness, with distributed capacitance in the range of 0.8-3 nF/in^2 and 4-22 nF/in^2, for standard Dk (4.4) and high Dk (~10) products, respectively. This capacitance is available for a wide frequency performance, and PCB can be manufactured in hybrid stackup, i.e. to include low loss layers for high speed signals and other layers buried distributed capacitance for favor of PDN impedance profile improvements. The topic was covered in the literature[4].

One of these solutions is based on substituting the discrete capacitors components in favor of distributed capacitors based on thin film and ultra-thin film laminates. Once the component balls pitch is strongly decreased and is going to 0.5 mil, the current consumption increases and PDN requirements have to be addressed with less spacing under the vias for decoupling caps, the thin film solution must be considered. The thin core material (< 1mil), also called embedded capacitance material, has significant advantages of low impedance and low inductance. It can replace one or few laminates in PCB stackup, such as the core layer which is of 2-4 mils thickness with distributed capacitance in order of 0.8 nF/in2, with wide frequency performance, and can be manufactured in hybrid stackup. The topic was previously discussed in the literature (TecForum TF9: Thin and Very Thin Laminates for Power Distribution Applications: What Is New in 2004, DesignCon 2004).

Embedded Capacitors

Embedded passive components implementation, particularly embedded capacitors, have been driven and explored in order to improve electrical performance as well as miniaturization trends in mobile and other industries. PDN electrical performance is improved due to electrical proximity, meaning a shorter inductive path, to the load. Therefore, large components like server CPU or network processors with high power delivery requirements can also benefit from this technology[5].

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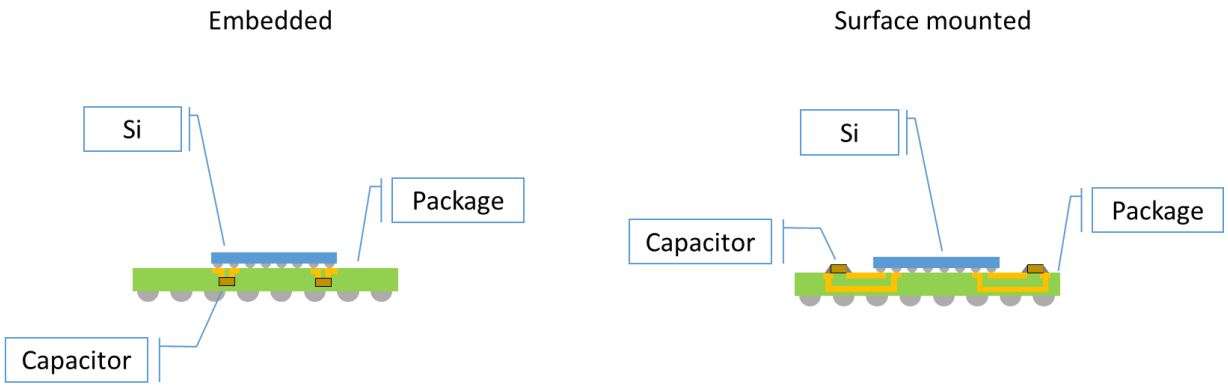
[4] "DesignCon 2004 Thin and Very Thin Laminates for Power Distribution ...." http://www.electrical-integrity.com/Paper_download_files/DC04_TF09.pdf. Accessed 16 Dec. 2018.

[5] "Embedded capacitors in the next generation processor - IEEE Xplore." https://ieeexplore.ieee.org/document/6575731/. Accessed 17 Dec. 2018.



Embedding the large ceramic capacitor into a thick substrate core brings many concerns and issues. First, the coefficient of thermal expansion (CTE) difference of the ceramic capacitor, substrate core, molding polymer, and substrate build-up materials could result in internal stress and induce de-lamination at each interface during standard substrate manufacturing, assembly, and product usage. Therefore, a proper material selection and treatment of its interface are essential. Second, embedded capacitors in the substrate core could influence the warpage of substrate, and this could cause first or second level interconnection failures. The number of embedded capacitors and their location should be carefully decided upon, to balance the substrate warpage and the embeddable capacitor performance. Lastly, the rough surface of ceramic capacitors could act as a starting point for cracks to propagate to substrate core or build-up layers. Visual appearance criteria are therefore more important for embedded capacitors than for surface mounted capacitors.

Case study

In this paper we will examine the use of distributed capacitors based on thin and ultra-thin film laminates for controlling PDN impedance at the MHz to GHz frequency band of fine pitch BGA design, along with several PDN design approaches. The resulting power integrity simulation and PDN lab measurements are presented for the different options. Additional practical product design aspects such as manufacturability and reliability are discussed, and the limitations for this solution are examined as well as its key benefits.

The aim of this work is to adjust the existing PCB design supporting 0.8um BGA devices to the same device with reduced package size of 0.5um BGA pitch. As a result of BGA pitch reduction, the PCB can no longer populate the large amount of small decupling capacitors of the analog rails mounted on print side of the PCB surrounding the BGA.

In order to maintain PI characteristic of the PDN, after careful examination of available decoupling solutions described in the previous section, it was concluded that the best approach was to replace the small decoupling capacitors with distributed capacitance of ultra-thin film laminate by replacing the layers associated with analog PDN with ultra-thin film laminate with high Dk. The original stackup is displayed in figure 8 along with the layers to be changed marked in orange and an indication of the PDN rail associated with each layer of interest. It is worth mentioning that the analog rails accommodate 2 main types of capacitors: 3 100uF capacitors and several 1uF capacitors (and several smaller one as well) on the periphery of the BGA. The layout design of the analog rail on each of the associated PCB layers is presented in figure 9 and figure 10. The design of the analog rails is expected to cause little or no change in the transition process to 0.5um pitch BAG package. Additional investigation is made to examine the effectiveness of distributed capacitance of large area plains such as 1.8v PDN rail and will be discussed later on in this paper.

Original	Stackup	Thickness (mil)	DK Value
L1	0.5oz+plating	2.2	
	PP(1080*1)	2.6	3.97
L2	1oz	1.15	
	Core(2116*1)	5	4.06
L3	0.5oz	0.55	
	PP(2116*1)	3.92	4.06
L4	1oz	1.15	
	Core(2116*1)	5	4.06
L5	0.5oz	0.55	
	PP(2116*1)	3.92	4.06
L6	1oz	1.15	
1v PDN	**Core(1506*1)**	**6**	**3.87**
L7	1oz	1.15	
	PP(2116*1)	3.92	4.07
L8	0.5oz	0.55	
	Core(7628*2)	16	4.42
L9	1oz	1.15	
	PP(2116*1)	3.92	3.97
L10	1oz	1.15	
1v PDN	**Core(106*1)**	**2**	**3.87**
L11	1oz	1.15	
	PP(2116*1)	3.92	3.97
L12	1oz	1.15	
	Core(7628*2)	16	4.42
L13	0.5oz	0.55	
	PP(2116*1)	3.92	4.07
L14	1oz	1.15	
1.8v PDN	**Core(1506*1)**	**6**	**3.87**
L15	1oz	1.15	
	PP(2116*1)	3.92	4.06
L16	0.5oz	0.55	
	Core(2116*1)	5	4.06
L17	1oz	1.15	
	PP(2116*1)	3.92	4.06
L18	0.5oz	0.55	
	Core(2116*1)	5	4.06
L19	1oz	1.15	
	PP(1080*1)	2.6	3.97
L20	0.5oz+plating	2.2	

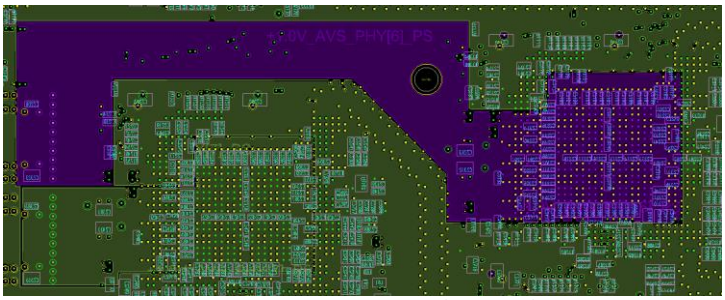


Figure 1: Micromodel describing the behavior as a function of system variables for the

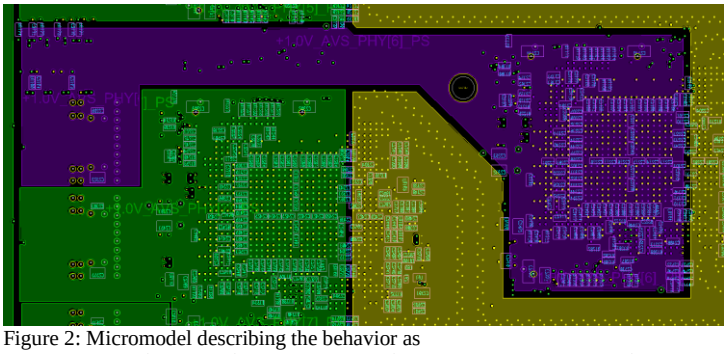


Figure 2: Micromodel describing the behavior as

Figure 3: Micromodel describing the behavior as a function of system variables for the magnitude response frequency

PDN Measurement

In order to characterize the PDN of interest, as observed form the BGA, and cover the required frequency band 1kHz–3GHz with adequate accuracy with respect to the measured impedance levels of the design, two types of measurements were conducted, using the shunt thru measurement technique for each of the two types. To cove the lower frequency band, 1KHz-30MHz, a gain-phase measurement was performed with a response thru calibration. For coverage of the higher frequency band, 10MHz-3GHz, a standard SOLT calibration was performed for the VNA ports. In order to maximize the accuracy of the measurement, the double side probing technique was implemented with GSG microprobes landing directly on top of the PTH vias to reduce the parasitic xtalk between the probes and minimize the parasitic inductance that is not accounted for in the calibration process. The pitch of the GSG probes was selected as the minimum pitch allowing the above procedure, and a standard ISS calibration substrate was used for the various calibration procedures. The measurement setup is shown in fig11 .

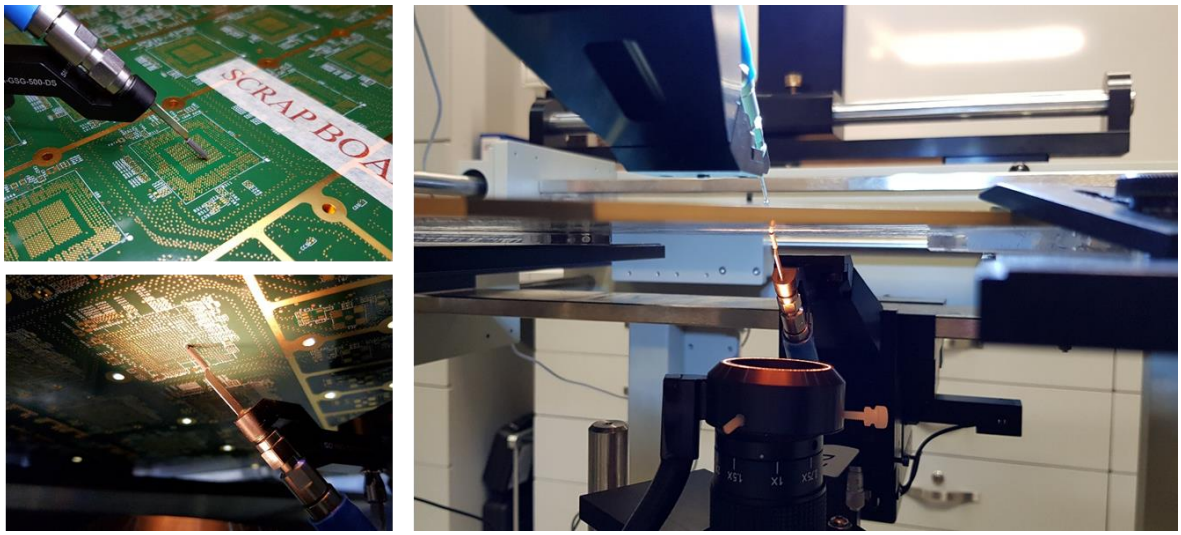


Figure 4: Micromodel describing the behavior as

Several system configurations were examined:

1. Bare PCB
2. All capacitors populated
3. 100uF capacitors removed
4. Bare PCB and 100uF capacitors only (no small capacitors)

Both of the two measurement types, for low and high frequency, were executed for each of the configurations, and the measurements results for the low and high frequency bands are presented in figures 15 and 16 respectively. From analyzing the low frequency PDN measurements displayed in fig 15 it can be clearly concluded that the overall PDN impedance profile is dominated by 100uF capacitors up to ~3 MHz , and by the smaller 1uF capacitors above this frequency. The high frequency band measurement results displayed in fig 16 show that the smaller 1uF caps dominate the overall PDN profile up to

1GHz. Above the 1GHz frequency the plane capacitance dictates the PDN profile , however its impact is noticeable already at the 100MHz area.

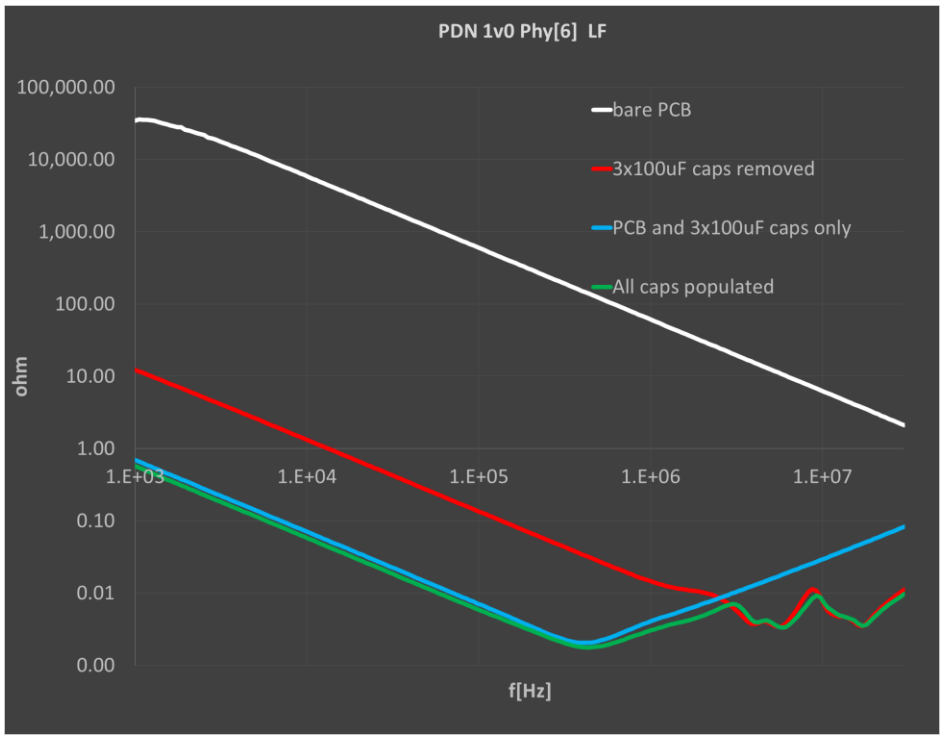


Figure 5: Micromodel describing the behavior as

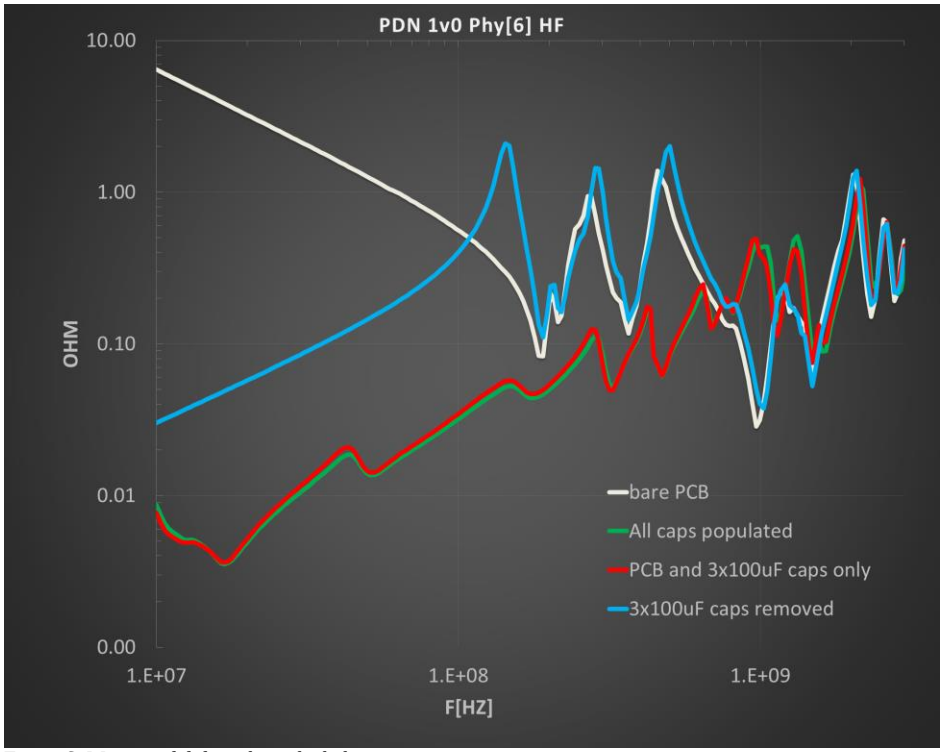


Figure 6: Micromodel describing the behavior as

Feasibility study

From an observation of the high frequency results, it can be clearly seen that if improved by two orders of magnitude plane capacitance could dominate the overall impedance profile starting at ~10 MHz range and along with the 100uF capacitors impact on PDN impedance in the lower frequency range will eliminate the need for mounting multiple 1uF capacitors in order to achieve similar PDN performance, achieving impedance levels similar to existing design as demonstrated in figure 17.

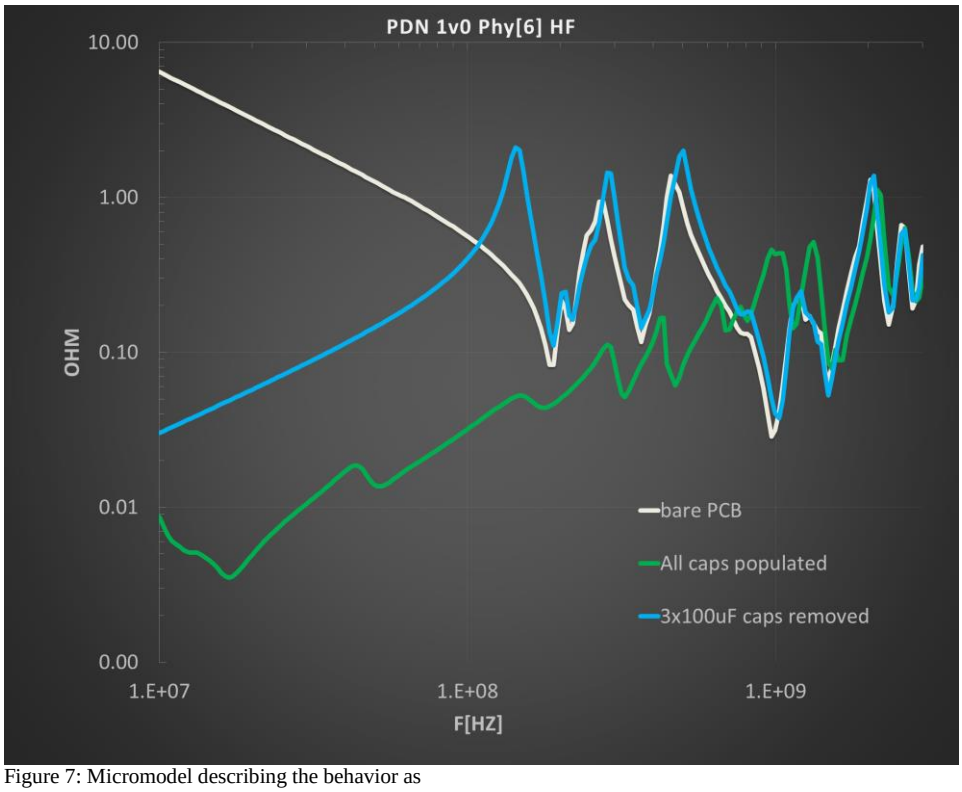


Figure 7: Micromodel describing the behavior as

To achieve such an effect without significantly changing the PDN layout, two ultra thin film high Dk laminates were initially examined: MC8TM and MC8T. The high Dk and low thickness of the dielectric produces the maximum capacitance per area for these two types of thin film laminates, as shown in table 2 below.

Properties	Test Method	High Dk Products				
		MC12TM	MC8TM	MC8T	MC12ST	MC12LD
Dielectric Thickness, µm	IPC or others	12	8	8	12	12
Cp @1 MHz, nF/in² (pF/cm²)	Nominal	4.2 (650)	7.1 (1100)	22 (3400)	10.5 (1630)	4.32 (670)
Dk (Dielectric Constant) @ 1 MHz/1 GHz	IPC TM-650 2.5.5.2	10.0/ 9.5	10.5/ 10.0	30.0/ 25.0	25.1 @ 1 MHz	7.3/ 7.4
Df (Loss Tangent) @1 MHz/1 GHz	IPC TM-650 2.5.5.2	0.015/ 0.020	0.020/ 0.021	0.025/ 0.031	0.005 @ 1 MHz	*0.0020/ 0.0018

Figure 8: Micromodel describing the behavior as

Verifying PDN Simulation Correlation to measured data

The first step of the investigation work in order to establish confidence in the accuracy of the simulation-based prediction of the PDN impedance profile was to establish a correlation between the measured PDN impedance results and the simulation data. The larger 1.8v plane was selected for this purpose and the simulated results vs both low and high frequency measurements results are shown in fig20, displaying a good agreement between the three data types, and enabling further investigation with sufficient confidence in simulation-based prediction. Although some discrepancies are found, they are mostly associated with the deviation of actual capacitors characteristics from the simulation models, and are insignificant considering the purpose of our analysis.

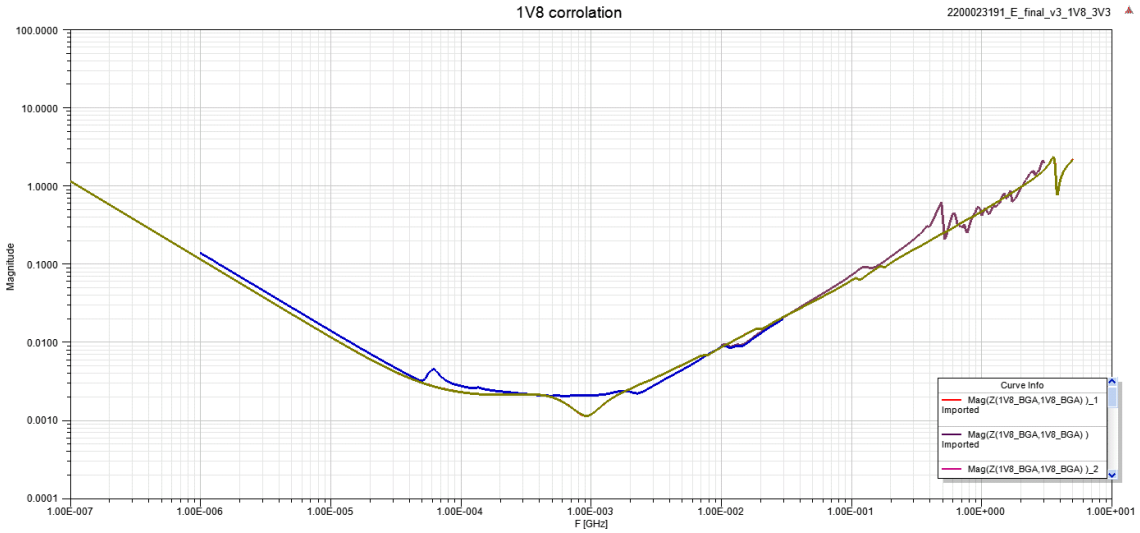


Figure 9: Micromodel describing the behavior as

Estimation of capacitors impact on PDN impedance profile

Due to the fact that at lower frequencies, up to 100MHz, the impedance profile of the analog rails is dominated by the various capacitors, the impact of each capacitor type on the PDN impedance profile (excluding the mounting inductance) is examined and displayed in fig 21.

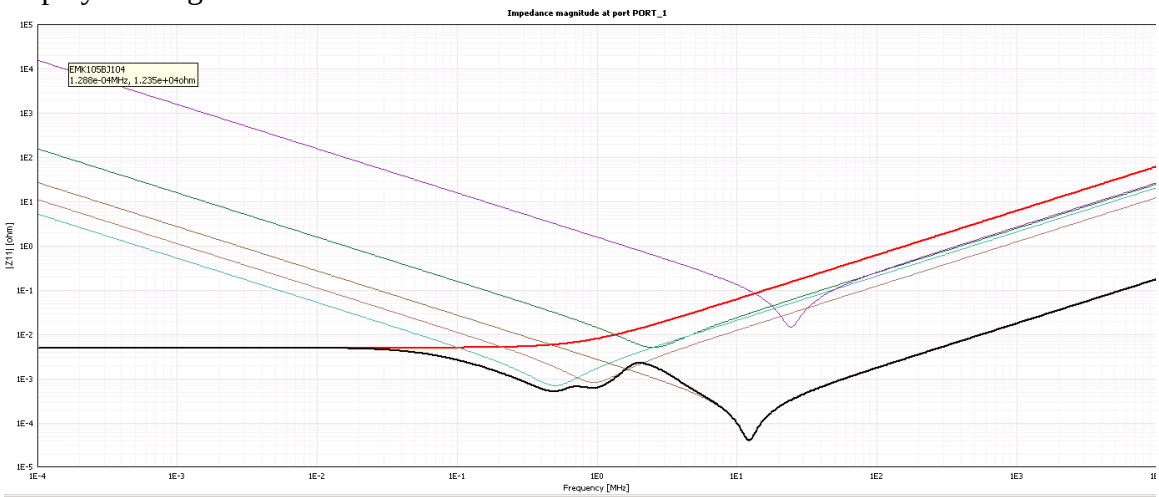


Figure 10: Micromodel describing the behavior as

The individual capacitance type contribution is compared to the measured impedance profile and displayed in figure 22, showing a good agreement of the major capacitors types used in the design, 100uF and 1uF, further validating the accuracy of the capacitors models used for the simulation.

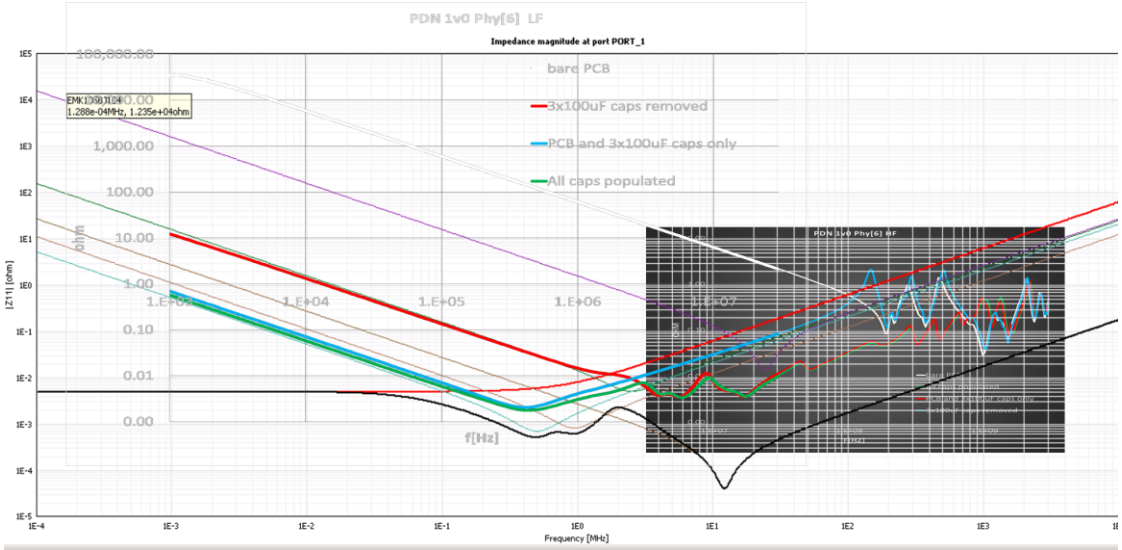


Figure 11: Micromodel describing the behavior as(need to replace fig)

The impact of ultra-thin laminates on PDN impedance

The impact of replacing the selected FR4 layers with MC8TM laminate on analog PDN impedance is examined in this section. The MC8TM core has a dialectric thickness of 0.3mil and Dk value of 10 providing 1.1 nF/cm^2. The impact on the analog plane impedance of bare PCB is presented in fig 23, demonstrating a reduction of the plane impedance by an order of magnitude at frequencies above ~100MHz. The effect on the analog rain without removing any of the existing capacitors is presented in fig 24 displaying a noticeable impedance reduction starting from 200MHz and a significant improvement at GHz region.

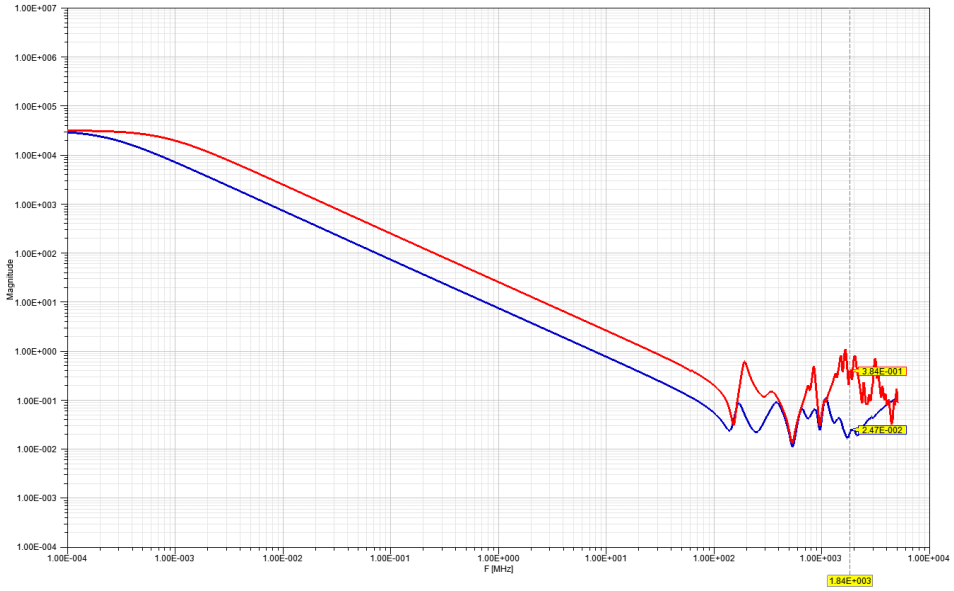


Figure 12: Micromodel describing the behavior as

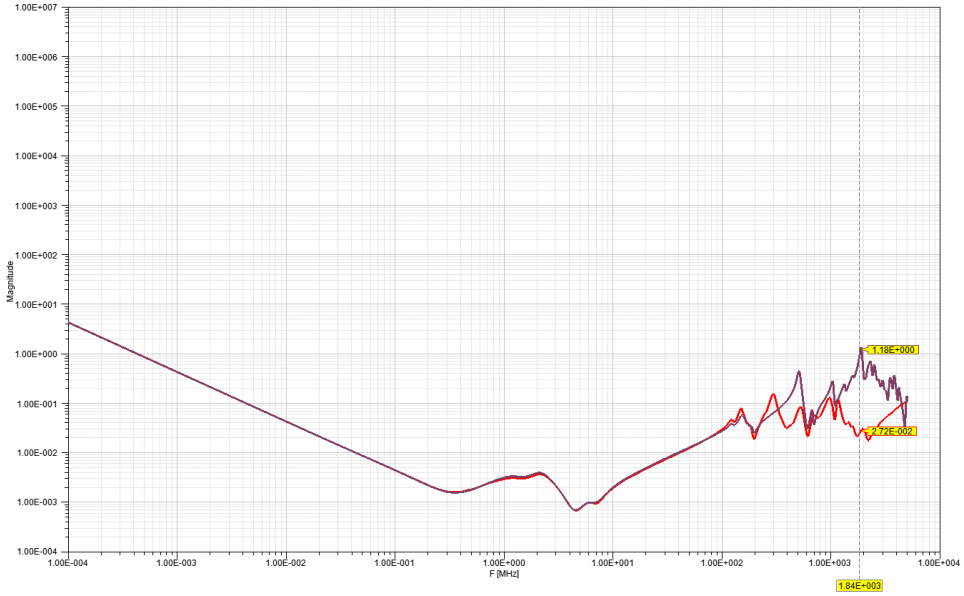


Figure 13: Micromodel describing the behavior as

Power plane size impact on PDN impedance

Next we extended the analog power plane area at the top thin core laminate layer (L6) by 3cm^2 in order to increase the plane capacitance .The result of adding 3cm^2 to power plane area is shown in figure 25, demonstrating a further improvement in overall PDN impedance and a significant impedance reduction already at 150MHz and above .

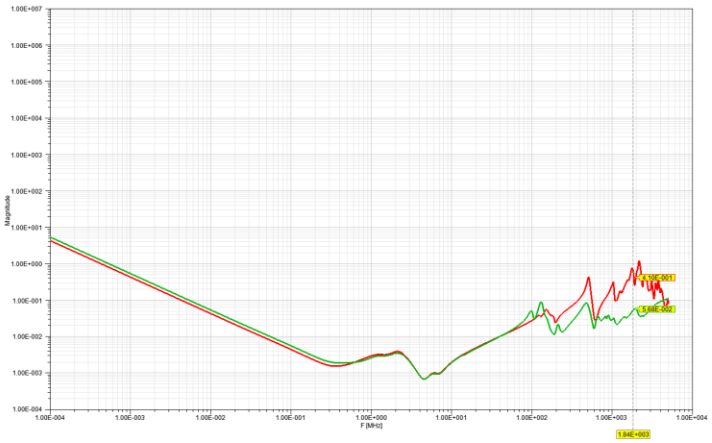


Figure 14: Micromodel describing the behavior as

The power plane proximity to top layer-The impact of plane order on PDN impedance

Next we assessed the effect of the power plane order in a given stack-up on the analog rail impedance. The proximity to the top plane and eventually the Si has a major impact on the parasitic inductance of the via connecting the plane to the BGA, due to the longer path required for reaching the plane inside the PCB stuck-up. Although this effect could be mitigated by increasing the number of vias, this approach is not always feasible, due to other design restrictions such as pin count and BGA size, and might have a negative effect on other power planes. The via inductance in practice has a significant effect in comparison to ESL values of decoupling capacitors. The effect of changing the top analog plane form L6 in the stack-up to the lower L15 is demonstrated in fig 26, showing a negative impact on PDN impedance and a significant effect at the GHz range.

Figure 15: Micromodel describing the behavior as

Higher thin laminate Dk effect on PDN impedance

The impact of the phenomena mentioned above could be mitigated by increasing the Dk value of the plane, thus increasing the plane capacitance per unit area. The MC8T provides such charaterestics and has a Dk value of 30, while maintaining the same dielectric thickness of 0.3um. The effect of increasing the Dk value to 30 on the plane impedance is presented in figure 27, which displays a significant improvment over the previous case from 80MHz and an improvment by an order of magnitude in the GHz area.

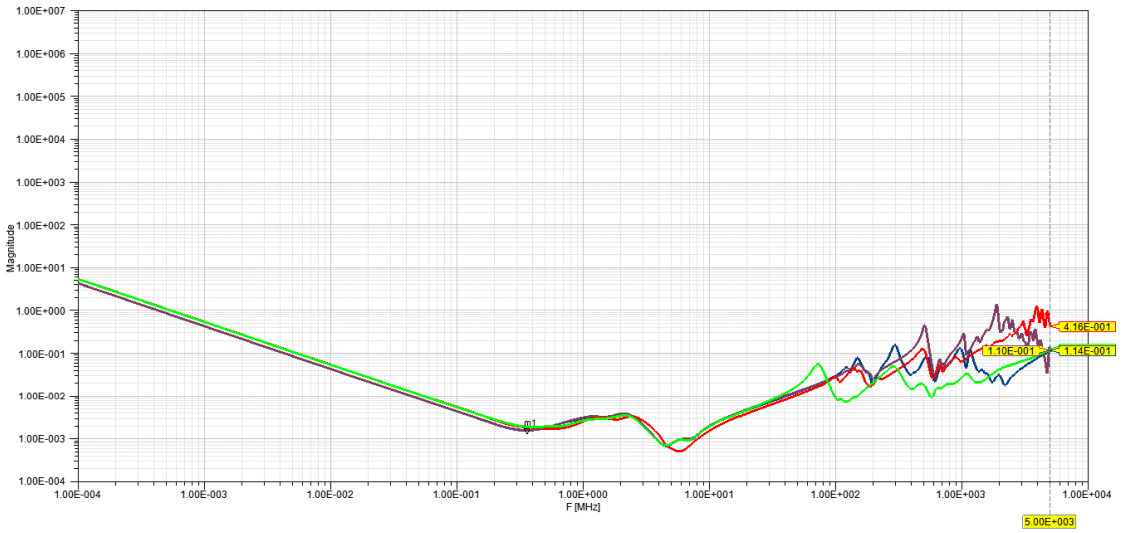


Figure 16: Micromodel describing the behavior as

Manufacturing Considerations for Ultra-Thin laminates PCB designs

As it turns out, industry experience with MC8TM is extremely limited. The few engagements that have been made by PCB manufacturers have been experimental only and were not successful as manufacturing and reliability issues have been cited --- so much so that even the most experienced facility has no interest in taking additional orders in any capacity.

There is more experience across the industry with MC12TM and even more with MC24TM. MC24TM capability is fairly routine and there should be no issues in getting boards manufactured. MC12TM capability is more limited and there are important manufacturing guidelines associated with its use, but some top facilities should be able to provide boards with this technology.

Going with ultra-thin laminates is a bumpy road. It seems that most PCB manufacturers of this technology suffer from lack of experience working with such unique stack up combinations.
In addition, for a unique stackup combination, a UL (safety and compliance standards) certification issues are to be addressed.
Additional to the above complexity and due to the lack of knowledge, PCB manufacturers are required to build support samples and carry out fine tuning for mass production, which translates to high NPI cost.
One of the big concerns was etching these ultra-thin laminates. The “normal” application per the material vendor is to use the BC laminates as a big plane of a single rail, without having “traces” etching on the BC laminate. In our case study we examined a high runner PCB which had multi-rails over the power plane. This forces the manufacturer to use unique etching processes (similar to flex PCB technology). When considering such a unique process for etching for large PCBs, it directly affects the PCB cost, resulting in a much higher one than in the standard etching process.
Another point to consider is the lamination process. Some of the BC materials require a sequential PCB processing core, while the others require both sides processing core. The difference is related to the core thickness, as can be seen at the table below:

Properties	Test Method	High Dk Products				
		MC12TM	MC8TM	MC8T	MC12ST	MC12LD
Dielectric Thickness, µm	IPC or others	12	8	8	12	12
Cp @1 MHz, nF/in² (pF/cm²)	Nominal	4.2 (650)	7.1 (1100)	22 (3400)	10.5 (1630)	4.32 (670)
Dk (Dielectric Constant) @ 1 MHz/1 GHz	IPC TM-650 2.5.5.2	10.0/ 9.5	10.5/ 10.0	30.0/ 25.0	25.1 @ 1 MHz	7.3/ 7.4
Df (Loss Tangent) @1 MHz/1 GHz	IPC TM-650 2.5.5.2	0.015/ 0.020	0.020/ 0.021	0.025/ 0.031	0.005 @ 1 MHz	*0.0020/ 0.0018
Peel Strength, lbs/ linear in.	IPC TM-650 2.4.8	5	5	4	4	>4
Dielectric Strength, kV/mil	IPC TM-650 2.5.6.2	5	4	1	2	2
Tensile Strength, MPa (kpsi)	ASTM D-882A	153 (22.2)	127 (18.4)	NA	NA	NA
Elongation, %	ASTM D-882A	31.4	14	NA	NA	NA
CTE, ppm/°C, x-y (40-200 °C), TMA	TMA	28	22	17 (α1) 42 (α2)	32 (α1) 97 (α2)	55
Tg, °C	DMA	189	191	191	170	170
Dielectric Withstanding Voltage (Hi-Pot test)	IPC TM-650 2.5.7.2	PASS (500V)	PASS (250V)	PASS (100V)	TBD	TBD
Thermal Stress (20 Sec Float @288 °C), Times	-	>10	>10	>6	>6	>10
THB, 85 °C/85% RH/dc bias	1000hr	PASS	PASS	PASS	TBD	TBD
Flammability/Temp Rating	UL	V0 130°C	V0 130°C	V0 130°C	TBD	TBD
PWB Processing	-	Both sides	Both sides	Sequential	Sequential	Sequential

Note: This chart provides typical values for ***FaradFlex***® products. For a full list of our products please contact us.

***Low loss material**

Figure 17: Micromodel describing the behavior as

As seen above, any product ended with –T requires Sequential PWB Processing instead of both Side Processing. This will increase the lamination process difficulties especially on such core.

BC core PCB process and their stack up requirement are shown below:

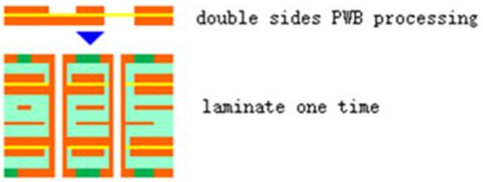
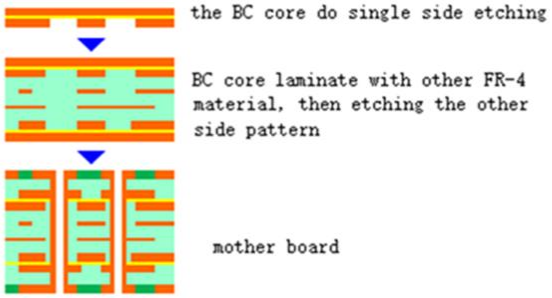
PWB Processing	graphical	Requirement of the PCB layup
both sides		Just keep the layup is symmetric, the BC core number could be odd or even.
Sequential		1)The number of the BC core could only be even. 2)The layup should be symmetric, especially the BC core. 3)If the BC core number is 2x， then laminating time equal to x+1.

Figure 18: Micromodel describing the behavior as

BC core cost comparison vs. regular FR-4 design presented in table 4 :

NO.	Item	NPI 10PC U/P	MASS PRODUCTION U/P	LEAD TIME	NRE	Material Type
1	Stack-up #1	3X	3X	1.5X	2X	FR-4 & Ultra thin core
2	Stack-up #2	3X	2X	1.5X	2X	FR-4 & Thin core
3	Stack-up #3 (REF)	X	X	X	X	FR-4

Figure 19: Micromodel describing the behavior as

The end result

Despite our efforts to convince manufacturers and the potential benefits the ultra-thin cold have on our design, the manufacturing obstacles and technology reediness prevented us from adopting significant changes to our design. The original and requested stackup is displayed below along with the proposed stuck-up from manufacturer.

Original	Stackup	Thickness (mil)	DK Value
L1	0.5oz+plating	2.2	
	PP(1080*1)	2.6	3.97
L2	1oz	1.15	
	Core(2116*1)	5	4.06
L3	0.5oz	0.55	
	PP(2116*1)	3.92	4.06
L4	1oz	1.15	
	Core(2116*1)	5	4.06
L5	0.5oz	0.55	
	PP(2116*1)	3.92	4.06
L6	1oz	1.15	
1v PDN	**Core(1506*1)**	**6**	**3.87**
L7	1oz	1.15	
	PP(2116*1)	3.92	4.07
L8	0.5oz	0.55	
	Core(7628*2)	16	4.42
L9	1oz	1.15	
	PP(2116*1)	3.92	3.97
L10	1oz	1.15	
1v PDN	**Core(106*1)**	**2**	**3.87**
L11	1oz	1.15	
	PP(2116*1)	3.92	3.97
L12	1oz	1.15	
	Core(7628*2)	16	4.42
L13	0.5oz	0.55	
	PP(2116*1)	3.92	4.07
L14	1oz	1.15	
1.8v PDN	**Core(1506*1)**	**6**	**3.87**
L15	1oz	1.15	
	PP(2116*1)	3.92	4.06
L16	0.5oz	0.55	
	Core(2116*1)	5	4.06
L17	1oz	1.15	
	PP(2116*1)	3.92	4.06
L18	0.5oz	0.55	
	Core(2116*1)	5	4.06
L19	1oz	1.15	
	PP(1080*1)	2.6	3.97
L20	0.5oz+plating	2.2	

Requested	Stackup	Thickness (mil)	DK Value
L1	0.5oz+plating	2.2	
	PP(1080_RC68%*1)	2.955	3.97
L2	1oz	1.2	
	Core(2116*1)	5	4.06
L3	0.5oz	0.6	
	PP(2116_RC57%*1)	4.556	4.06
L4	1oz	1.2	
	Core(2116*1)	5	4.06
L5	0.5oz	0.6	
	PP(2116_RC57%*1)	4.556	4.06
L6	1oz	1.2	
1v PDN	**Core(MC8TM)**	**0.315**	**10**
L7	1oz	1.2	
	PP(2313_RC59%*1)	3.532	4.07
L8	0.5oz	0.6	
	Core(7628*2)	16	4.42
L9	1oz	1.2	
	PP(2116_RC57%*1 + 2313_RC5	8.638	4.06
L10	1oz	1.2	
1v PDN	**Core(MC8TM)**	**0.315**	**10**
L11	1oz	1.2	
	PP(2313_RC59%*1 + 2116_RC5	8.638	4.06
L12	1oz	0.6	
	Core(7628*2)	16	4.42
L13	0.5oz	1.2	
	PP(2313_RC59%*1)	3.532	4.07
L14	1oz	1.2	
1.8v PDN	**Core(MC8TM)**	**0.315**	**10**
L15	1oz	1.2	
	PP(2116_RC57%*1)	4.556	4.06
L16	0.5oz	0.6	
	Core(2116*1)	5	4.06
L17	1oz	1.2	
	PP(2116_RC57%*1)	4.556	4.06
L18	0.5oz	0.6	
	Core(2116*1)	5	4.06
L19	1oz	1.2	
	PP(1080_RC68%*1)	2.955	3.97
L20	0.5oz+plating	2.2	

Proposed	Stackup	Thickness (mil)	DK Value
L1	0.5oz+plating	2.2	
	PP(1080_RC68%*1)	2.955	3.97
L2	1oz	1.2	
	Core(2116*1)	5	4.06
L3	0.5oz	0.6	
	PP(2116_RC57%*1)	4.556	4.06
L4	1oz	1.2	
	Core(2116*1)	5	4.06
L5	0.5oz	0.6	
	PP(2116_RC57%*1)	4.556	4.06
L6	1oz	1.2	
1v PDN	**Core(106*1)**	**2**	**3.87**
L7	1oz	1.2	
	PP(2313_RC59%*1)	3.532	4.07
L8	0.5oz	0.6	
	Core(7628*2)	16	4.42
L9	1oz	1.2	
	PP(1080_RC68%*2)	5.783	3.97
L10	1oz	1.2	
1v PDN	**Core(106*1)**	**2**	**3.87**
L11	1oz	1.2	
	PP(1080_RC68%*2)	5.783	3.97
L12	1oz	0.6	
	Core(7628*2)	16	4.42
L13	0.5oz	1.2	
	PP(2313_RC59%*1)	3.532	4.07
L14	1oz	1.2	
1.8v PDN	**Core(106*1)**	**2**	**3.87**
L15	1oz	1.2	
	PP(2116_RC57%*1)	4.556	4.06
L16	0.5oz	0.6	
	Core(2116*1)	5	4.06
L17	1oz	1.2	
	PP(2116_RC57%*1)	4.556	4.06
L18	0.5oz	0.6	
	Core(2116*1)	5	4.06
L19	1oz	1.2	
	PP(1080_RC68%*1)	2.955	3.97
L20	0.5oz+plating	2.2	

Figure 20: Micromodel describing the behavior as

Conclusion

In this paper we examined the use of distributed capacitors based on thin and ultra-thin film laminates for controlling PDN impedance at the MHz to GHz frequency band of fine pitch BGA design, along with several other approaches, such as Si based capacitors and distributed capacitors of standard laminates. The resulting power integrity simulation and PDN lab measurements were presented for the different options. Additional practical product design aspects such as manufacturability and reliability were discussed, and the limitations for each solution were examined as well as its key benefits. Some of the key benefits are listed below along whit some potential issues one might discover.

BC Laminate PROS & CONS:

- Reduction of SMD capacitors which increases the overall design reliability
- EMI from the PCB can be reduced
- Power rail plane impedance can be reduced
- Makes the design easier to route, due to a lack of vias for the capacitors
- Makes the power rails plane much more efficient for current delivery due to lack of via holes
- Possible cost saving. Reduces the number of capacitors and assembly (might reduce PCB size), but increases the bare PCB cost.
- This technology is not new but not commonly used, hence requires FAB qualification
- BC core sometimes requires UL approval for a unique stack-up
- Thinner Power Distribution Planes are required for improved impedance performance at high frequency
- New substrates have demonstrated excellent electrical performance and physical properties.
- They are compatible with PCB processing; a truly “drop in” material.
- Materials are commercially available from many fabricators
- Substrates filled with ferroelectric particles have better performance, but result in higher cost PCBs
- Green and lead free solution

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