DesignCon 2019

Link Channel Mode Conversion and its Impact on 112Gbps PAM4 Systems

Geoff Zhang, Xilinx Inc. geoff.zhang@xilinx.com

Jason Chan, Cadence Design Systems Inc. cjason@cadence.com

Hong Ahn, Xilinx Inc. hongsika@xilinx.com

Min Huang, Xilinx Inc. mhuang@xilinx.com

Abstract

As data rates increase to 56G based PAM4 modulation scheme and beyond, mode conversion becomes non-negligible as its impact is comparable to or even larger than other noise impairments, such as crosstalk. A simulation approach is proposed such that the mode conversion impact on the system margin is included, in contrast to the conventional method in which only pure differential signaling is modeled as facilitated by perfectly balanced and de-skewed transmit signals. Necessary changes to IBIS-AMI standards are proposed such that inclusion of mode conversion is optionally included. Detailed examples are provided to show the impact of mode conversion on link performance margin degradation.

The key takeaways from this paper are the following: understand causes of mode conversion, manifestation of common mode and how to include them in existing simulation platforms. Necessary changes to IBIS-AMI standards to incorporate common mode TX components and mode conversion effects are also proposed for the industry. The paper will provide detailed examples.

Authors Biography

Geoff Zhang received his Ph.D. in 1997 in microwave engineering and signal processing from Iowa State University, Ames, Iowa. He joined Xilinx Inc. in June, 2013. Geoff is currently Distinguished Engineer and Supervisor, in transceiver architecture and modeling under SerDes Technology Group. Prior to joining Xilinx he has employment experiences with HiSilicon, Huawei Technologies, LSI, Agere Systems, Lucent Technologies, and Texas Instruments. His current interest is in transceiver architecture modeling and system level end-to-end simulation, both electrical and optical.

Jason Chan received his MSEE degree in Applied Electromagnetics from the University of New Hampshire in 2004. He is currently working as a Senior Principal Product Engineer for Cadence Design Systems where his primary responsibilities reside in customer engagement & product engineering support for the Sigrity 3DEM Field Solver platform. Prior to joining Cadence, he previously served at Samtec, Invecas, LSI, Huawei Technologies, and Amphenol-TCS. His professional interests reside in high speed system-level architectural design/simulation and applied electrodynamics.

Hong Ahn received his Master degree in Electrical Engineering from Korea University, Seoul, Korea in 1995. He is currently working in SerDes Technology Group in Xilinx. His current interests are transceiver application, transceiver validation, signal integrity and system level architecture with transceiver. Prior to joining Xilinx, he worked with NetLogic, Broadcom and LGIC.

Min Huang received her Master in 2013 in electrical engineering from University of California, Los Angeles. Min joined Xilinx Inc. since 2015 in transceiver architecture and modeling team under SerDes Technology Group. Prior to that, she was working on SerDes architecture at LSI. Her current interest is high speed IO architecture modeling and system level simulations.

1. Introduction

As data rates increase to 56G and beyond, link performance margins decrease. PAM4 signaling, which must be utilized at such speeds for the given system architectures that translate to certain dB loss which is too much for NRZ to handle, even with FEC, poses significant challenges in terms of link margin budgets as it suffers from inherent SNR degradation and highly diminished jitter margins. To accurately assess link performance margins, simulation accuracy becomes even more critical. However, the caveat is that link simulations are only as accurate as the models that are used for both active and passive components.

A passive linear link system is usually represented by s-parameters. Traditionally end-toend link simulations only involve perfectly driven differential signals where the SDD portion of the s-parameter matrices of the system, or differential-to-differential signal transmission, is considered for both THRU and crosstalk paths. Even if it is modeled accurately, mode converted components including SDC, SCC, and SCD are typically ignored. In addition, common mode generation at the TX package output is ignored where TX models typically assume perfectly balanced differential signals with zero skew. This practice is not a problem or at worst marginally inaccurate in the past, but it is now a problem we must cope with. Though some proprietary tools can include mode conversion effects, no such provision is available generally among commercial EDA tools, nor in the most widely adopted IBIS-AMI modeling approach.

In this paper we will first cover the potential causes of mode conversion, specifically SDC. A brief qualitative discussion on the sources of mode conversion in the passive channel, including non-ideal fabrication effects of skew tolerances and differential balance, are covered.

The impact on link performance margin is illustrated intuitively via examples. Inclusion of SDC mode conversion modeling in conventional simulators, which currently includes only SDD components, is shown in detail. Subsequently, necessary changes to the IBIS-AMI standard are proposed to better capture SDC effects within the passive channel and imbalanced TX outputs.

Finally, the paper will provide detailed examples to show the adverse effects of mode conversion on reducing the link margin. The reader will walk away with the understanding of the importance in controlling mode conversion, and in modeling it in end-to-end link simulations and analyses.

2. Mode Conversion in High-Speed Serial Channels

Mode-conversion effects are generally decomposed into two domains: temporal imbalance and physical imbalance. Let us review the physical basis of each type of mode-conversion as follows:

A. Temporal Imbalance

The first such domain is temporal-based, predicated on imperfect length-matching of the P/N nets within a differential pair that is classically known as intra-pair skew. Sources of intra-pair skew include:

- Asymmetric electrical propagation delays due to inhomogeneities in PCB substrates (e.g. fibre weave effects, air voids,, etc)
- Asymmetric propagation delays due to imperfections of P/N physical routing
- PCB/package fabrication tolerances that could contribute to imperfect physical/electrical balance (e.g. over-etch, air voids due to slight CTE mismatches, etc).

Length mis-matching within a differential pair can lead to misaligned propagation delays between the P/N components, thereby leading to the ubiquitous "suckout" resonance phenomenon owing to phase cancellation between the P/N channels. This suckout has immediate implications in terms of insertion loss, especially if the suckout frequency is located near the Nyquist frequency of interest. Another consequence is the manifestation of SDC mode conversion where differential mode energy is partially lost to the common mode due to misaligned propagation delays.

B. Physical Imbalance

The second such mode conversion domain pertains to physical imbalance, i.e. imperfect impedance balance between P/N. All physical systems will always have some degree of inherent imbalance due to fabrication tolerances, even if prop delay balances are somehow zeroed out. Such imbalances are inherent in all devices, IC packages, PCB's and interconnects.

Although high speed channel designs nominally assume perfect balance, cumulative effects of fabrication tolerances throughout the entire system will contribute to overall mode conversion. Unlike temporal imbalance, the ill-effects of physical imbalance are not as ostensibly apparent – diff pair channels that are very well de-skewed could possibly have elevated levels of mode conversion, without the suckout effect, due to aggregate physical imbalances in the channel. From a more global perspective, the entire system is replete of such physical imbalances including:

- Substrate and etching tolerances in PCB's and IC packages
- Imbalanced pinouts in open pin-field connectors

- Imbalanced GND configurations in IC package ball and bump grids
- Inadvertent impedance imbalances (e.g. narrow routing channels with asymmetric GND cutouts, asymmetric co-planar GNDs in IC package, etc.)
- Imbalanced source terminations at the TX/RX buffers.

What are the overall consequences considering the aggregate effects of both temporal and physical imbalances? For the sake of simplicity, suppose that we have a simple 100 ohm diff pair trace with imbalanced line widths of 5.5 & 5.0 mils and line spacing of 8 mils. Precision modelling of physical imbalance contributions from devices, IC packages, PCB's, and interconnects are well beyond the scope of this study; for simplicity sake, we shall approximately emulate aggregate physical imbalance, let us consider three skewed channel scenarios: 0 ps skew, 5ps skew, and10ps skew, which we will label as "RC-0", "RC-5", and "RC-10", respectively.

The corresponding SDD21 and SDC21 s-parameters (note: SCD21 / SDC21 are symmetric) are depicted in Figure 1. For the RC-0 case, observe that the SDD21 insertion loss is free of any suckout resonances out to 100 GHz. This is aligned with our expectations as no temporal imbalance, i.e. skew, is introduced to this channel. However, just because the channel is completely de-skewed does not mean that the channel is free of mode conversion.

As shown in the SDC21 plot, RC-0 still demonstrates finite amounts of mode conversion due to the presence of physical imbalance. Implications of the finite SDC21 in the RC-0 case will be shown later. Cases RC-5 and RC-10 clearly demonstrates the presence of suckouts in the SDD21 spectra. As skew values increase, the suck-out frequency reduces while SDC21 increases in the frequency range of interest. The bottom line is that the addition of temporal imbalance on top of the already-present physical imbalance will only exacerbate aggregate SDC mode conversion. Implications and consequences of the aggregate mode conversion contributions for 112Gbps PAM4 signaling will be shown in subsequent sections.



Figure 1. SDD21 and SDC21 for the three channels

3. Modeling with Mode Conversion

The conventional simulation topology for a THRU channel is shown in Figure 2. Although crosstalk is commonly included in high speed serial channel analyses, it is not considered in this analysis. Note that the topology shown in Figure 2 is representative of most IBIS-AMI channel simulation environments where pure differential mode is only considered to capture the impulse response properties of the entire channel. As demonstrated in the previous section, SDD21 will only capture temporal imbalances of the channel while SDC mode conversion effects are not considered in the THRU channel.



Figure 2. Conventional THRU channel modeling for SDD21

A. Proposed Topology to Include Mode Conversion Effects

To include mode conversion effects, specifically SDC, we would need to somehow incorporate the mode conversion properties of the channel in question into the IBIS-AMI modeling topology while using the same transmitter. A modified modeling topology in Figure 3 is proposed where SCD/SDC mode conversion effects, sourced from the same TX, is summed with the SDD channel as an equivalent noise source at the RX. Note that the Sxx21tx capture aggregate effects of both device and package.



Figure 3. Modified THRU channel modeling for both SDD21 and SDC21

The physical basis for casting the SCD/SDC channel as an equivalent noise source is as follows. First, as previously proposed in reference [1], there is sufficient complexity in the interconnect such that it is possible for signals to undergo multiple mode conversion cycles within the THRU channel. The differential TX component would lose some energy to the common mode (SCD) where the induced common mode would then mode-convert back to the differential mode (SDC). The subsequent SCD \rightarrow SDC mode-conversion cycle would lead to a distorted differential mode component at the RX input that we could approximate as <u>Self-Generated SDC noise</u>. This conversion cycle is mathematically equivalent to cascading SCD and SDC transfer functions in the frequency domain. Multiplying two transfer functions with very low magnitudes results in a net

transfer function with even lower magnitude. Also, the SCD and SDC magnitudes scale with insertion loss, thus high frequency self-generated noise magnitudes are expected to be low enough such that Self-Generated SDC noise can be safely neglected from a modelling perspective.

Secondly, hardware measurement studies have shown that some amount of commonmode energy is embedded in the TX output of the package. In such a scenario, common mode energy is directly sourced from the TX output of the device package. Consequently, this will lead to direct common-mode to differential (SDC) modeconverted noise, which shall be referred to as <u>TX-sourced SDC noise</u>. TX-sourced SDC noise is much more significant than Self-Generated SDC noise as it is scaled by a single SDC transfer function in conjunction with a driven common-mode source from the TX.

Hardware-correlated TX models that include both differential and common mode components represent the worst-case scenario as mode-converted noise is primarily driven by **TX-Sourced SDC Noise**. Implementation of the worst-case scenario in an IBIS-AMI EDA environment is proposed in the following sub-section.

B. Implementation of SDC Mode-Converted Noise in EDA Tools

Commercial EDA tools for IBIS-AMI model simulations currently do not support the use of SDC terms. As previously mentioned, the current IBIS-AMI standard considers only pure differential mode to capture the impulse response properties of the entire channel. To facilitate the inclusion of SDC mode-conversion terms in IBIS-AMI simulations, some manipulations of the THRU channel s-parameter file is necessary. Moreover, a new .dll for the *AMI_GetWave* function is also required to support transmitted common-mode waveforms for the TX; details on incorporating common-mode waveforms into the AMI_GetWave function is beyond the scope of this discussion.

To understand how this is accomplished, we need to understand how single-ended sparameter measurements are converted to mixed mode. In Figure 4 the port maps for single-ended and mixed mode configurations are defined.



Figure 4. Port map definitions for single-ended and mixed mode

The conversion from single-ended s-parameter file to mixed mode s-parameter file is represented by Eq. (1):

$$S^{mm} = M \cdot S^{se} \cdot M^{-1}$$
 Eq. (1)

Note that S^{se} is the original single-ended matrix, S^{mm} is the mixed-mode matrix and transformation matrices M and M⁻¹ are specified in Eq. (2)

$$M = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix}$$
$$M^{-1} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ -1 & 0 & 1 & 0 \\ 0 & -1 & 0 & 1 \end{bmatrix}$$
Eq. (2)

From Eq. (1) and Eq. (2) it is straightforward to obtain the mixed mode s-parameters for SDD and SDC, as respectively expressed in Eq. (3) and Eq. (4).

$$S_{DD11} = (S_{11} - S_{31} - S_{13} + S_{33})/2$$

$$S_{DD12} = (S_{12} - S_{32} - S_{14} + S_{34})/2$$

$$S_{DD21} = (S_{21} - S_{41} - S_{23} + S_{43})/2$$

$$S_{DD22} = (S_{22} - S_{42} - S_{24} + S_{44})/2$$
Eq. (3)

$$S_{DC11} = (S_{11} - S_{31} + S_{13} - S_{33})/2$$

$$S_{DC12} = (S_{12} - S_{32} + S_{14} - S_{34})/2$$

$$S_{DC21} = (S_{21} - S_{41} + S_{23} - S_{43})/2$$

$$S_{DC22} = (S_{22} - S_{42} + S_{24} - S_{44})/2$$
Eq.(4)

The respective diagonal and off-diagonal elements in Eq. (3) and Eq. (4) differ only by a negative sign in the last two terms of the numerator. As shown in Eq. (5), we can create a "THRU-equivalent" s-parameter file for the SDC noise channel, S_{mod}^{se} , whose matrix terms are easily derived from the original s-parameters by simple insertion of negative signs in the last two columns of the matrix. This technique allows us to mathematically "trick" the AMI algorithm into transforming matrix S_{mod}^{se} into an SDC matrix.

$$S^{se} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix}$$

$$S^{se}_{mod} = \begin{bmatrix} S_{11} & S_{12} & -S_{13} & -S_{14} \\ S_{21} & S_{22} & -S_{23} & -S_{24} \\ S_{31} & S_{32} & -S_{33} & -S_{34} \\ S_{41} & S_{42} & -S_{43} & -S_{44} \end{bmatrix}$$
Eq. (5)

Figure 5 shows a general schematic implementation of both THRU and mode-converted noise channels. In our example, we can create an .s6p s-parameter file as shown. The "Combined_Channel" is composed of the original THRU channel s-parameter S^{se} and the mode-converted noise channel S^{se}_{mod} . What is important in creating the "Combined_Channel" file is that {1-2; 3-4} and {5-2; 6-4} are equivalent to the original 2 files. Also note that the original TX source, which contains both differential and common mode components, is generated in both the SDD THRU channel ("TX_SDD") and equivalent noise source ("TX_SDC").



Figure 5. EDA schematic setup to complement SDC equivalent noise source with conventional SDD THRU Channel

4. Mode-Conversion Modelling Examples

Based on the setup, an IBIS-AMI simulation example is performed with the needed modifications to include the mode-conversion channel as an equivalent noise source. Simulation conditions include:

- 112Gbps PAM4 signaling simulated with a <u>hardware correlated</u> IBIS-AMI model
- PRBS23, gray-coded, is the data pattern for the simulation
- TX output swing is set to 1000 mVdpp
- The 3-tap TX FFE coefficients are manually configured and fixed for all simulations
- RX side equalizers include multi-stage CTLE, AGC, and a DSP (FFE and DFE)
- RX equalizer and CDR parameters are all adaptively tuned
- Offset and baseline wander cancellation is adaptive as well
- Crosstalk is excluded: the purpose is to compare skew and mode conversion effect
- In each setup 2.8M symbols are simulated. The first 1.8M is for adaptation convergence, and the last 1.0M is used to evaluate BER and to plot eye diagrams

A. BER Degradation of SDD21-only Channels

Let us first exemplify the effects of loss-based skew effects of the "RC" channels when SDD21 is only considered without mode-converted noise. Subsequent results are summarized in Table 1. Without taking mode-converted noise effects into consideration, the intra-pair skew already introduces more loss as reflected in the simulated link BER's. Note that the BER is not necessarily inversely proportional to channel loss: there are many other factors, including the settings in the TX and RX equalizers and specific features in the SerDes architecture that contribute to such non-linearity. Overall, Table 1 demonstrates a clear trend: the inclusion of loss-based skew-effect does indeed entail an erosion in BER margin. The subsequent BER erosion can also be visualized by the progressively shrinking 112G-PAM4 eye apertures as shown in Figure 6 below. Another notable observation is that resonance effects well beyond the Nyquist do influence BER, thus making it clear that it is no longer sufficient to just consider the spectral properties up to the Nyquist frequency.

Channel	RC-0	RC-5	RC-10	
Loss at 28GHz	22.76 dB	24.11 dB	28.05 dB	
BER	1.22e-11	4.35e-11	1.01e-9	

Table 1. Original THRU channel modeling with only SDD21



Figure 6. Simulated 112G-PAM4 Eye Diagrams for (a) RC-0 channel, (b) RC-5 channel, and (c) RC-10 channel

B. BER Degradation of SDD21 Channels with Mode-Converted Noise

The SDD-only simulation scenario in the above example typifies today's IBIS-AMI simulation environment. Although the SDD model does indeed capture loss-based effects of mode conversion due to intra-pair skew, the SDD-only topology has no such provisions to include mode-converted noise. We shall demonstrate the deficiencies of the SDD-only topology by exemplifying the aggregate effects of mode-converted noise on overall BER performance when mode conversion is incorporated into the modeling topology.

The previous SDD21-only analysis with RC channels illustrated that increasing amounts of intra-pair skew generally leads to increasing loss, which corresponds to a subsequent increase in BER. To properly compare the effects of SDC mode-converted noise on link performance, the RC trace models will need to be renormalized for a fixed loss budget. For this example, we shall intentionally increase RC-0 and RC-5 channel lengths such that their insertion loss at 28 GHz is equal to RC-10 insertion loss of 28 dB. The increased losses are facilitated by cascading the 0ps skew channel (RC-0) and the 5ps skew channel (RC-5) with additional PCB trace lengths (perfectly balanced) such that all 3 channels are normalized to 28dB loss at 28GHz. The renormalized SDD21 spectra are depicted in Figure 7 below. To minimize confusion, let us refer to the newly renormalized channels as MC-0, MC-5, and MC-10. Obviously, RC-10 is the same as MC-10 as its SDD21 loss is already anchored at 28 dB.



Figure 7. Modified example channels normalized to 28 dB SDD21 loss

Next, let us now utilize the MC channels and include SDC mode-converted noise source by applying the proposed modelling topology depicted in Figures 3 and 5. Subsequent IBIS-AMI simulation results are tabulated in Table 2 that compares BER performance for the following perturbation sweeps:

- "THRU-only" SDC mode-converted noise injection excluded
- "THRU with SDC" SDC mode converted noise injection included

Notable observations from the tabulated results are as follows:

- 1. Even though the MC channels are approximately normalized for equivalent losses at the Nyquist frequency, the "THRU-Only" sweep clearly shows that the largest skew channel (MC-10) exhibits the worse BER performance. The tabulated BER's clearly show that resonant suckouts well beyond the Nyquist frequency adversely affect overall bandwidth and subsequent BER performance. Higher skew leads to greater BER as the suckout frequency creeps closer to Nyquist frequency.
- 2. The inclusion of SDC noise injection generally leads to an immediate increase in BER relative to the "THRU-Only" scenario: this demonstrates that the inclusion of SDC mode-conversion effects is not insignificant and should be considered as another source of noise impairment.
- 3. The MC-0 perturbations demonstrate that even with perfectly de-skewed differential pairs, residual physical imbalances in the channel could lead to incremental erosion in BER performance.
- 4. Inclusion of non-zero physical imbalance leads to significant decay in BER performance. SDC mode-converted noise injection perturbations exemplify the following increases in BER degradation:
 - MC-0: less than half order of magnitude BER increase when modeconverted noise included
 - MC-5: 1.5 orders of magnitude BER increase when mode-converted noise is included ,
 - MC-10: <u>more than 3 orders of magnitude</u> BER degradation when mode converted noise is included

Channel	MC-0	MC-5	MC-10
THRU-Only: BER without SDC Noise Injection	1.65e-11	1.33e-10	1.01e-9
THRU with SD: BER with SDC Noise Injection	5.37e-11	7.91e-8	6.05e-5

Table 2. Modified THRU channel modeling comparison

The exponential decay in BER performance, described in the 4th observation above, can be visualized in Figure 8 below. The PAM4 eye diagrams on the left column ("THRU-Only") exhibits a general decrease in eye aperture margins with increasing skew. However, a left-to-right column comparison clearly demonstrates significant deterioration once SDC mode-converted noise is injected into the THRU channel.

Overall, the above perturbation study demonstrates inclusion of non-zero intra-pair skew in tandem with imperfect differential balance could potentially lead to significant erosion in BER performance. The bottom line factor for high speed serial designers is clear: there is a potential risk of overestimating link performance margins at 112G-PAM4 when aggregate mode-conversion effects are not considered.



Figure 8. Simulated 112G-PAM4 Eye Diagrams for (a) MC-0 THRU-Only, (b) MC-0 THRU with SDC, (c) MC-5 THRU-Only, (d) MC-5 THRU with SDC, (e) MC-10 THRU-Only, (f) MC-10 THRU with SDC

5. Conclusions

Standard IBIS-AMI channel modeling topologies consider only pure differential channels to capture ISI properties from associated differential impulse responses. Moreover, standard modeling practices assume channels with perfect differential balance and zero skew, i.e. channels with negligible mode conversion. Previous studies have shown that mode conversion effects on link performance margins are, at worst, marginal for applications up to 32 Gbps NRZ. Thus, mode conversion was considered a second-order effect that could safely be neglected in IBIS-AMI modeling.

A modified IBIS-AMI modeling topology is proposed in this paper to incorporate aggregate mode conversion effects on link margins. Heuristic IBIS-AMI modeling studies with the modified topology demonstrate that impairment effects of mode-conversion on highly constrained 112G PAM4 jitter margins are not insignificant. Thus, aggregate mode conversion effects due to imperfect intra-pair skews and imperfect differential balance should be considered as additional sources of THRU channel impairment.

References

- [1] Jason Chan, et al, "Performance Limitations of Backplane Links at 6 Gbps and Above", DesignCon 2008
- [2] Ken Ly, et al, "Channel Mode Conversion Impact on 56G-PAM4 Link Performance", OIF2015.475.01