DesignCon 2019

The Problem of Comparator Metastability in High-speed Wireline Receivers

Sina Naderi Shahi, Huawei Canada – HiLink,

sina.naderi.shahi@huawei.com

Marc-Andre LaCroix, Huawei Canada - HiLink

Semyon Lebedev, Huawei Canada - HiLink

Davide Tonietto, Huawei Canada - HiLink

Abstract:

With the adoption of ADC-based transceivers at 56-Gb/s and beyond, ADC comparator metastability induced errors (MIE) become part of the communication link impairment profile. In order to reduce the probability of MIE typically requires an increase in power, area or complexity of the ADC. Yet, the impact of MIE upon links that feature forward-error correction (FEC) has, to our knowledge, not been reported upon. Our work investigates this problem within the context of a 56-Gb/s transceiver implemented with 32 interleaved asynchronous SARs (ASARs). We first develop a theoretical framework for predicting the probability of MIE for each bit in an ASAR based ADC. We then validate our findings with full link-level time domain simulations and BER measurements from our 56-Gb/s transceiver communicating over a link with insertion loss of 38 dB. We conclude with revised guidance for our ADC design.

Author Biographies:

Sina Naderi Shahi joined Huawei Technologies in 2014 as a system engineer. He has been working on signal integrity, link architecture and modeling throughout his tenure. He received his MSc in 2008 from Sharif University of Technology, Iran, and Ph.D. degree in 2013, from McMaster University, Canada. His current interests include equalization, CDR, FEC, and modeling methodologies. Currently, he is involved in the development of 112-Gb/s technologies for optical and electrical channels.

Marc-Andre LaCroix received B.Sc.Eng (EE) degree from the University of New-Brunswick, in 2000, and the M.A.Sc in electrical engineering from Carleton University, Ottawa ON, Canada, in 2002. Since 2011 he has been with Huawei Technologies where he has served as design lead, and architect for several generations of high-speed wireline transceivers. Prior to joining Huawei, he held positions at Gennum Corporation, STMicroelectronics, and Nortel Networks. He has been involved in the design of wireline transceivers throughout his career.

Semyon Lebedev received M.S. degree from Leningrad Electro-Technical University, Russia in 1977. Currently, he is Principle Engineer at Huawei Canada developing high-speed SAR ADCs. He has more than 30 years of experience working for Intel, Blackberry and other companies in transceivers field.

Davide Tonietto received his Laurea Degree in 1995 from University of Pavia, Italy. Currently he is the Director of SerDes Development at Huawei Canada Research Center, Ottawa. He has more than 15 years of experience in signal integrity and high speed serial interface design and development. Previously he was Senior Manager of Signal Integrity IC development at Gennum Corporation, Manager of SerDes IP development at STMicroelectronics and lead designer of high speed serial interfaces, at Broadcom and other companies.

I. Introduction:

Several SAR ADC based wireline receivers targeting emergent 50+ Gbps PAM-4 standards have been demonstrated in recent years. These receivers have largely favored SAR converters due to the competitive power efficiency within the resolution range (5b-8b) required in the space. Moreover, these works have shown that suitable power-performance is achieved with interleaving factors as low as 32x [1-3]. The sub-ADCs within these receivers must quantize to the desired resolution in less than ~1ns. In this regime, the problem of comparator metastability is of interest due to the reduced timing budget. A common method to address the problem has been to design the comparator (and per bit conversion loop) to be sufficiently fast such that the error probability lies below target rates. This solution invariably leads to worsening Power Performance Area (PPA) since power or area must be expensed to increase margin.

Now that emergent 'PAM-4' standards have introduced forward error correction (FEC) we propose to leverage the correction capability in setting the targets for the ADC metastability rate. In this paper we demonstrate how superior PPA can be achieved while meeting total link BER.

This paper first explores the problem of metastability induced error (MIE) in asynchronous SAR (ASAR) ADCs. MIE and its probability is well-understood in synchronous SARs, and it has been described with simple, closed-form equations [4, 5]. However, the analysis becomes more complicated for asynchronous SAR ADCs. Herein, we present a simplified analytical approach to find the probability of a MIE for each bit (MSB to LSB) in ASAR ADCs. The importance of a MIE at system level depends on the position number of the binary bit responsible for this error within the *N*-bit ADC output code. Consequently, it is essential to understand the related per bit probabilities. We validate our findings with time domain simulations of an ASAR.

Finally, we demonstrate the impact of MIE in ASARs upon system level BER with simulations and measurements of our 56-Gb/s ADC-DSP transceiver communicating over a high loss channel. Our transceiver is implemented in 16nm FinFet and features 32 time-interleaved ASAR sub-ADCs and a full integrated DSP. In both contexts (e.g. in simulation and measurement) we stress the ASARs in order to increase the probability of MIE. The results indicate that the average conversion time can be increased substantially with significant PPA improvement. We surmise that the probability of LSB sized MIE can be as high as 10^{-2} with no impact to BER.

II. Analysis of Probability of Metastability in SAR and ASAR ADCs

A comparator is said to have entered a meta-state condition if it fails to produce a sufficiently large output voltage so as to be correctly interpreted by downstream circuits. In this case, the resulting output may be invalid resulting in an error in the overall ADC output code; the severity of which depends upon its location within the code. Simply stated, an error in the most significant bit (MSB) is more damaging than an error in the least

significant bit (LSB) due the radix-2 relationship of bit position (for binary conversion). Comparator meta-stability (MS) is a well-researched topic [4-8], thus this section provides but a brief overview. We then expand to multi bit conversion processes and focus upon per-bit MS event probability in ASARs.

A. Review of comparator meta-stability

The comparator input-output relationship is defined by [4]:

$$V_{out}(\mathrm{t}) = A_0\, V_{in}\, \mathrm{e}^{(\mathrm{t}\,/\,\tau_{\mathrm{comp}})} \quad \textbf{(1)}$$

where A_0 is comparator gain, τ_{comp} is comparator time constant, and V_{in} and V_{out} are comparator input and output voltages, respectively. As V_{in} gets smaller (e.g. the input voltage approaches the comparator decision level), longer time is required for the output to reach a valid voltage level, V_{valid} (See Figure 1-b). The relationship between valid output voltage and time is described in Eq. 1 and can be re-written using these terms as shown in Eq. 2.

$$V_{valid} = A_0\, V_{in}\, \mathrm{e}^{(t_{comp-rq}\,/\,\tau_{\mathrm{comp}})} \quad \textbf{(2)}$$

where $t_{comp-rq}$ is comparator regeneration time required to receive V_{valid} at the comparator output. The regeneration time, is thus given by (3), where it has also been normalized with respect to τ_{comp}. Note that comparator required regeneration time increases logarithmically with $1/V_{in}$.

$$T_{comp-rq} = \frac{t_{comp-rq}}{\tau_{\mathrm{comp}}} = \ln\left(\frac{V_{valid}}{A_0\, V_{in}}\right) \quad \textbf{(3)}$$

The overall behavior is depicted in Figure 1-c. It can be seen that, larger $|V_{in}|$ results in smaller $T_{comp-rq}$ and vice-versa. From (3), it is also possible to define a minimum input voltage (V_m) that allows full regeneration (V_{valid}) within the available comparator time $t_{comp-av}$. The comparator thus always produces a valid output for input voltages above this threshold.

$$V_{valid} = A_0\, V_m\, \mathrm{e}^{(t_{comp-av}\,/\,\tau_{\mathrm{comp}})} \quad \textbf{(4)}$$

$$V_m = \frac{V_{valid}}{A_0}\, \mathrm{e}^{(-T_{comp-av})} \quad \textbf{(5)}$$

$$T_{comp-av} = t_{comp-av}\,/\,\tau_{\mathrm{comp}} \quad \textbf{(6)}$$

For all voltages in the range $|V_{in}| < V_m$ (hereby defined as the metastate window or MSW as shown in Figure 1-c), the output voltage cannot reach V_{valid} and a MS event is created. The MSW for a single comparator is illustrated in Figure 1-b and Figure 1-c.

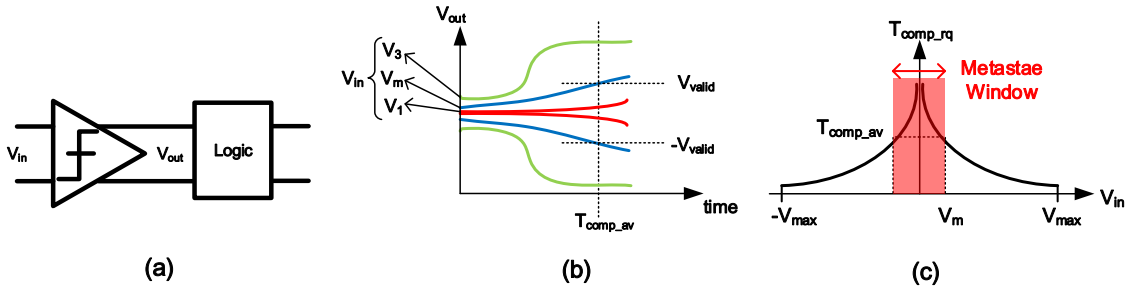

Figure 1: (a) Comparator and logic block, (b) V_{out} vs time for different V_{in}, (c) Required comparator time ($T_{comp-rq}$) vs V_{in} and MSW for given available comparator time ($T_{comp-av}$)

The MS event probability is calculated by dividing the area of the input voltage PDF that lies within the MSW by the total area of the input voltage PDF. For example, in the case of a uniformly distributed input, the MS event probability is given by:

$$P_{MS} = V_m / V_{max} \qquad (7)$$

B. Extending to multi-bit cycles in SAR and ASAR ADC

For a synchronous SAR ADC $T_{comp-av}$ and MSW size are equal for all bits. Prior work [4, 5] has shown that P_{MS} can be calculated in closed form. However, for asynchronous SAR (ASAR) ADC, there is no specific time allocation for each bit conversion. Each bit uses some part of the overall $T_{comp-av}$ making difficult to define the individual MSWs per binary bit. Few ASAR meta-stability studies are reported in the following publications [6-8]. In the following discussion, a simplified analytical approach is developed for calculating the MSW for each bit in an ASAR ADC. A similar approach was used in [8].

In a typical ASAR ADC, the overall conversion time can be divided into two main parts (Figure 2). The first part is the time required in preparation of per-bit conversion and is not dependent on comparator input values. This phase can include sampling time and reset time amongst other possible functions. And importantly, the time consumed in this phase is fixed and thus equal across cycles. The second part is as a result of the successive approximation process. It is the time, (T_{conv}), used for conversion of all bits. It also can be divided per each bit (assuming one bit per each conversion) into constant and variable components, (T_c), and ($T_{\tau,i}$), respectively. The constant term is independent of input voltage and includes time for comparator reset, pre-amplification, and general signal propagation (for the simplicity of discussion we assume that DAC output waiting time is also included into this term.). The variable term captures the comparator regeneration time and is a function of input voltage.

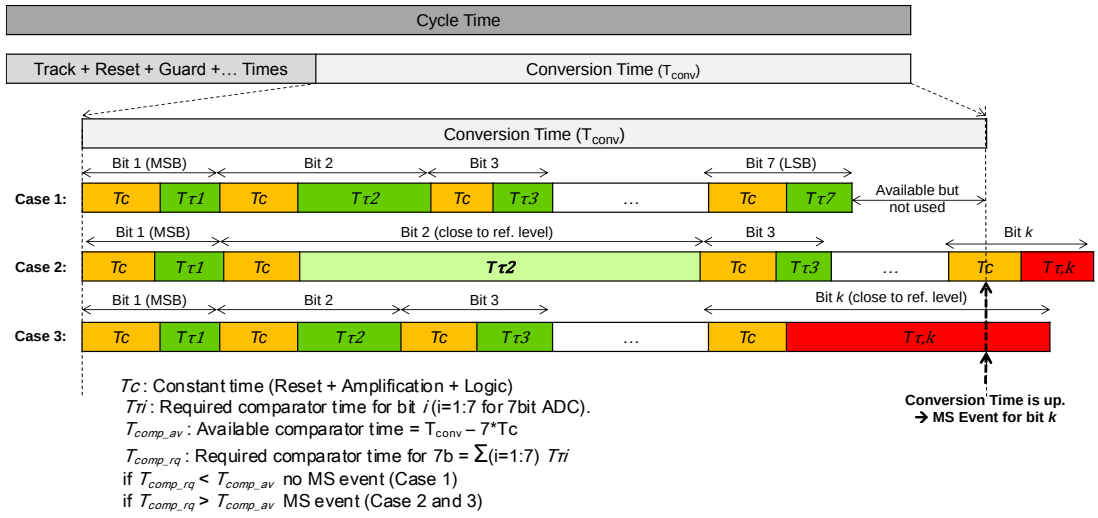

Figure 2: ASAR ADC bit conversion. Case 1: no MS event. Case 2 and 3: MS event at bit k.

For a N_b bit SAR ADC, the total required comparator regeneration time is equal to the sum of all per bit regeneration times:

$$T_{comp-rq} = \sum_{i=1}^{N_b} T_{\tau,i} \tag{8}$$

where $T_{\tau,i}$ is the required comparator regeneration time for bit i:

$$T_{\tau,i} = \frac{t_{comp-rq,i}}{\tau_{\text{comp}}} = \ln\left(\frac{V_{valid}}{A_0\, V_{in,i}}\right) \tag{9}$$

$$V_{in,i} = |(ADC\ Input\ Voltage) - (Bit\ \text{i}\ Reference\ Voltage\ Decision\ Level)|$$

The global MS event will be non-zero if $T_{comp-rq} > T_{comp-av}$. The total regeneration time available ($T_{comp-av}$) is equal to the difference between the total conversion time (as previously defined) and the sum of the per bit constant terms.

$$T_{comp-av} = T_{conv} - N_b T_c \tag{10}$$

Three scenarios are depicted in Figure 2 to further illustrate the dynamic properties. In the first scenario (case 1), the input voltage is located relatively far from any of the ADC decision levels (true for each comparison) and $T_{comp-av} > T_{comp-rq}$ (no MS event). By contrast, in case 2, the input voltage is in close proximity to the second bit decision level resulting in long comparator regeneration time for this bit ($T_{\tau,2}$). Although the 2nd bit ultimately converges, there remains insufficient time for processing all subsequent bits. In this example, a non-zero MS event on the bit *k* is created as a direct consequence of the lengthy regeneration time experienced on the 2nd bit. In the other possible scenario (case 3

in Figure 2), input voltage is close to k^{th} bit decision level resulting in long regeneration time for this bit ($T_{\tau,k}$). It also creates a MS event on the bit *k*.

C. Total comparator regeneration time across for multiple cycles

Regeneration time was previously described for a generic comparator operating from a single reference level (Eq. 3). This concept is now expanded to include all comparison decision levels relevant to an ADC's conversion process. In Figure 3, the comparator regeneration time ($T_{comp-rq}$) is shown versus input voltage for a 2-bit and 3-bit ADC. An ADC with 2 and 3-bits is first chosen in order to maximize clarity. In these examples, the gain $A_0 = 2$, and the ADC input dynamic range is assumed to be 400mV.

Note that the required regeneration time increases logarithmically (Eq. 9) as the input voltage approaches any of the decision levels. In the 2-bit example asymptotes are seen near 0 mV, and +/- 100 mV. Though masked by apparent complexity, the same underlying situation arises in higher resolution ADCs such as the 7-bit ADC shown in Figure 4. In this ladder case, there are 127 decision levels and related spikes. The number of possible asymptotes is equal to the number of levels, $2^{(N-1)}$, and thus grows exponentially per bit.

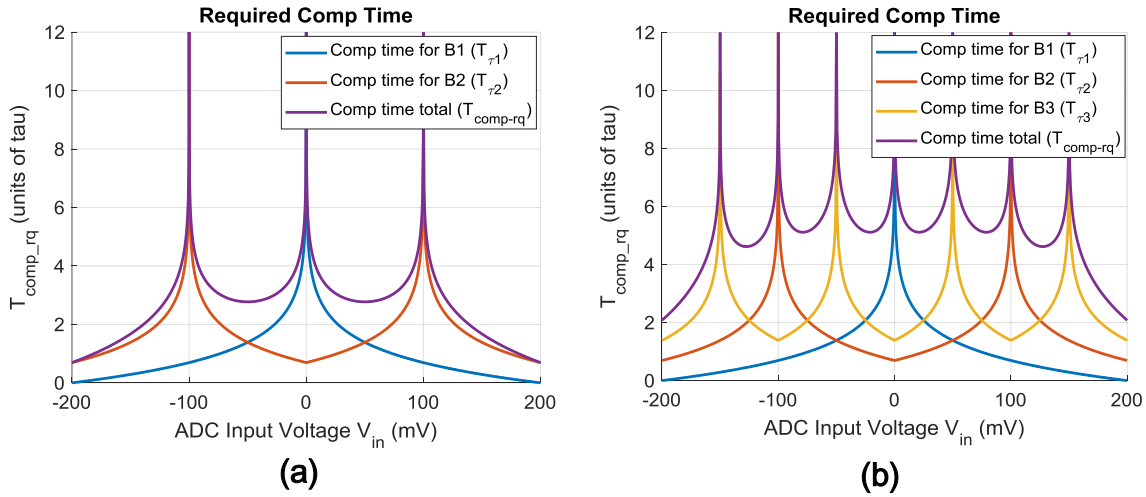

Figure 3: Required comparator time for (a) 2bit SAR ADC, (b) 3bit ADC. Comparator gain $A_0 = 2$, ADC input dynamic range = 400mV.

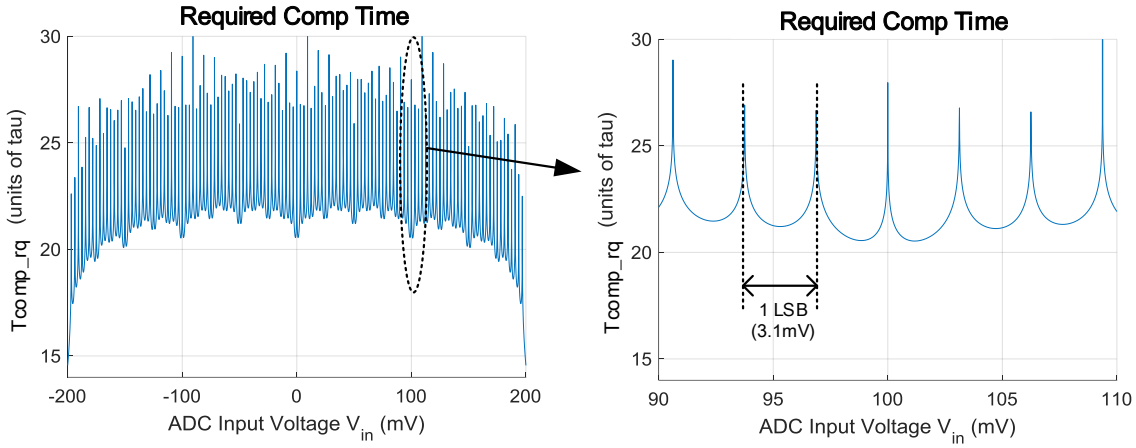

Figure 4: Required comparator time for a 7bit ADC. Comparator gain $A_0 = 2$, ADC input dynamic range = 400mV.

The combined distributions is the total regeneration time needed for all input voltages. Any input that has a corresponding regeneration time $T_{comp-rq} > T_{comp-av}$ will result in a global MS event. The probability of such an error on a per bit basis is discussed in the next section.

D. The MSWs

In this section, we present an analytical method for determining the location and width of the MSW for each bit in the ASAR conversion process. As alluded to earlier, the MSW size for each individual bit depends on its binary position. In turn, the different size of the MSWs impacts the MS event probability for each bit and so an accurate method to calculate these is essential. Figure 5 illustrates all MSWs for bit-1 (MSB), bit-2 and bit-3. The analytic solution, and its development, is explained relative to Figure 5 and the cases it contains. Beyond these, the concept is easily generalized and extended to more bits.

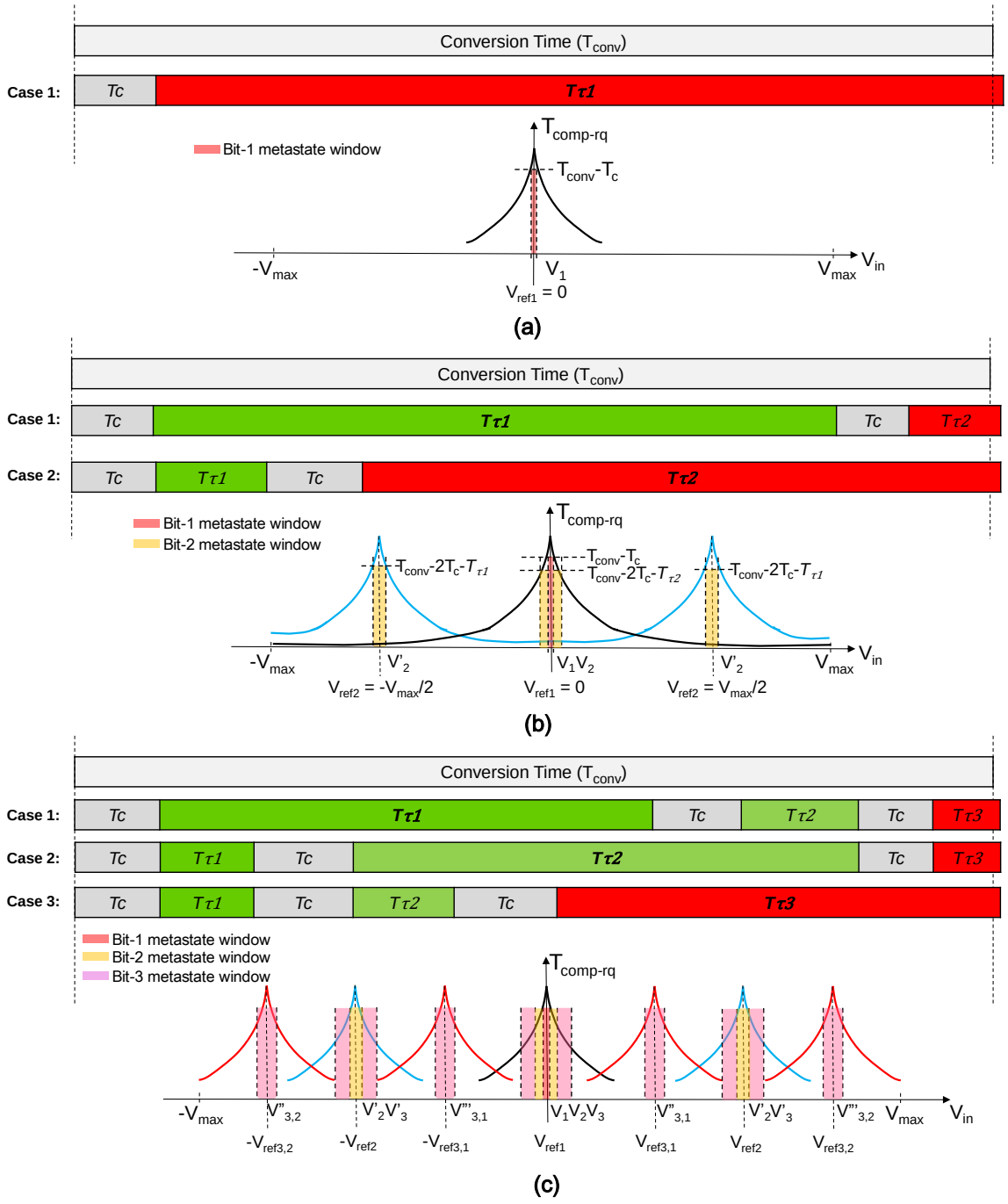

Figure 5: Mechanism of MS event for (a) bit-1 (MSB), (b) bit-2, (c) bit-3

MSW for 1st bit

The 1st bit is the easiest. There is only one MSW, it is folded about the initial decision level and extends outward to V_1. It is evident that a MS event will be generated for input voltages that satisfy $|V_{in} - V_{ref1}| < V_1$. In this case, the constant time (T_c) plus required comparator regeneration time ($T_{\tau,1}$) is bigger than total 7-bit conversion time (T_{conv}) (Figure 5-a):

$$T_c + T_{\tau,1} > T_{conv} \quad (11)$$

or

$$T_{\tau,1} > T_{conv} - T_c \quad (12)$$

In order to define the width of the window (V_1), $T_{\tau,1}$ in Eq. 12 is replaced with its equivalent representation based upon the input, reference, and target voltages:

$$\ln\left(\frac{V_{valid}}{A_0\left(V_1 - V_{ref1}\right)}\right) = T_{conv} - T_c \quad (13)$$

Setting $V_{ref1} = 0$ (for this 1st bit) gives the following expression for MSW width:

$$V_1 = \frac{V_{valid}}{A_0}\ \mathrm{e}^{(-(T_{conv}-T_c))} \quad (14)$$

Note that the width of the window is independent of the input voltage, and that it is quite narrow owing to the large (total) amount of time available ($T_{conv} - T_c$). We thus expect a relatively low MS event probability for the 1st bit in an ASAR.

MSW for the 2nd bit

Next we consider the 2nd bit. As was shown in Figure 5-b, there are two ranges of input voltage which may result in a non-zero MS event probability. Each is now explored in turn. Here, V_{ref2} corresponds to decision reference levels of 2nd bit, and V_2 and V_2' correspond external borders of 2nd bit MSW.

Case 1: The 1st comparison successfully regenerates but there is insufficient time for the fastest possible conversion of the 2nd bit (depicted as inner windows in Figure 5-b). The condition occurs for the following voltage range:

$$(V_1 < \left|V_{in} - V_{ref1}\right| < V_2),$$

where the total regeneration and constant time is larger than the total conversion time:

$$T_c + T_{\tau,1} + T_c + T_{\tau,2} > T_{conv} \quad (15)$$

or

$$T_{\tau,1} + T_{\tau,2} > T_{conv} - 2T_c \quad (16)$$

Substituting for $T_{\tau,1}$ and $T_{\tau,2}$ in order to define the MSW for the 2nd comparison (e.g. 2nd bit regeneration):

$$\ln\left(\frac{V_{valid}}{A_0\,(V_2)}\right)+\ln\left(\frac{V_{valid}}{A_0\left(\left|V_{ref2}-V_2\right|\right)}\right)=T_{conv}-2T_c \tag{17}$$

Note that both $T_{\tau,1}$ and $T_{\tau,2}$ are functions of V_{in}. However, since V_{in} (in this case) is located far enough from V_{ref2} (near constant slope region), $T_{\tau,2}$ can be replaced by a constant value $T_{\tau,2}\left(V_1<\left|V_{in}-V_{ref1}\right|<V_2\right)\cong T_{\tau,2}(V_1)$ which corresponds to the fastest possible regeneration time for bit2:

$$T_{\tau,2}=\ln\left(\frac{V_{valid}}{A_0\left(V_{ref2}-V_2\right)}\right)\cong\ln\left(\frac{V_{valid}}{A_0\left(V_{ref2}-V_1\right)}\right) \tag{18}$$

Now V_2 can be easily found:

$$T_{\tau,1}=T_{conv}-2T_c-T_{\tau,2} \tag{19}$$

$$\ln\left(\frac{V_{valid}}{A_0\,(V_2)}\right)=T_{conv}-2T_c-T_{\tau,2} \tag{20}$$

$$V_2=\frac{V_{valid}}{A_0}\,\mathrm{e}^{(-(T_{conv}-2T_c-T_{\tau,2}))} \tag{21}$$

To summarize, under this input condition, the valid MSWs for the 2nd bit are localized in $\pm(V_2-V_1)$. Furthermore, the width of the window is approximately constant due to the liming behavior of $T_{\tau,2}$.

Case 2: V_{in} is close to the 2nd bit decision level V_{ref2} such that ($\left|V_{in}-V_{ref2}\right|<V_2'$). In this case, $T_{\tau,1}$ is much smaller than $T_{\tau,2}$ since V_{in} implicitly lies far enough from V_{ref1}. Using the same general approach as for case 1, MSW (V_2') can be calculated as follows:

$$T_{\tau,1}=\ln\left(\frac{V_{valid}}{A_0\left(V_{ref2}-V_{ref1}\right)}\right) \tag{22}$$

$$T_{\tau,2}>T_{conv}-2T_c-T_{\tau,1} \tag{23}$$

$$V_2'=\frac{V_{valid}}{A_0}\,\mathrm{e}^{(-(T_{conv}-2T_c-T_{\tau,1}))} \tag{24}$$

The MSW thus spans $\pm\left|V_2'-V_{ref2}\right|$ around the two locations of V_{ref2}.

The approach outlined thus far can be extended for all other bits and used to calculate their possible MSWs. As a last example, we provide the breakdown for the 3rd bit below.

.

$$V_3 = \frac{V_{valid}}{A_0}\ \mathrm{e}^{(-(T_{conv}-3T_c-T_{\tau,2}-T_{\tau,3}))} \quad (25)$$

$$T_{\tau,2} = \ln\left(\frac{V_{valid}}{A_0\left(V_{ref2}-V_2\right)}\right) \quad (26)$$

.

$$T_{\tau,3} = \ln\left(\frac{V_{valid}}{A_0\left(V_{ref3}-V_2\right)}\right) \quad (27)$$

.

$$V_3' = \frac{V_{valid}}{A_0}\ \mathrm{e}^{(-(T_{conv}-3T_c-T_{\tau,1}-T_{\tau,3}))} \quad (28)$$

.

$$T_{\tau,1} = \ln\left(\frac{V_{valid}}{A_0\left(V_{ref1}-V_2'\right)}\right) \quad (29)$$

$$T_{\tau,3} = \ln\left(\frac{V_{valid}}{A_0\left(V_{ref3}-V_2'\right)}\right) \quad (30)$$

.

$$V_{3,i}'' = \frac{V_{valid}}{A_0}\ \mathrm{e}^{(-(T_{conv}-3T_c-T_{\tau,1,i}-T_{\tau,2,i}))} \quad (31)$$

.

$$T_{\tau,1,i} = \ln\left(\frac{V_{valid}}{A_0\left(V_{ref3,i}-V_{ref1}\right)}\right) \quad (32)$$

$$T_{\tau,2,i} = \ln\left(\frac{V_{valid}}{A_0\left(V_{ref3,i}-V_{ref2}\right)}\right) \quad (33)$$

E. Calculating the MS event probability

For an input with uniform PDF (our case) the per-bit MS event probabilities are calculated as ratios of the sum of bit related MSWs to total input span. Figure 6 compares the MS event probability vs $T_{comp-av}$ received by analytical approach vs time-domain simulations. For time-domain simulations, in order to find the MS event probability, 10^{10} uniformly distributed samples were generated. As seen in the figure, time-domain simulations show good agreement with the analytical approach. Furthermore, we note that the most significant bits have much lower MS event probability since they can use T_c and the conversion time of the following bits. Three different constant times (T_c) were used for comparison in Figure 6. Note that as T_c increases, available conversion time T_{conv} also increases because of $T_{conv} = T_{comp-av} + N_b T_c$ assumption. For fixed T_{conv}, increase of T_c reduces available comparator conversion time ($T_{comp-av}$) resulting in the higher MS event probability.

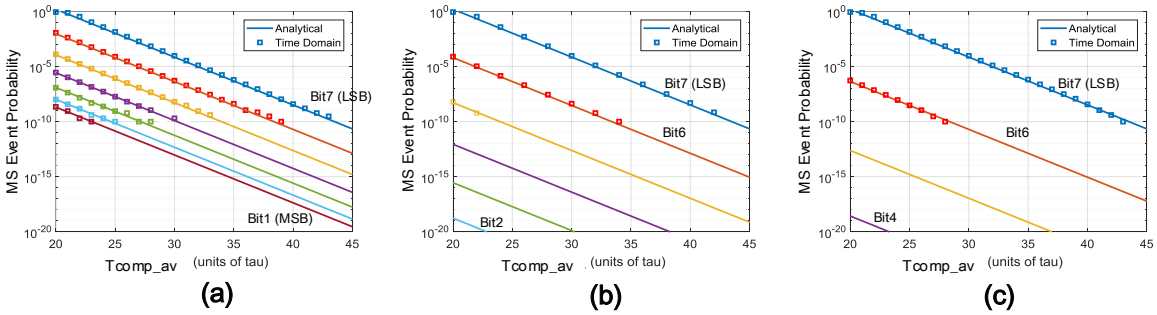

Figure 6: MS event probability vs $T_{comp-av}$ for (a) $T_c = 0$, (b) $T_c = 5\tau$, (c) $T_c = 10\tau$. ASAR ADC number of bit = 7,

III. Metastability Impact on System Performance

A. Metastability induced error (MIE)

In the previous section, a method to compute the probability of a MS event for each bit ($P_{MS,k}$ k = $1, \ldots, N_b$) in an ASAR's output code was presented and ultimately validated with time domain simulation. These bit-wise metastate probabilities are themselves not representative of the total error probability (for each bit). Nor do they inform upon the magnitude of any error that ultimately does occur. In this section, we extend the analysis and translate bit-wise probability of MS event to probabilities of errors of different magnitudes or MIE. This is a key component in the translation to the link bit-error-rate (BER). The outcome leads to new guidelines for the bit-wise probability of MS event which in-turn allows for relaxation of ASAR maximum allowable conversion time requirements.

In ASAR(s), processing and conversion of bit (*N+1*) is gated by the completion of the prior bit (*N*). Thus, failure to complete conversion for any one bit results in the current bit and

all lower order bits retaining their default state. For our purposes here, we assume the default state to be logic 0 but it could just as easily be 1. Note that this statement is not intended to imply usage of metastate detection and correction concepts. These have been widely reported upon [9, 10] and remain somewhat controversial. In fact, for channels operating at 56-Gb/s, where PAM-4 and FEC has been standardized we show that such approaches are unnecessary.

We first present two simple MS scenarios (for a 7b ADC) in Figure 7 to illustrate how an MS event translates to a MIE; and to further show that, once created, MIE has limited number of possible magnitudes. To quantify SNR impact we are interested in the ladder point.

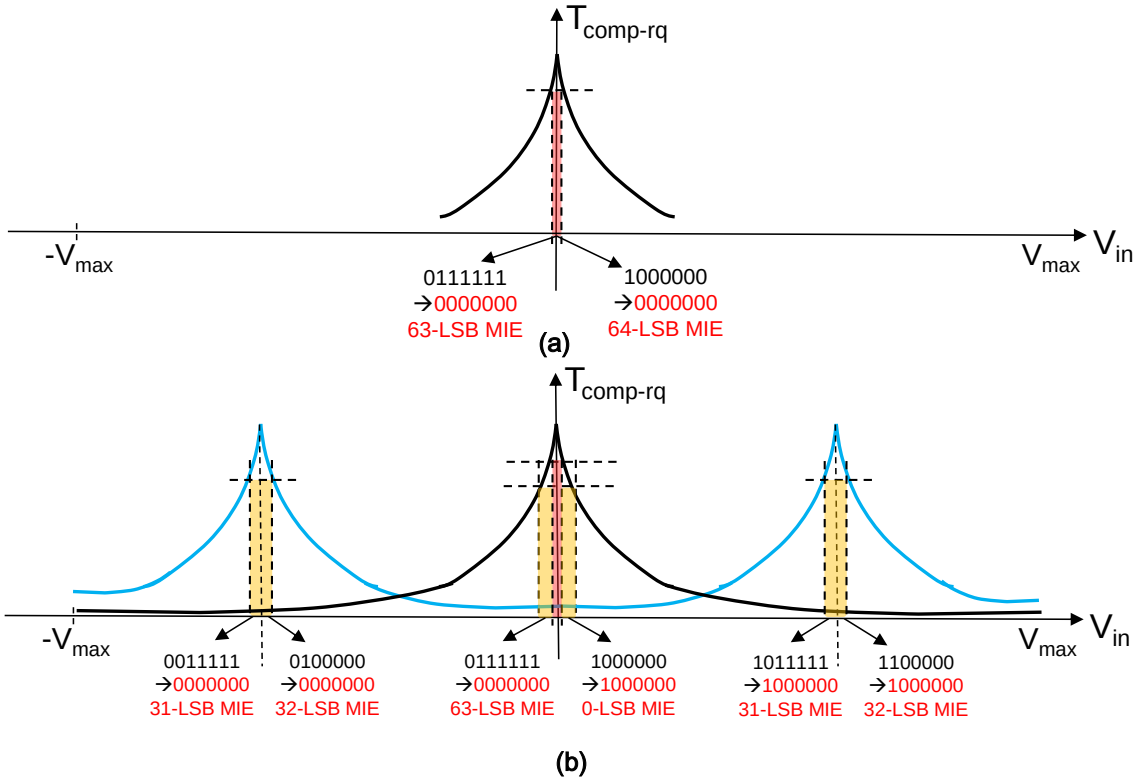

Figure 7: MS event and MIE magnitude relationship: (a) MS event for MSB (bit 1), and (b) MS event for bit 2

In the first case, a MS event occurs in the 1st bit (MSB) and it is not converted. The ADC output code retains the default or reset state at this position (0000000). As shown in Figure 7-a, there are two possible codes that fall into MSW of bit 1: 0111111 (code 63) and 1000000 (code 64). Within the MSW, both cases result in ADC output of 0000000 (code 0). In this limited case, there is direct equivalence to there being a 50% probability for an error with MIE magnitude of 63-LSB and 64-LSB.

Figure 7-b shows possible MIE magnitudes when MS event occurs in bit 2: 31-LSB, 32-LSB, and 63-LSB. It can also be shown than possible MIE magnitudes for MS event in bit

3 are: 15-, 16-, and 31- LSB. Expanding this for a 7-b ADC, possible MIE magnitudes are: 64-, 63-, 32-, 31-, 16-, 15-, 8-, 7-, 4-, 3-, 2-, 1-LSB. Knowing the MSWs for each case (Section II.D), probability of MIE for each magnitude can be calculated.

Figure 8 shows the simulated MIE vs available comparator time for $T_c = \mathbf{0\tau}, \mathbf{5\tau}, \mathbf{10\tau}$. Solid line shows the analytical approach results which are validated by time-domain simulation (star markers). Note that when $T_c = \mathbf{10\tau}$, MIE with magnitudes of 2- and 3-LSB are $\sim 10^7$ times less likely than 1-LSB errors. And that the MIE at these magnitudes is as low as $\sim 10^{-16}$ with available comparator time of $\mathbf{40\tau}$. This is a reasonable number for 1-Gs/s ADCs [11]. Errors with 1-LSB magnitude are much more likely and dominate the overall MIE (across all magnitudes). However, they also have a low probability of occurrence reaching $\sim 10^{-9}$ at $\mathbf{40\tau}$ and $\sim 10^{-5}$ at $\mathbf{30\tau}$. We will show that these events are far below other noise sources in a typical wireline system designed for the 56-Gbps systems.

The above observations, coupled with the relatively high preFEC BER targets in 56-Gb/s PAM-4 standards, are used to develop a relaxed specification and framework for the probability of MS events in ASARs. In turn, this relaxation enables substantial improvement of the ADC PPA.

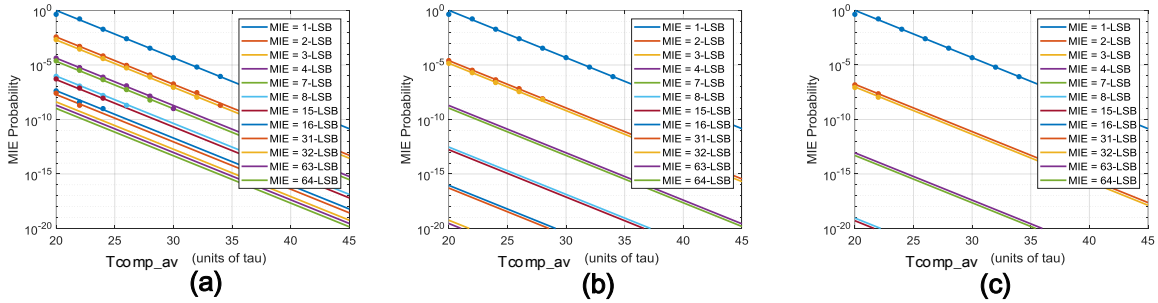

Figure 8: MIE vs $T_{comp-av}$ for (a) $T_c = \mathbf{0}$, (b) $T_c = \mathbf{5\tau}$, (c) $T_c = \mathbf{10\tau}$. ASAR ADC number of bit = 7. Solid lines are obtained by analytical approach and star markers are obtained by time-domain simulation.

B. Impact on BER and Defining the Maximum MIE

56-Gb/s backplane systems must sustain a BER on the order of 10^{-5} across a channel with bump-to-bump insertion loss of up to 38 dB. This is a far higher BER than traditionally permitted and results from the introduction of forward error correction (FEC) techniques. The overall reduction in link margin in these 56-Gb/s systems makes FEC a necessity. Several recent works [1, 2] have demonstrated that the target BER is achievable. Conversely, they also implicitly confirm that there is not excess margin on the links.

The MIE at the various error magnitudes is but one type of error amongst many in the total system. A non-exhaustive list of other error sources might include: thermal noise, quantization noise, cross-talk, distortion due to non-linearity, and inter-symbol interference. How does the MIE fit into this picture? Prior works on this subject have either designed the ADC so as to achieve very low MSE probabilities [3, 11], or claimed to integrated metastate detection and correction techniques [9, 10]. In the prior section, we showed that

the MIE is dominated by 1-LSB sized errors reaching 10^{-5} at $\mathbf{30\tau}$ and 10^{-9} at $\mathbf{40\tau}$. For comparison, we show in Figure 9 a PDF of a Gaussian noise with 1-LSB standard deviation. The ADC code transition points for an ADC subjected to this noise are highlighted. As a sole consequence of this noise, error probabilities of 1-LSB, 2-LSB, 3-LSB and 4-LSB are $\sim 5 \times 10^{-1}$, $\sim 1 \times 10^{-1}$, $\sim 1 \times 10^{-2}$, and $\sim 5 \times 10^{-4}$ respectively. In each of the comparisons, this simple case shows that the thermal noise alone dominates the error probability at the various error magnitudes. From this simple analysis we thus expect that a design can target a 1-LSB MIE of up to 10^{-2} with no significant impact on total 1-LSB error probability. The 2-3 LSB MIE remains far below at $\sim 10^{-9}$.

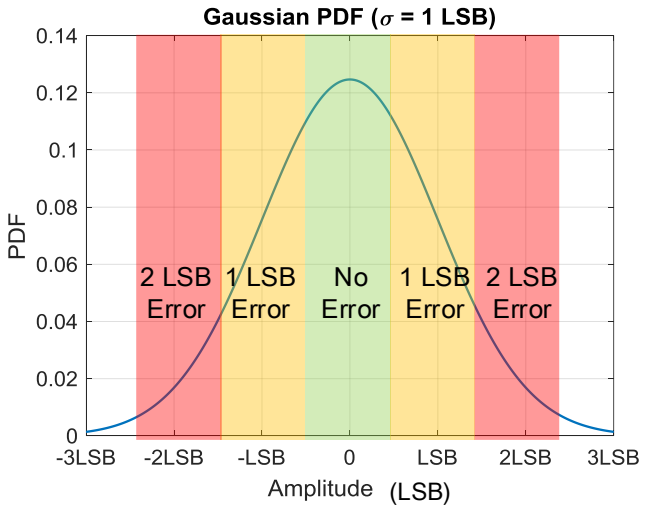

Figure 9: Gaussian noise pdf and probability of ADC code error (assuming $\sigma_n = 1$ LSB and $V_{in} = 0$)

A relaxation of the allowed error probability for errors of 1-LSB in magnitude from 10^{-9} to 10^{-2} can be achieved by slowing down the conversion of each bit. In this comparison the total extra time allotted would amount to ~20τ. Under the assumption that τ ~= 5 ps, as in [11], we receive ~100 ps. This extra time can be used to improve PPA in several ways such as reducing area by decreasing the number of interleaved ADCs. Each sub-ADC therefore operates within tighter time limits but meets the 10^{-2} target. Alternatively, the extra time can be leveraged to lower the power supply. The average conversion speed of the ADC will slow down and will yield 10^{-2} probability of LSB sized errors. Power consumption, however, will be significantly lower. In our ADC, a 100 ps change in average conversion time translates to a change of ~140 mV in power supply. Due to the dynamic nature of an ASAR, power consumption is a squared function of voltage. In other words, both supply voltage and current draw reduce. For context, consider a sub-ADC operating at 1-Gs/s which consumes 3.75 mW from a 1 V power supply. At 0.86 V it can be expected to consume ~2.77 mW or 35% less.

The relaxation scenario described above is simulated within the context of a 56-Gb/s PAM-4, 7b ADC-DSP transceiver system operating across a channel with total insertion loss of 34 dB and 42 dB, respectively. The results are shown in Figure 10. The BER and SNR

are evaluated against the 1-LSB error probability. Where, for example, the increasing probability can be attributed to a decrease in power supply level. In both cases, the target BER (preFEC) is 10^{-5}. As expected, the MIE has negligible impact on system BER and SNR at probabilities smaller than 5×10^{-2}. Note that in the extreme case where the 1-LSB MIE probability equals 0.5 (which means ADC LSB is always 0), the BER has increased 3x indicating that the least significant bit does indeed carry useful information. In other words, the same outcome cannot be achieved by simply cutting the last bit.

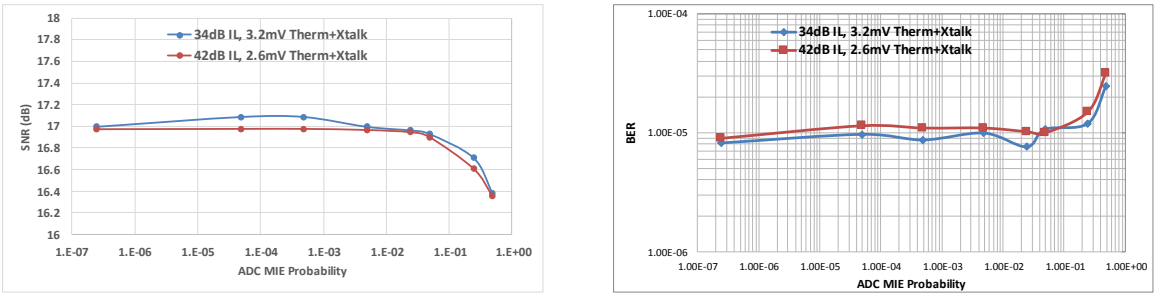

Figure 10: System SNR/BER vs 1-LSB MIE probability. SNR is at slicer input.

IV. Measurement Results

The theoretical framework presented thus far demonstrates the feasibility of increasing the probability of MIE for a typical mid-resolution ASAR deployed in a 56-Gb/s PAM-4 receiver. Next, we present measurement results of our 56-Gb/s PAM-4 SerDes transceiver operating across a channel with bump-to-bump insertion loss of 38dB. We attempt, via these measurements, to show how our total system performance is impacted by increasing the MIE.

This transceiver is implemented in 16nm FinFet and includes analog, and DSP. The transceiver is connected to a FEC module which is integrated on the same chip. The separate FEC module implements KR4 and KP4 FEC encoder and decoders. The receiver includes a CTLE followed by 32 interleaved ASAR sub-ADCs. The transmitter [12] is a PAM-4 voltage-mode driver with 3-tap FIR. The fully integrated DSP includes FFE, DFE and CDR. Our receiver features a system and method which enables direct measurement of the average conversion time for each sub-ADC. The method is described in [13].

A high insertion loss channel was chosen in order to achieve a preFEC BER near 10^{-6}. This leaves reasonable margin to the 10^{-5} limit and is sufficiently low so as to ensure that the system remains sensitive to extra additive noise. The transceiver performance (e.g. pre-FEC BER) is assessed across a range of SAR power supply voltages. The supply voltage to the SAR is swept from 0.95 V to 0.85 V in order to slow conversion. As presented earlier, this increases the probability of MIE. The results are shown in Figure 11. Note that the performance of the link is compared with the ADC in 6-, and 7-bit modes. The 6-bit mode is analogous to having a 50% probability of MIE on the 7th bit. The 6-bit mode shows ~4X worsening in BER confirming the effectiveness of this bit under these conditions.

Furthermore, the 7-bit mode shows no change in BER across the voltage sweep indicating that it is not impacted by the related increase in the average conversion time.

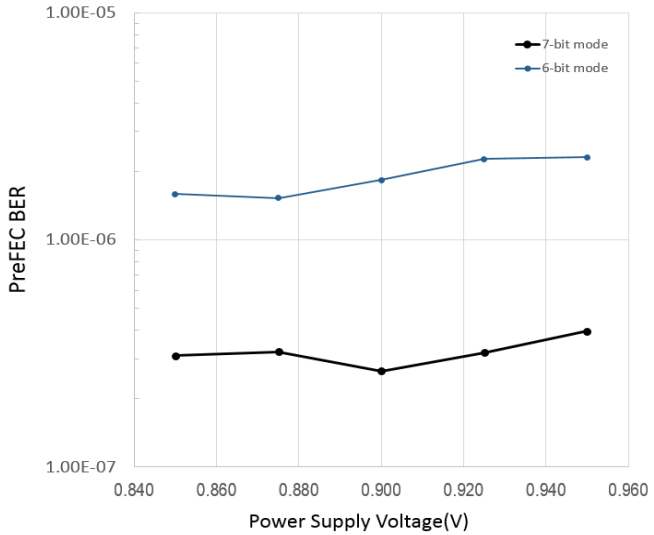

Figure 11: Pre-FEC BER vs Power Supply Voltage. 56-Gb/s, PAM4, IL 38 dB.

The ASAR average conversion times over the supply voltage sweep are shown in Figure 12 for the 7-bit mode. These average conversion times are averaged over numerous conversions and across all 32 sub-ADCs. The conversion times are measured directly from each of the sub-ADCs.

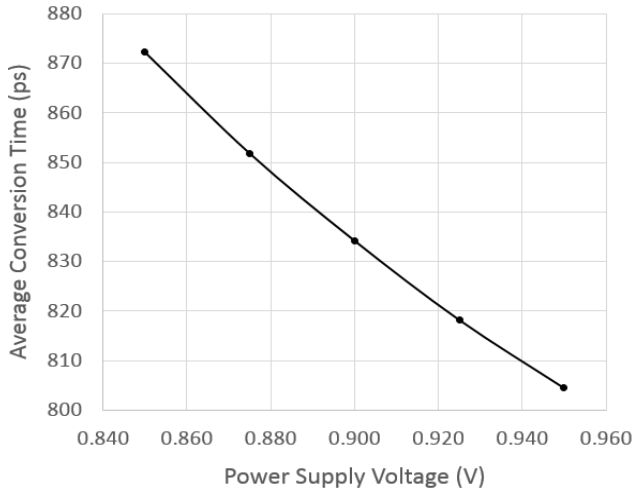

Figure 12: ASAR Average Conversion Time versus power supply voltage in 7-bit mode.

The average conversion time is clearly a function of the power supply level. Faster average conversion times are achieved with high supply voltages reaching ~805 ps at 950 mV. On average, conversion time slows by ~70 ps from 950mV to 850mV resulting in a sensitivity of ~0.7 ps/mV. The power consumption of the 32 ASARs is reduced by ~25 mW at 850 mV compared to 950 mV.

The noted increase in average conversion time reduces the time available for long regeneration times and thus increases the probability of a MS event. We estimate that 70 ps represents a change equivalent to ~16τ (from 40 τ total budget) yielding an available time of ~24τ with related probability for 1-LSB magnitude MIE of $\sim 10^{-2}$. Finally, we remark that the total pre-FEC BER remains unaffected and well below the 6-bit reference.

V. Conclusion

The problem of comparator metastability was investigated within the context of 56-Gb/s transceivers. There transceivers typically feature high-speed interleaved ASAR ADCs, and are intended to operate over links that include forward error correction (FEC) as an integral part of the system. We studied this problem with an interest in leveraging FEC to improve the power, performance, or area (PPA) of our ADCs. We've developed a methodology for analyzing the probability of metastate induced errors (MIEs) of various magnitudes and showed that errors of small magnitude dominate. Furthermore, we noted that errors with magnitude larger than 3-LSB have probabilities below the link BER target. Our analysis indicated that our system can tolerate very high probability of LSB size errors which in turn could be leveraged to improve PPA. From example, we estimated that power can be reduced by ~25% (with no impact to BER) by adjusting LSB error rate from 10^{-9} to 10^{-2} .Finally, we demonstrated validity with full link-level time domain simulations and BER measurements from our 56-Gb/s transceiver communicating over a link with insertion loss of 38 dB.

References

[1] P. Upadhyaya, et al., “A Fuly Adaptive 19-to-56Gb/s PAM-4 Wireline Transceiver with a Configurable ADC in 16nm FinFet,” ISSCC, 2018, pp. 108-109.

[2] K. Gopalakrishnan, et al., “A 40/50/100Gb/s PAM-4 Ethernet Transceiver in 28nm CMOS,” *ISSCC*, 2016, pp. 62–63.

[3] Y. Frans, J. Shin, L. Zhou, P. Upadhyaya, J. Im, V. Kireev, M. Elzeftawi, H. Hedayati, T. Pham, S. Asuncion, C. Borrelli, G. Zhang, H. Zhang, K. Chang, "A 56-Gb/s PAM4 wireline transceiver using a 32-way time-interleaved SAR ADC in 16-nm FinFET", IEEE J. Solid-State Circuits, vol. 52, no. 4, pp. 1101-1110, Apr. 2017.

[4] S. Hashemi, B. Razavi, "Analysis of metastability in pipelined ADCs", IEEE J. Solid-State Circuits, vol. 49, no. 5, pp. 1198-1209, May 2014.

[5] C. H. Chan, Y. Zhu, S. W. Sin, B. Murmann, S. P. U, and R. P. Martins, "Metastablility in SAR ADCs, " IEEE Trans. Circuits Syst., II, Exp. Briefs, vol. 64, no. 2, pp. 111–115, Feb. 2017.

[6] A. Waters, J. Muhlestein, U. K. Moon, "Analysis of metastability errors in conventional LSB-first and asynchronous SAR ADCs", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 11, pp. 1898-1909, Nov 2016

[7] A. Waters, J. Muhlestein, U.-K. Moon, "Analysis of metastability errors in asynchronous SAR ADCs", Proc. IEEE Int. Conf. Electron. Circuits Syst. (ICECS), pp. 547-550, Dec. 2015.

[8] S. Cai, A. Shafik, S. Kiran, E. Z. Tabasy, S. Hoyos, S. Palermo, "Statistical modeling of metastability in ADC-based serial I/O receivers", Proc. 2014 IEEE 23rd Conf. Electrical Performance Electronic Packaging and Systems, pp. 39-42.

[9] J. Yang, T. L. Naing, R. W. Broderson, "A 1 GS/s 6 bit 6.7 mW successive approximation ADC using asynchronous processing", IEEE J. Solid-State Circuits, vol. 45, no. 8, pp. 1469-1478, Aug. 2010.

[10] S. Cho, et al., “A Two-Channel Asynchronous SAR ADC With Metastable-Then-Set Algorithm”, IEEE Transactions on VLSI Systems, pp. 765-769, April 2012.

[11] L. Kull, T. Toifl, M. Schmatz, et al., "A 3. 1mW 8b 1. 2GS/s Single-Channel Asynchronous SAR ADC with Alternate Comparators for Enhanced Speed in 32nm Digital SOI CMOS," ISSCC Dig. Tech. Papers, pp. 468-469, Feb. 2013.

[12] L. Wang, Y. Fu, M. LaCroix, E. Chong, A. C. Carusone, "A 64Gb/s PAM-4 transceiver utilizing an adaptive threshold ADC in 16nm FinFET", IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp. 110-111, Feb. 2018.

[13] M. LaCroix, et al., “A 60Gb/s PAM-4 ADC-DSP Transceiver in 7nm CMOS with BER-Based Adaptive Power Scaling Achieving 6.9pJ/b at 32dB Loss”, ISSCC, Feb. 2019.