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Electrical Integrity for LPDDR5 Memory Technology

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Abstract

LPDDR5 is emerging memory for Low Power small form factor electronic design systems. LP power delivery operating range is getting reduced in subsequent generations. Also, the signal integrity requirements are also getting stringent as the speeds of the operation are increasing. It is becoming challenging to system design engineers to comply to the JEDEC specifications. In this paper we describe the specification trends and various techniques that can be used to meet electrical requirements including power integrity, signal integrity, thermal integrity, power and performance.

Author(s) Biography

Vishram Pandit is currently a Technologist at Intel, Bangalore, working on Power and Signal Integrity, EMC for chip/package/PCB. Prior to that, he was a technical lead in Client Power Integrity and EMC Group, Intel Santa Clara. He is a co-author of a book "Power Integrity for I/O Interfaces," published by Prentice Hall. He has co-authored numerous papers in external conferences and Intel internal conferences.

Aiswarya Pious is currently System Architect at Intel, Bangalore, working on system and platform designs for next generation reference platform designs for Intel SoC intercepting new technologies. She also handles memory platform architecture

Prabhat Ranjan is currently Signal Integrity Engineer at Intel, Bangalore, working on Signal integrity for package/PCB design for Client Computing Products. His work focuses on the signal integrity modeling, simulation and analysis for latest memory technology.

Arvindh Rajasekaran is a Power Management Systems Architect responsible for definition, architecture, product development and commercializing in-house PMICs at Intel.

Kirankumar Kamisetty is a senior Analog Engineer at Intel, Oregon USA, responsible for designing the cost and performance optimized power and signal integrity solutions for Client computing products and enabling new memory technology solutions on Client platforms.

Jun Liao is a technical lead for memory subsystem electrical design at Intel Hillsboro, working on new technology definition, simulation methodology and tools development, and client product design. Previously, Jun was senior engineer at Altera. He published more than 30 papers and hold 10 US patents. Jun received his Ph.D. in electrical engineering from Rensselaer Polytechnic Institute at Troy, New York

Nagi Aboulenein is a lead client memory system architect at Intel Oregon. He has led memory system architecture for a number of Intel client and device SOCs, and holds a number of patents in memory controller architecture and design.

Christopher Cox is a memory design architect at Intel Folsom. He has been involved in memory for almost 20 years, is a significant contributor to most of the JEDEC DDR/LPDDR standards and currently focused on LPDDR5 and DDR5 development. Cox holds numerous patents on memory technologies.

Introduction

Low Power Dual Data Rate (LPDDR) memory has been popular in low power devices such as handheld, smartphones, tablets, and low power notebooks. LPDDR2 specification first ratified by JEDEC in 2010. In 2012 JEDEC published first LPDDR3 spec, and in 2014 LPDDR4 was introduced. LPDDR4x was introduced in 2016 and LPDDR5 spec will be published by JEDEC in 2019. Table 1 shows the speed comparison for these memories

	LPDDR2	LPDDR3	LPDDR4	LPDDR4x	LPDDR5*
JEDEC Spec	2010	2012	2014	2016	2019
Speed (MTPS)	1033	2133	4267	4267	5400-6400*

Table 1 Features of LPDDR memories

*JEDEC specification is not published yet, so we are just showing the trend.

Electrical System

LPDDR5 electrical system representation is as shown in the following diagram.

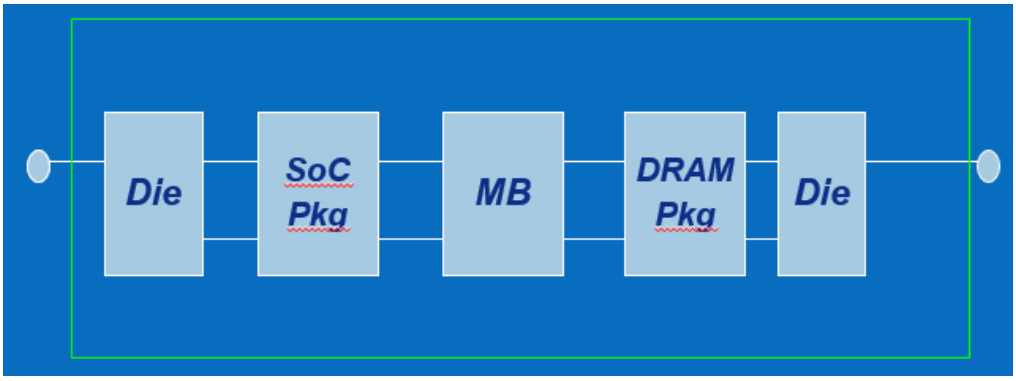

Figure 1 Block Diagram for SoC and LPDDR

The figure shows the SoC LPDDR5 die, pkg and then Motherboard (MB). This particular implementation shows BGA down version for the LPDDR5. The LPDDR5 package is shown to be connected to the motherboard.

There are two major power domains for the LPDDR5 memory, one is VDDQ or final stage driver/ receiver power domain and the other is VDD2 or DRAM core stage power domain. The system designers need to meet the JEDEC specifications for these domains discussed in the next section

Power Delivery

Table 2 shows LPDDR memory voltage requirements and termination scheme for the final stage.

	LPDDR2	LPDDR3	LPDDR4	LPDDR4x	LPDDR5*
Final stage voltage (V)	1.2	1.2	1.1	0.6	< 0.6
DRAM Vdd2 core voltage (V)	1.2	1.2	1.1	1.1	< 1.1
DRAM Vdd1 voltage	1.8	1.8	1.8	1.8	1.8
Final stage termination scheme	Unterminated	Unterminated/ power terminated	Ground termination	Ground termination	Ground termination*
Speed (MTPS)	1033	2133	4267	4267	5400-6400*

Table 2 LPDDR Specifications for different generations

*JEDEC specification is not published yet, so we are just showing the trend.

Figure 2 shows the JEDEC specifications for the VDDQ voltage requirements (Vim and Vmax) from LPDDR2 to LPDDR4x.

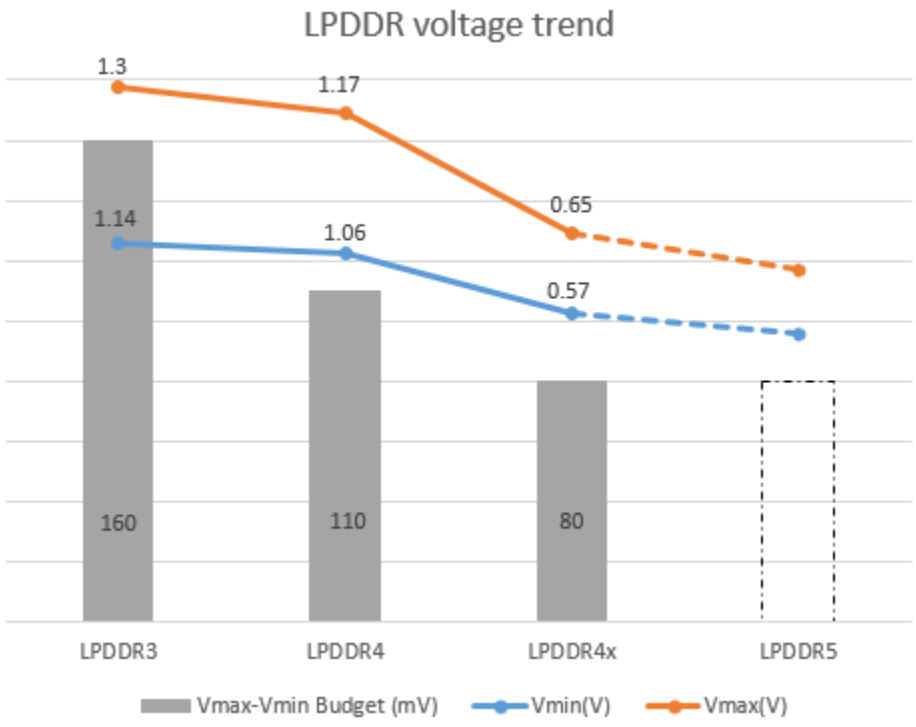

Figure 2 LPDDR voltage trends

As shown in the graph the VDDQ min to max voltage is decreasing generation over generation (LPDDR3 to LPDDR4x) to save the power. LPDDR5 Vmin-Vmax voltage estimates are projected based on the trend. In order to meet these specification for LPDDR5 carefully design for different components including PMIC, PCB and DIMM card needs to be done.

PMIC/regulator DC accuracy, ripple:

The voltage set point at the regulator is depends on DC and AC components and the DC component further comprises of DC losses on board and package in addition to the DC accuracy of the voltage regulator. Since the regulation point can change with process, voltage and temperature, choosing a regulator with low DC variation has a direct impact on the ability to meet the JEDEC spec at the memory ball and lowering power by setting it as low as possible.

PMIC/regulator load transient response:

The inherent nature of DDR loads is bursty and hence there is a corresponding load transient that the voltage regulator/PMIC will have to support. Understanding the worst case load transient possible is the first step in determining how to deal with it. The voltage budget assigned to transient dip and overshoot must be planned so that the final JEDEC specification is still met. In order to lower the voltage excursion due to a load transient there are several voltage regulator techniques popular in the industry today and it is usually a trade-off between transient performance, spectral content and amount of board capacitance used.

Popular VR architectures employ automatic transitions between a high performance mode (eg.PWM) and a high efficiency mode at light loads (eg.PFM) to deliver optimal efficiency across load conditions. This however usually implies worse transient performance when transitioning between these modes and can impact power adversely if the voltage has to be set higher to compensate for the larger dip in auto-mode of the regulator.

Stack up of the PCB, and power shape routing:

Losses on the board must be minimized in order to lower power and meet the JEDEC voltage specifications. The PCB must be designed carefully and the requirements to accomplish low path losses must be understood while deciding the stack-up and routing. Often, the DDR location is such that it is placed to optimize for signal integrity and power delivery into that section of the PCB is challenging. In order to meet impedance targets, the materials used, copper thickness and board shapes must be chosen accordingly. Type 4 PCB with buried/ blind vias can be used for reducing the losses.

PMIC/regulator placement:

The distance from PMIC to the memory directly impacts the impedance irrespective of stack-up and conductive materials and so it is important to plan the placement of the PMIC and the regulator so as to minimize losses. If the application permits, a dual sided placement is beneficial allowing power to be delivered to the DDR from the other side of the board. This however may not always be a possibility due to OEM requirements on form factor and cost.

Power Integrity

For power integrity analysis, end-to-end system models are put together and frequency domain and time domain analysis is performed. The following section focuses on DRAM side analysis.

DRAM Die

While LPDDR DRAM die and package models are not commonly available via the web, they are available upon request under NDA. Figure 3 shows an example of an equivalent PDN model for the LPDDR die.

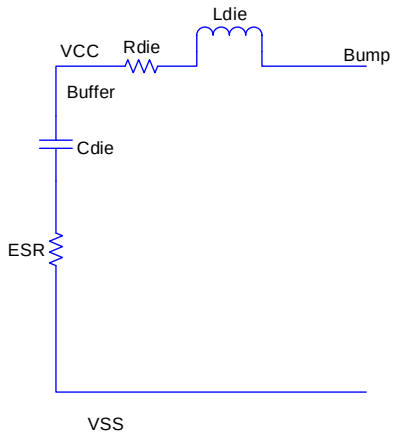

Figure 3 Equivalent PDN model for the LPDDR die

- On-die capacitor
    - Cdie: On-die capacitance
    - ESR: Resistance series to the cap. (see earlier presentations)
- Power Grid:
    - Ldie: Power grid inductance
    - Rdie: Power grid resistance

  Please note ESR and Rdie are separate. DRAM vendors may have monolithic or stacked die model.

Package Model

Without going into supplier specific parameters, a generic methodology is described in the following section. It shows the package model elements such as solder ball and bondwire. Quasistatic electromagnetic simulations can be done on the package layout and we can extract the resistance and inductance for the package.

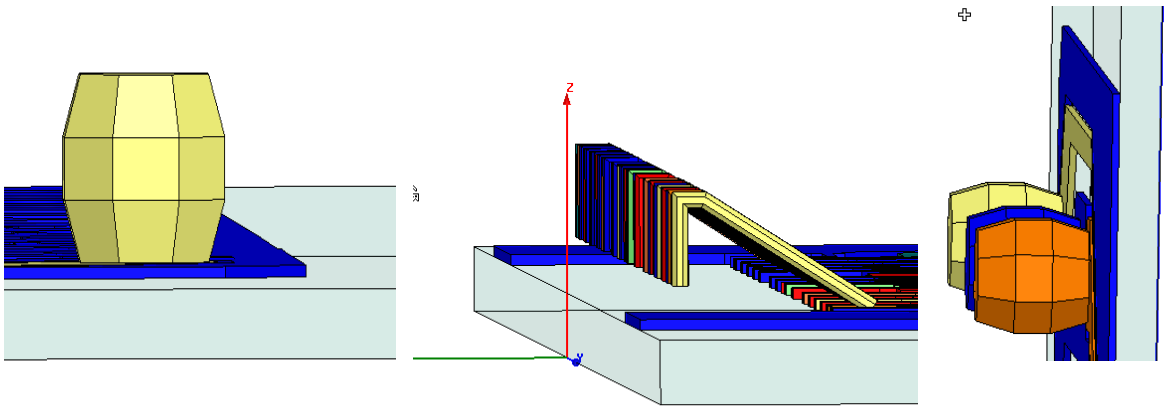

Figure 4 BGA balls and Bondwire modeling

The number of BGA/bondwires assigned to VddQ and Vdd2 and ground will determine the equivalent R and L. It is desirable to reduce the R and L and assign more BGA/bondwires as possible. For Signal Integrity, this R and L will play important role at higher speeds.

Impedance profile for the DRAM

Although, the R and L are extracted for the DRAM model, for system level simulations, S parameters are used. Similar to the DRAM model, the motherboard model is simulated with quasistatic 3D or planar 3D solver and the S parameter model is generated. For the impedance analysis, die, package and motherboard models are put together are simulated.

Figure 5 shows the self-impedance plot for a generic DRAM. It shows two domains VddQ and Vdd2. There are some variations in the package and the die and optimized model with lower impedance is plotted.

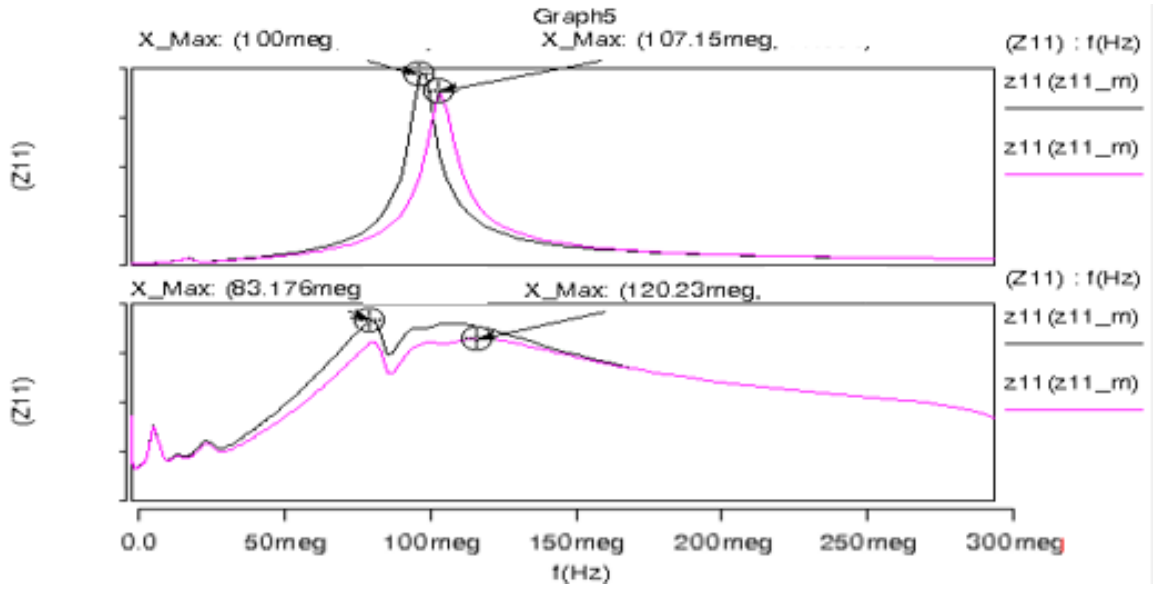

Figure 5 Self Impedance for VddQ and Vdd2 domains

It should be noted that there is supplier, process, die config, fab variation (in order of typical impact) and designs should take that into consideration. In this example, the resonance frequency is shown to be around 107Mhz for VddQ domain and around 120MHz for Vdd2 domain.

Final stage currents VddQ

Figure 6 shows the final stage current and noise simulation setup for the DRAM. There is a channel considered for the PDN simulations. At the buffer there are three currents: current from power to central node where transmission line is connected, current to ground from that node, and third one is final stage current

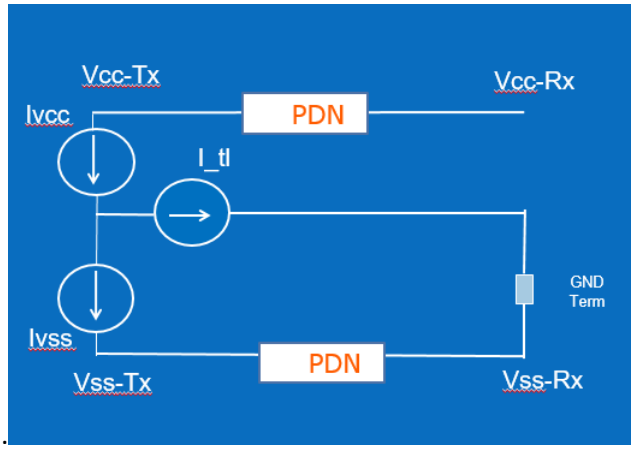

Figure 6 Final Stage Current for LPDDR

Noise simulations

Since LPDDR5 information is not publically available, we cannot comment on actual excitation profiles, but users can speculate based on commonly known info or such. Some approximations are used and noise simulations are done for establishing the methodology. Here, the termination is at the ground. Current profiles are injected on the PDN model and noise simulations are done.

Figure 7 shows noise simulations at the LPDDR5 DRAM side, when the SoC is transmitting. There is termination to the ground, so there is no direct power to ground current. However, there is a current from transmission line to the ground. For this simulations, planar 3D electromagnetic time domain solver is used. Transmission lines are used along with the power and ground structures. Currents are injected and we see noise across power and ground (shown in blue) for the DRAM.

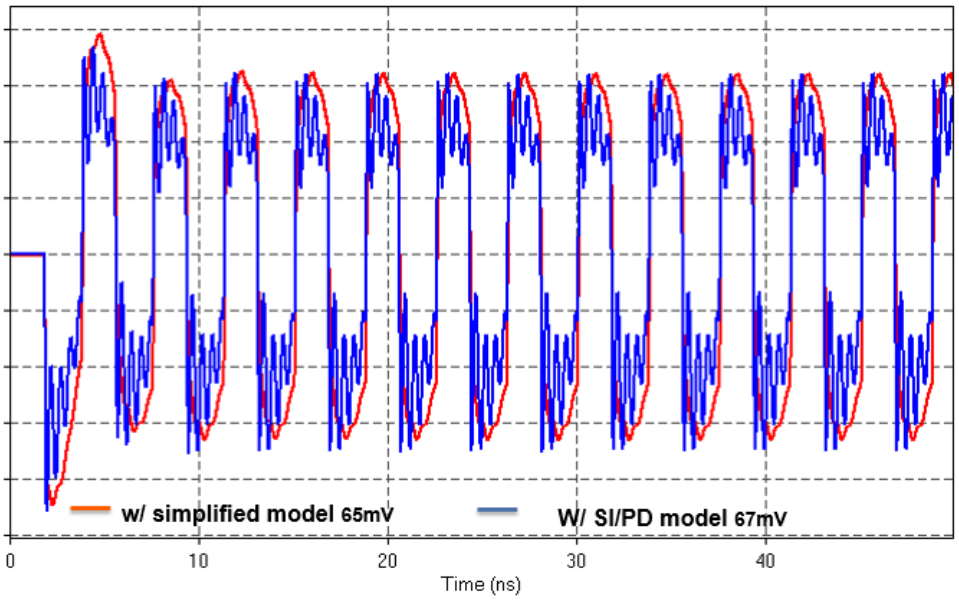

Figure 7 VddQ noise simulations at DRAM

It is difficult to use planar 3D electromagnetic solver with transmission lines every time we had to do Power integrity simulations. Therefore, an equivalent methodology is established. Using some scaled current of transmission line to ground, another current is derived from power to ground (at the DRAM) based on the decoupling capacitors. This current is injected from power to ground and the noise produced is shown in red color in Figure 7. The current magnitude is adjusted to match with the noise simulated earlier with transmission lines. In Figure 7, both the simulations show similar magnitude, but the noise signature is significantly different. Transmission line based PDN simulation results show much high frequency content. This illustrates that the entire system needs to be simulated for the LPDDR5 PDN analysis and we cannot ignore the ground current impact. It is to be noted that the noise amplitude of 65mV is for generic example and levels may change dependent on the parameters.

Motherboard MEMORY RAIL PDN design

Recommended DC Operating Conditions

DRAM	Symbol	Min	Typ	Max	Unit	Notes
Core 1 Power	V_{DD1}	1.70	1.80	1.95	V	1,2
Core 2 Power/Input Buffer Power	V_{DD2}	1.06	1.10	1.17	V	1,2,3
I/O Buffer Power	V_{DDQ}	0.57	0.6	0.65	V	2,3,4,5

NOTE 1 V_{DD1} uses significantly less current than V_{DD2}.

NOTE 2 The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz at the DRAM package ball.

NOTE 3 The voltage noise tolerance from DC to 20 MHz exceeding a pk-pk tolerance of 45 mV at the DRAM ball is not included in the TdIVW.

NOTE 4 V_{DDQ}(max) may be extended to 0.67 V as an option in case the operating clock frequency is equal or less than 800 Mhz.

NOTE 5 Pull up, pull down and ZQ calibration tolerance spec is valid only in normal V_{DDQ} tolerance range (0.57 V - 0.65 V).

Figure- 8: LP4x PI SPEC (Source: JEDEC LPDDR4x BALLOT, Item # JC-42.6-1831.55)

For LPDDR4x, DRAM Voltage noise bandwidth SPECs are defined at the DRAM BGA ball from DC to 20 MHz (Figure-8). The bandwidth/Max frequency is generally a consensus between the DRAM vendors and JEDEC Members. DRAM vendors publish the IDD numbers but there is no easy way to derive the Icc(t) at the DRAM DIE/BGA. Designing an efficient MB PDN will require the DRAM PKG PDN, DRAM CDIE/RDIE, Die level Icc(t) or a de-rated Icc(t) at the DRAM BGA ball. Without this information we potentially end up over/under designing the platform. While we can get the Icc(t)/DRAM PKG information from some vendors, it is not representative of the industry and we cannot rely on this information to design the MB PDN.

Here is an example (Figure-9) showing the difference in the Voltage noise seen at the DRAM BGA with/Without DRAM DIE/PKG PDN. (Note: DRAM DIE/PKG PDN is not a representative of any Vendor. It's an estimation based on commonly known information).

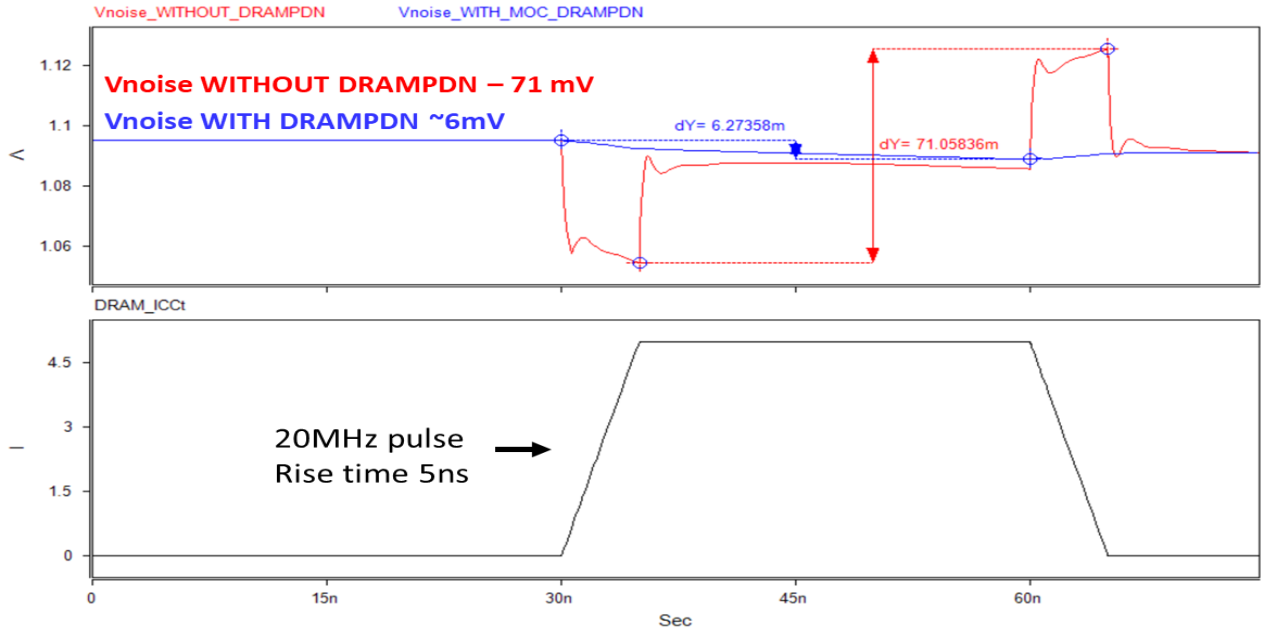

Figure- 9(a): VDD2 Voltage noise waveform

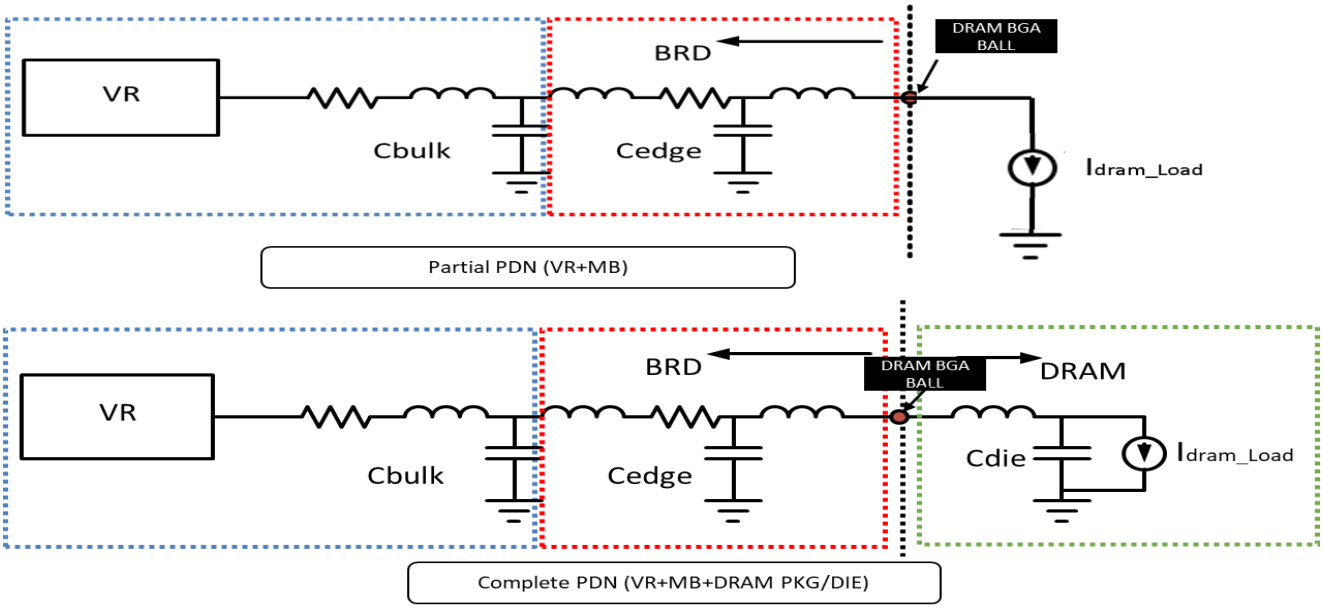

Figure- 9(b): Power Delivery Network

As illustrated above, PI analysis with the same Icc(t) done with/without DRAM PKG/DIE PDN, we see a different Voltage noise at the DRAM BGA. The voltage noise that we see at the bump heavily depends on the DRAM DIE/PKG PDN and Icc(t). Our PI design approach, to meet the PI specs, involves using a mock up DRAM PDN and/or using a 20 MHz low pass filter at the DRAM BGA.

While it is desirable to have a JEDEC published SPEC on DRAM PDN, We understand that some of this information is proprietary/IP and cannot be shared. For LPDDR5, we are proposing an impedance target SPEC in addition to the voltage noise bandwidth SPEC (Note: This is currently being discussed in the JEDEC). This will provide a clear design target for the MB PDN and removes ambiguity. This will also provide a test bench for the DRAM vendors to design their package.

Packaging solutions

LP4/4x BGA packages are available in x32 and x64 bus widths in FBGA and BGA for POP packages. This section discusses the design methodology to allow laptop designers to compress and design smaller compact motherboard designs with the POP BGA down on the motherboard, which in-turn gives advantage of better battery volume (and hence capacity) available for the system.

The phasing out of LP4x and entry of LPDDR5 is mainly driven by 2 factors

- Power savings achieved with LPDDR5
- Industry moving towards LPDDR5 due to phone market volume and demand

Given this, it is expected that the first industry enabled package would be a POP BGA device rather than a discrete FBGA. Due to the delay in enabling the actual BGA package for laptop like devices, the design methodology mentioned for LPDDR4x POP can be followed for LPDDR5 also allowing PCB designers to design the motherboard designs with LPDDR5 technology to take advantage of the power benefits for overall system.

POP packages

Need for POP packages – the case of form factor and power : While the name POP (Package on Package) implies that this BGA device will be used on top of another device such as an SOC, it can also be used as a direct attach to the motherboard, allowing the system designer to take advantage of the cavity for breakin vias. The high volume of phone market is one of the primary reasons as to why LPDDR5 POP package is popular. At the same time, upcoming form factors for converged mobility, which bridges the gap between a phone and a PC, bringing in companion type use cases are all thin and sleek devices. With a thin and sleek system, the cooling technology used needs to be fanless, which puts a restriction on the overall power that can be sustained within the system.

PCB type: Traditional BGA packages allow both type 3 and type 4 (High Density Interconnect or HDI) breakout motherboard designs. POP package allows customers to do type 4 (High Density Interconnect or HDI) motherboard designs which allow OEMs to design compact motherboards

Total system power = sum total of each of the subsystems, SoC being the major contributor along with memory & storage and connectivity subsystems.

Table 3 shows details of LPDDR4x POP package and design considerations for device down implementation.

LP4x POP package	Ballmap	No of balls	SRO size	Joint size
	No balls on center area	556b	240um	200um
	Balls spread across entire area	178b	260um	220um

Table 3 LPDDR4x POP package and design considerations

Design considerations for POP packages:

Due to above differences, when POP package is soldered down on the motherboard it experiences more stress and strain due to thermal cycling as compared to the discrete BGA. Design considerations to negate the above risk: Use corner glue on all 4 corners of the package for assembling the POP package on motherboard. The fillet length and width dimensions have been worked out for a 12.4x12.4 LPDDR4 POP package as shown in Figure 10.

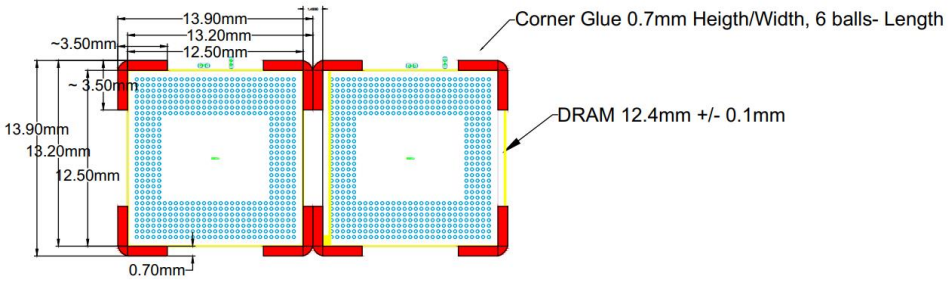

Figure 10 LPDDR4x POP package example

Standard packages

Standard packages which are under definition in JEDEC, will require platform considerations on power & signal integrity (details in SI/PI section) but no separate reliability concerns.

Signal Integrity

Low Power DRAM technology is evolving to the fifth-generation (LPDDR5) to deliver significant reduction in power and extremely high bandwidth as compared to LPDDR4. In this section we discuss the proposed trends for LPDDR5 which impacts overall memory channel electrical performance.

LPDDR5 DRAM is expected to have data rate upto 6400 megabits per second which is 1.5x faster than the existing LPDDR4x based on the JEDEC specifications trend [figure-11a]. Based on [figure-11b] one can project that for LPDDR5, the final stage voltage is going to decrease and DRAM pad capacitance is going to be equal or lower. Since the specifications are not published, we are projecting/ estimating the values for Signal Integrity analysis and recommendations.

LPDDR Electrical Spec Evolution

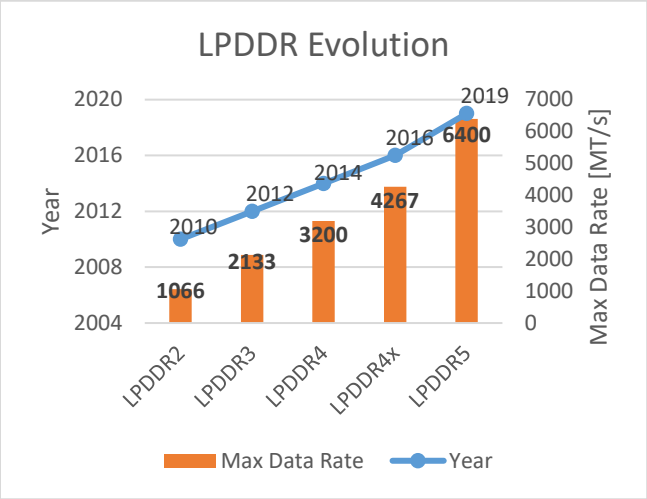

Figure-11a LPDDR chronology

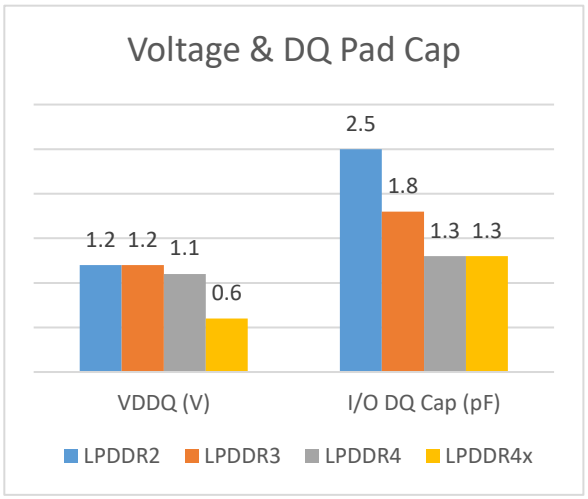

Figure-11b LPDDR voltage and padCap

Electrical Specification differences:

Below [Table-4] is the comparison between LPDDR4x & LPDDR5 signals based on max operation speed.

Item	LPDDR4x	LPDDR5 *
Data Rates(max)	4.2Gb/s	Up to 6.4Gb/s
Voltage(VDDQ)	0.6V	<0.6
Write Sampling Edge	DQS	WCK
Read Sampling edge	DQS	RDQS
DRAM I/O Capacitance (DQ & DM)	Upto 1.3 pF	<1.3pF

Table-4 Electrical specification comparison for LPDDR4X and LPDDR5

*JEDEC specification is not published yet, so we are just showing the trend.

LPDDR5 DRAM Rx Mask:

To achieve the higher speed, LPDDR5 DRAM Rx mask requirement to be redefined. Current LPDDR4x Data Rx mask is a rectangular mask with 120mV height & 0.25*UI as width. Since UI (Unit interval) of data lines for LPDDR5 has reduced significantly for 6.4Gb/s, a different mask with lower height & width requirement will be essential for these lines.

Impact of Increased Speed of LPDDR5 on Memory Channel

Since data rate gets increased up to 6400Gbps, the bit Unit Interval shrinks and memory channel ISI (inter symbol interference) and crosstalk impact increases drastically. This is because the electrical

channel length requirements of memory interface would remain the same as the SoC and DRAM placement strategy and the package dimension not changed notably.

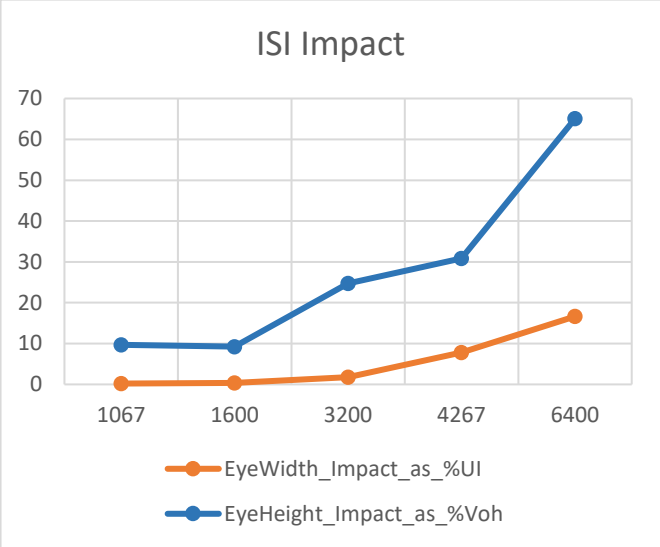

Figure-12a LPDDR5 ISI

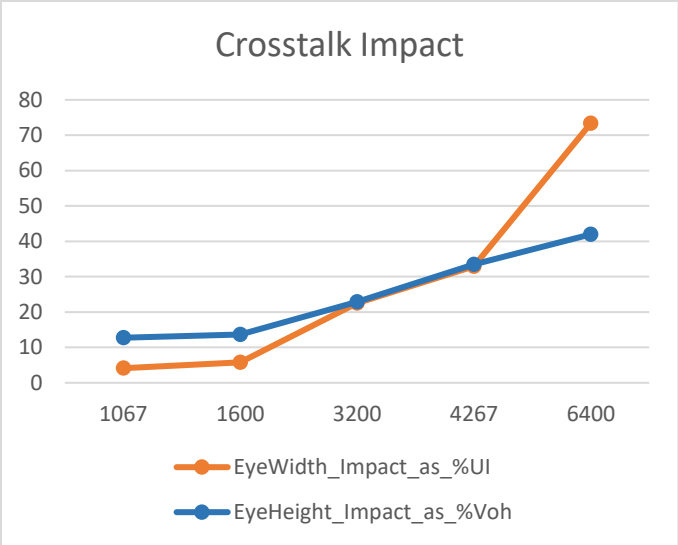

Figure-12b LPDDR5 Crosstalk

Eyewidth_Impact_as_%UI : Eye width loss due to ISI or crosstalk as % of UI
EyeHeight_Impact_as_%Voh: Eye height decrease due to ISI or Crosstalk as % of Voh measured with CPU Ron & DRAM ODT

As explained in the above graph [figure-12a/12b], the impact of both ISI and crosstalk at 6400 Mbps transfer have increased significantly. This could result in lot of memory channel performance issue and making the channel design very challenging to meet this speed targets. So to enable the LPDDR5 interface at 6400 Mbps, memory channel design has to include strategy to improve both ISI as well as crosstalk. Equalization in the channel is critical to enable LPDDR5 targeted speed.

Memory Channel design recommendation for ISI improvement:

Package & Motherboard :

a. Reduce the overall routing length as much as possible. As LPDDR5 is running at much higher frequency then previous generation memory, the low pass filtering effect of channel is greatly impacting link margin. It's observed that voltage AC swing at receiver side is much smaller than LPDDR4, and raising driver supply voltage for high speed signalling is not as beneficial as we observed at lower speed. Any design practice that helps to reduce channel effective loading will boost signal swing.
b. Package & Motherboard impedance need to be optimized along with whole channel. Initial analysis is showing that package & motherboard single ended impedances around 35Ohms-to-40ohms are optimum for LPDDR5 channel.
c. Improve the impedance discontinuity in memory channel for constant impedance. Impedance mismatch due to fan-out/in region routing, via (package & Motherboard) & ball (package) impact the overall significantly.

d. Fan-out/in impedance mismatch can be reduced by using thinner dielectric layer or using different routing strategy like inductive coupling.
e. Control the via impedance by controlling the via & anti-pad size. HDI board can be used for controlling the via length.
f. For increasing the solder ball impedance, shadow voiding at adjacent layer can be used.
g. Reduce the length of routing under fan-out/in region if impedance mismatch can be avoided.

Memory Channel design recommendation for Crosstalk improvement:

Package & Motherboard :

a. Use low crosstalk routing strategy like stripline/inner layer routing of package & mother board. Microstrip routing will not only cause crosstalk issue, but also generate undesired radio frequency noise. As LPDDR5 speed is close to various WiFi and 5G frequency band, stripline routing is required to minimize any radiation interference from platform.
b. Optimize the package & motherboard stackup for thinner dielectric thickness. This is very essential to reduce the crosstalk in fan-out/in region. See the below graph [figure-13] for dielectric thickness impact on crosstalk coefficient.

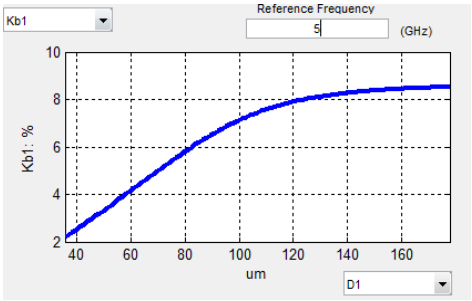

Figure-13 Dielectric thickness vs. Crosstalk Coefficient

c. As crosstalk is roughly linearly correlated to reflection in the channel, in some platforms, we can remove main route section and just use the same fan-out routing to connect SOC and DRAM. Since there is no impedance change along the channel, refection is minimized, which helps to reduce back and forth accumulative crosstalk.
d. Provide good isolation between signal vias. Maintain 1:2 ground-signal via ratio.
e. Provide good isolation between different signal groups (DQ-CAC-CLK) and also between different channels.
f. Different routing strategy like stubby routing or introducing capacitive coupling can be used to reduce the far-end crosstalk in channel.

Power-and-Performance

The biggest benefit in moving towards next generation of LPDDR technology is the power saving, which adds benefit to overall battery life of the system.

As evident graph in Figure 14 (Power comparison for Graphics workload), LPDDR5 targets 25-30% less power than LPDDR4x at iso-frequency. Please note that this is what DRAM suppliers are targeting and that actual product measurements to verify those targets won't be possible until representative DRAM parts are available.

Figure 14 (Graphics performance comparison) shows the comparison in a thermally constraint system

X-axis (1) and (2) are representatives of LPDDR4x and LPDDR5 normalized power at iso frequency. The expected power delta is shown

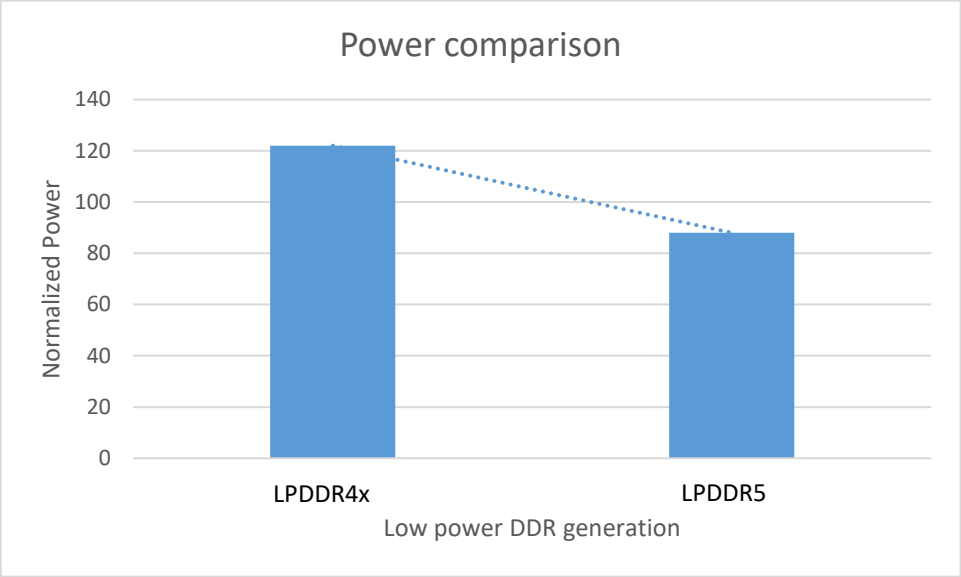

Figure 14. Performance comparison between LPDDR4x and LPDDR5

Factors impacting performance:

Impact of capacity on performance

Performance benchmarks drive minimum memory capacity for a platform. For example a benchmark SPEC17 MT requires 2GB/copy defined by the Operating System. Performance KPIs (benchmark scores) do not depend on memory capacity provided minimum capacity is met. Eg., Graphics workloads viz., 3DMark, Manhattan etc depend on GT frequency and DDR bandwidth. Similar case with CPU workloads viz., SPEC. Concurrent APPs/use cases assumed same between OS-DT and OS-A for minimum memory capacity analysis without impact to user experience. Increasing Memory capacity does not increase performance in the Graphics/CPU benchmarks

Impact of 1R vs 2R on performance

On a relative comparison between dual rank and single rank devices, 2R devices perform much better with Graphic workloads viz., Manhattan. For eg., Manhattan scores degrade by ~3% for 128b memory while using 1R devices. While CPU benchmark (SPEC) scores degrade by ~0-1% for 128b memory while using 1R devices. This concludes that there is minimal performance impact on CPU/ benchmark as we move from dual rank to Single Rank

Impact of bandwidth on performance

- Another critical factor affecting performance is the overall bus width. On a relative comparison, the graphics workloads performance drops when the data bus width on the SoC reduces from a x128 to a x64

Summary

Based on the available/projected information on LPDDR5 we have listed the trends. We have illustrated the system level design options for achieving Power Integrity, Power Delivery, Signal Integrity, Power and Performance requirements for the LPDDR5 systems.