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A Review of Combiner/Divider PCB Design Topologies For 5G and WiGig ATE Applications

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Abstract

The new 5G and Wigig standards present new challenges for the test and measurements of integrated circuits for those applications. The main challenges are the very high frequencies (e.g. as high as 44 GHz for 5G and 72 GHz for WiGig) and also the large number of ports (e.g. 16 to as many as 64) due to the use of phase array antennas in these standards and the need to support multiple standards/frequencies in a single IC.

Since these integrated circuits are intended for the consumer market, cost of test is a critical factor. This means that for volume production testing, it might be advantageous to combine the multiple RF ports into a single port that can then be measured with a single measurement instrument port. This is sometimes referred to as a “corporate feed” in the automated test equipment (ATE) community.

This approach would allow an ATE system with multiple measurement RF ports to test multiple integrated circuits in parallel and in this way reduce to cost of test. This approach is only valid for integrated circuits at wafer level or in packages that have no integrated antennas. For 5G and WiGig applications there are devices that have the phase array antennas integrated for example in the package. In these cases, an over the air (OTA) testing approach is necessary which is not addressed in this paper.

Authors' Biographies

Giovanni Bianchi (R&D Engineer) received the Laurea degree in Electronic Engineering from the University of Rome "La Sapienza", Rome, Italy, in 1987. In 1988, he joined the Microwave Department of Elettronica S.p.A. where he was involved in and later responsible for microwave components (including GaAs MMICs) and subassembly design. He joined Motorola PCS in 2000, where he worked on GSM and WCDMA mobile phone design, and in 2004 joined SDS S.r.L. as responsible for microwave designs. Since January 2008 he is working as a R&D Engineer in the hardware/RF division at Advantest Europe GmbH. He is an expert of high frequency theory and techniques. In his 31 years of professional design experience, he has covered both passive and active microwave components and subassemblies, including filters, amplifiers, oscillators and synthesizers, transmitters and receivers. He is author of five books and 29 technical papers and holds four USA patents.

Jose Moreira is a senior staff engineer in the HW R&D Team of the SOC business unit at Advantest in Böblingen, Germany. He focuses on the challenges of testing high-speed digital, silicon photonics and 5G mmwave devices, especially in the area of PCB test fixture design, signal and power integrity, measurement techniques and focus calibration. He joined Agilent Technologies in 2001 (later Verigy and in 2011 acquired by Advantest) and holds a Master of Science degree in Electrical and Computer Engineering from the Instituto Superior Técnico, Lisbon University, Portugal. He is a senior member of the IEEE and co-author of the book "An Engineer's Guide to Automated Testing of High-Speed Digital Interfaces".

Alexander Quint is a student at the Karlsruhe Institute of Technology. He received his B.Sc. degree in Electrical Engineering and Information Technology in 2017. The title of his Bachelor's thesis is "Design and Characterization of broadband Diplexers". He focuses on the design of passive microwave components.

Introduction

The opening of the mmwave spectrum to the next generation of mobile communications (e.g. 5G and WiGig) introduces mmwave based communications to the consumer area. From a test engineering point of view, it requires a significant jump in the testing frequencies from the maximum of 6 GHz used for LTE applications to frequencies as high as 44 GHz for 5G and 72 GHz for WiGig. On top of this significant jump in frequency, these new applications use phased array antennas, which means that the number of RF ports that need to be tested also increase significantly compared to LTE applications. At the same time the usual low cost of test pressure for consumer applications apply to the testing of these new mmwave integrated circuits.

There are multiple new topics and challenges for the automated test equipment (ATE) test engineering community from these mmwave applications [1].

In this paper we will concentrate on a very specific topic that is relevant for the testing of these new mmwave application with ATE systems. The topic is the design of combiners/dividers that can aggregate multiple RF ports into a single measurement/stimulus port. This can be very important for cost of test reduction since for example for a 5G integrated circuit with 16 antennas, a 1 to 16 combiner/divider would reduce the need of measurement resources from 16 to 1. In the case a single measurement resource is used with a 1 to 16 RF switch, the use of a combiner/divider might still be advantageous by allowing the parallel testing of all the RF ports reducing the test time. The choice of using a combiner/divider will be highly dependent on the target application and testing phase (e.g. initial characterization or high-volume production), available ATE resources, process/silicon maturity and test strategy.

In the next section, we will provide a high-level overview of mmwave combiner/divider topologies. We will then follow up with a discussion of the specific challenges with implementation in ATE PCB test fixtures and results from manufactured examples.

mmWave Combiner/Divider Topologies Review

In the last decades, A very solid theoretical background together with a myriad of combiner/divider designs and implementation approaches have been developed to address different requirements in terms of number of ports, frequency range, phase matching, power handling, etc…

In this section we will give a high-lever overview of two traditional design topologies used for implementing N-Port, phase matched combiner/dividers in an ATE PCB test fixture.

General Description

In general, power dividers/combiners are passive N-port networks ($N \geq 3$). They can be used as power dividers to split the power of an input signal into two or more output signals or they can be used to combine multiple input signals to one output signal of higher power [2]. In this case the power divider is called power combiner. The input of a power divider is the output of a power combiner and vice versa.

The easiest way to build a three-port power divider is shown in Figure 1. It consists of a T-junction and a susceptance which represents discontinuities in the junction. In [2] it is shown that a reciprocal 3-port network (which a power divider is) can never be lossless and matched at all ports. Therefore, to be matched at all ports, resistive elements need to be included in the schematic.

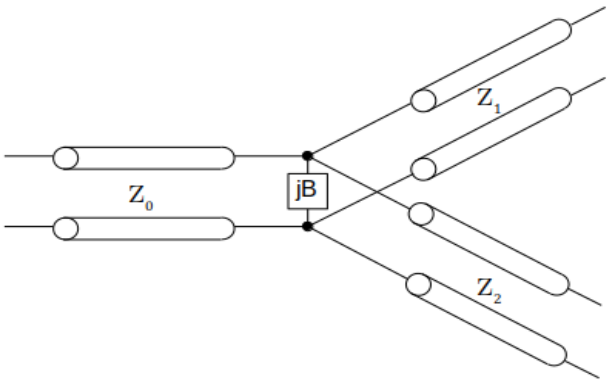


Figure 1: General schematic of a power divider.

Wilkinson Combiner/Divider

Another disadvantage of the simple power divider shown in Figure 1 is that the two output ports are not isolated against each other. To obtain isolation between the output ports, Wilkinson power dividers [2,3] are used. A 2-way Wilkinson power divider schematic is shown in Figure 2.

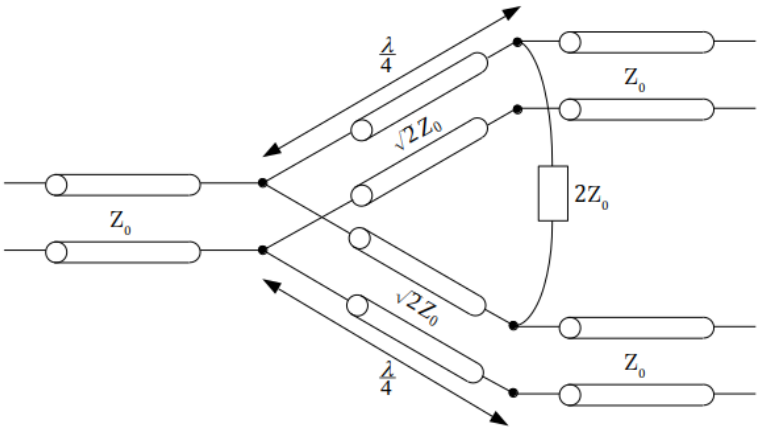


Figure 2: Schematic of Wilkinson Power Divider.

The two quarter-wave transformers provide good input matching whereas the resistor between the two outputs provides good isolation between the output ports. If the output ports are both matched the Wilkinson power divider even appears lossless because there is no current flowing through the resistor. The scattering matrix at the center frequency is shown below.

$$[S] = \frac{-j}{\sqrt{2}}\begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix}$$

As explained in [2,3,4], Wilkinson power dividers can be designed for multiple outputs. Furthermore, Wilkinson power dividers can have unequal power ratios as described in [5]. A Wilkinson power divider can also be extended using multiple sections to achieve a higher bandwidth [6].

Hybrid Ring or Rat-Race Combiner/Divider

As previously explained, it is not possible to build lossless 3-port networks that are matched at all ports. But for 4-port networks this is possible. One easy way to realize a 4-port power divider is a hybrid 180° coupler. The S-matrix for a 3 dB hybrid coupler at the center frequency is shown below.

$$[S] = \frac{-j}{\sqrt{2}}\begin{bmatrix} 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & -1 \\ 1 & 0 & 0 & 1 \\ 0 & -1 & 1 & 0 \end{bmatrix}.$$

One common way to realize this is a hybrid ring shown in Figure 3, also known as rat-race [2,4].

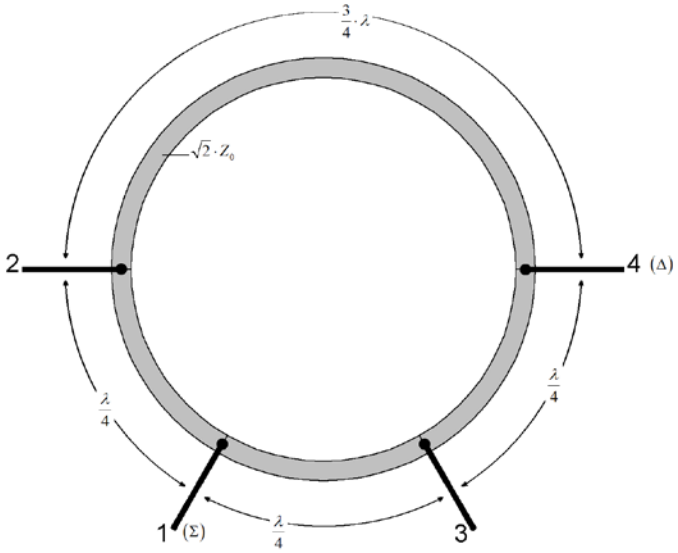


Figure 3: Hybrid Ring structure

If ports 1 or 3 are used as input ports the output ports (2,3 or 1,4 respectively) are in phase and the ports 4 or 2 respectively are isolated. If ports 2 or 4 are used as input ports the output ports (1,4 or 2,3 respectively) are shifted by 180° and the isolated ports are port 3 or port 1 respectively. A hybrid ring can also be used as a power combiner with two inputs and one sum and one difference output. For example, if ports 2 and 3 are used as input ports, port 1 is the sum output and port 4 is the difference output.

This type of power combiner divider is usually used in the frequency ranges above 50 GHz as it is very difficult to use power dividers with resistors at such high frequencies. For the lower frequencies range of 20-40 GHz a hybrid ring is not broadband enough, so for this frequency range a Wilkinson power divider is the better choice.

ATE Test Fixture Challenges for mmWave Applications

There are some important challenges for ATE PCB test fixtures used in mmwave applications. Figure 4 shows an example of a typical multi-site ATE PCB test fixture for high volume production testing of an LTE related RF device (below 6 GHz). These PCBs are very large (e.g. 516.8 mm by 600 mm) and very thick (e.g. a minimum thickness of 3.5 mm is required for some ATE platforms because of the spring pin based ATE interface for digital and power signals), with stackup thickness reaching 5 mm or higher. Also, due to cost of test pressure, it is necessary to do multi-site setups where multiple DUTs are test in parallel (e.g. in Figure 4, eight DUTs are tested in parallel). This creates further challenges since the pitch between the DUTs can be very tight due to handler requirements.

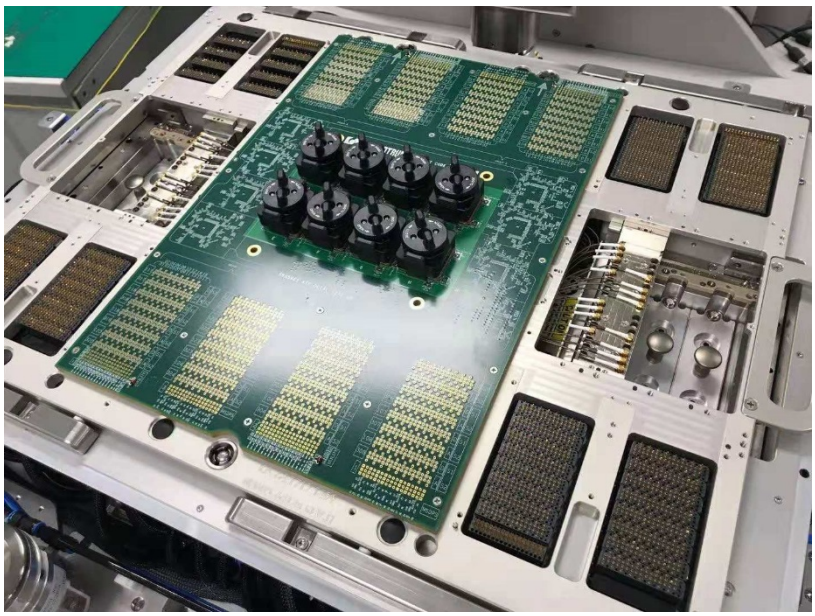


Figure 4: Example of an ATE test fixture with 8 sites for high volume testing of an RF integrated circuit (<6 GHz). Courtesy of Speadtrum.

Another important factor is that the manufacturing volume for an ATE PCB test fixture is small compared with other higher volume PCB applications. It can be as small as only 1 or 2 boards at the start of a project. Due to their size and complexity and low volume, these PCB boards will be relatively expensive. Also, they do not allow easy measurement access since on the DUT side where there will be for example a BGA pad array with a socket or a probe head.

The DUT pitch is also a challenge. Current BGA pitches for mmwave applications can be lower than 0.4 mm and non-regular sometimes. This small pitch coupled with a very large and thick PCB test fixture further complicates manufacturing. It will also create mechanical restrictions on any combiner/divider designs one needs to implement to connect to the DUT BGA pads.

One first important choice for an PCB ATE test fixture for mmwave applications is the dielectric material. High performance dielectric materials that have been the default choice in mmwave applications (e.g. Rogers Duroid) cannot be used for the large size, high layer count PCBs that are typical of ATE applications. The preferred choice is to use traditional high-performance materials that are already in use for ATE test fixture applications like Isola Meteorwave, or Panasonic Megtron 6. Of course, there are other dielectric material options and it is even possible to use hybrid stackups with a high-performance RF material in the outer layers and standard FR4 in the inner layers but this needs to be discussed in detail with the PCB test fixture fab house.

There is another important choice to make on the dielectric material and that is the type of fiber weave that is used. Typical high performance RF materials for ATE PCB test fixture manufacturing use a glass weave. This glass weave will have an impact on the dielectric loss and more important on the dielectric constant. The result is that depending on the used fiber wave and the trace layout, it will have an impact on the signal delay. This is exemplified in Figure 5. This is now important because mmwave application usually use phase array antennas where the phase of each element is critical. On the PCB test fixture, it is important that the phase delay of all interconnects to the antenna ports are the same. As shown in Figure 5, depending on the layout some traces might see a slightly different dielectric constant. To minimize this effect two approaches are used: The first is to use a spread glass fiber weave type like 1078. The other is to rotate the PCB test fixture on the manufactured panel (e.g. 10 degrees) [8].

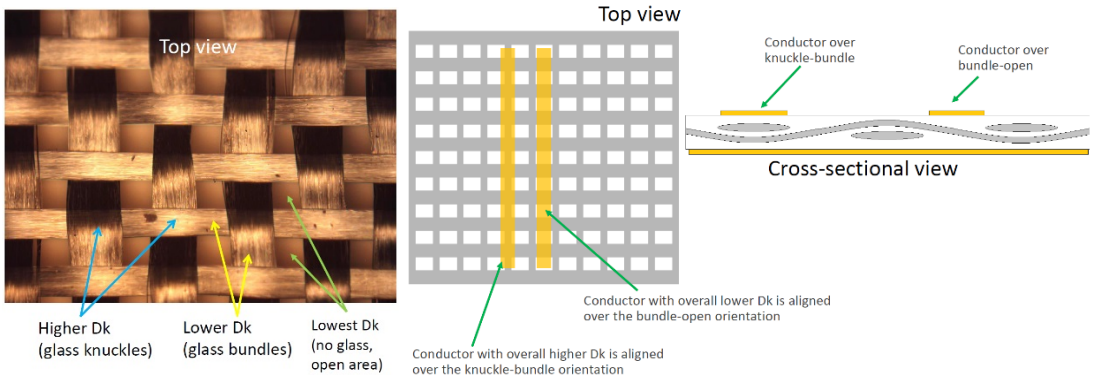


Figure 5: Fiber weave impact on mmwave signals (reproduced with permission from [7]).

Another challenge is the microstrip copper profile and plating. For traditional RF applications (< 6 GHz) only the skin effect and dielectric loss were important but for mmwave applications the surface roughness loss becomes important [8,9]. This means that when selecting the dielectric material, one also needs to consider the type of copper profile to be used. But this discussion also needs to take into account the manufacturing and reliability requirements of the PCB test fixture. Choosing for example a very low-profile copper might make sense from a loss mitigation point of view, but if the PCB fab house cannot guarantee its reliability for the specific requirements of a ATE PCB test fixture, then it should not be used because it might generate other problems.

Finally, although it is not discussed in this paper, the connection to the package DUT, either a socket or a wafer probing head will be the “last mile” on the signal path, and if not paid enough attention will significantly degrade the performance independently of how good the PCB test fixture was designed and manufactured.

Implementation Examples: Wilkinson Combiner

As mentioned on the previous section, ATE PCB test fixtures present significant challenges due to their size and requirements. Although there are off the shelf combiners/dividers with excellent performance especially for the 5G frequency range, they use materials and implementation techniques that are not possible in an ATE PCB test fixture. Figure 6 shows some off the shelf examples. Usually the signal trace is implemented as a very wide stripline between two flexible dielectric layers (e.g. Rogers Duroid) with the connectorized module body providing the reference planes. The designs are also usually large in size to allow implementation of a long tapered transformer to achieve excellent return loss. Multiple resistors are used, or in some cases a distributed resistor paste. More important the entire assembly can be measured prior to use and in some cases if needed tuned.

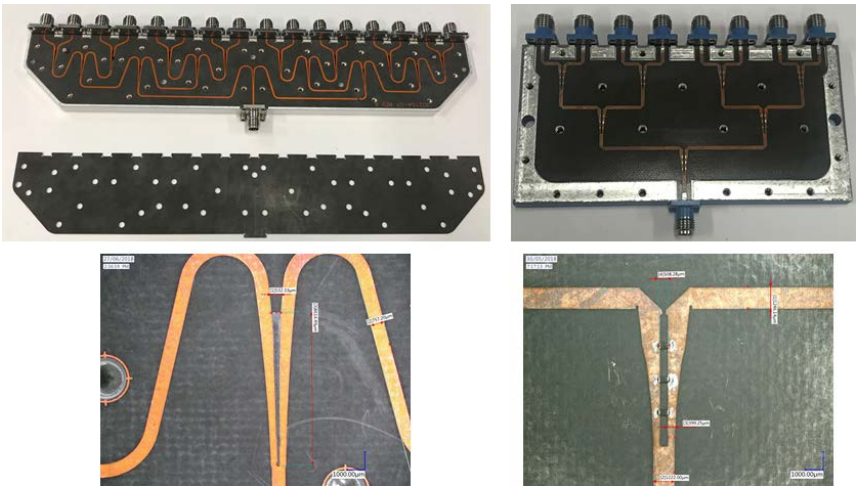


Figure 6: Example of off the shelf high performance power combiners/dividers for the 5G frequency range.

For ATE PCB test fixtures, the PCB size and the need for a multilayer implementation limits the types of possible approaches. Also, the large number of

ports needed for application like 5G coupled with the need for parallel testing of multiple DUTs for low cost of test, requires that the combiner/divider structures be small in size and cannot be tuned or use processes that are incompatible with standard ATE PCB test fixture manufacturing and assembly.

Figure 7 shows an example that exemplifies the challenges. In this example a quad-site 5G application is implemented. Each DUT has two phased array antennas composed of 16 individual antenna ports. These 16 antenna ports need to be combined using a Wilkinson combiner/divider. The pitch between the individual DUTs is defined by the production test cell requirements, specifically the pitch required by the test cell hander that automatically inserts packaged DUTs to be tested [8]. To better demonstrate the size difference, Figure 8 shows a size comparison between a single DUT on the PCB test fixture that has two 1 to 16 Wilkinson combiners implemented on the PCB test fixture with an off the shelf 1 to 16 Wilkinson combiner in a coaxial package.

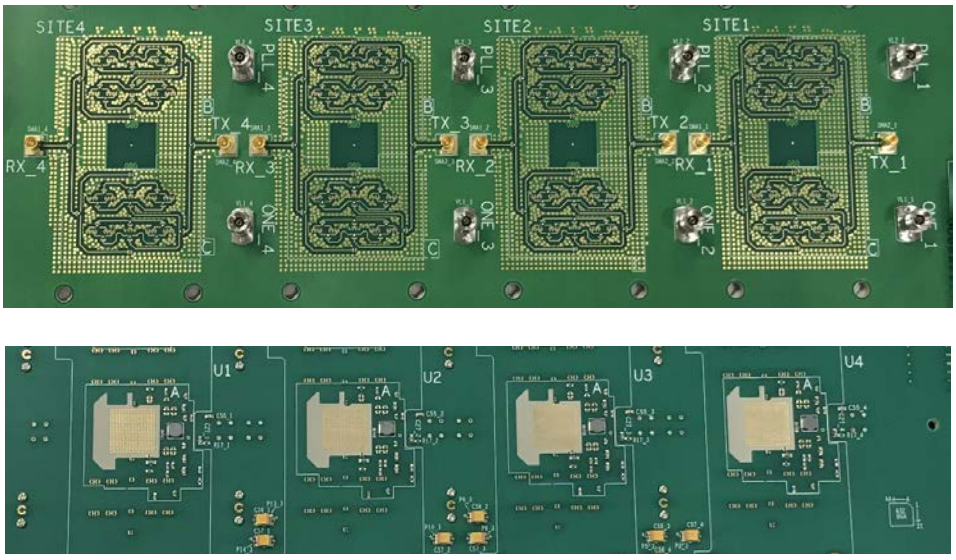


Figure 7: Example of an ATE PCB test fixture implementation of a 5G quad-site application where each DUT has two phased array antennas, each one with 16 antenna ports that need to be combined.

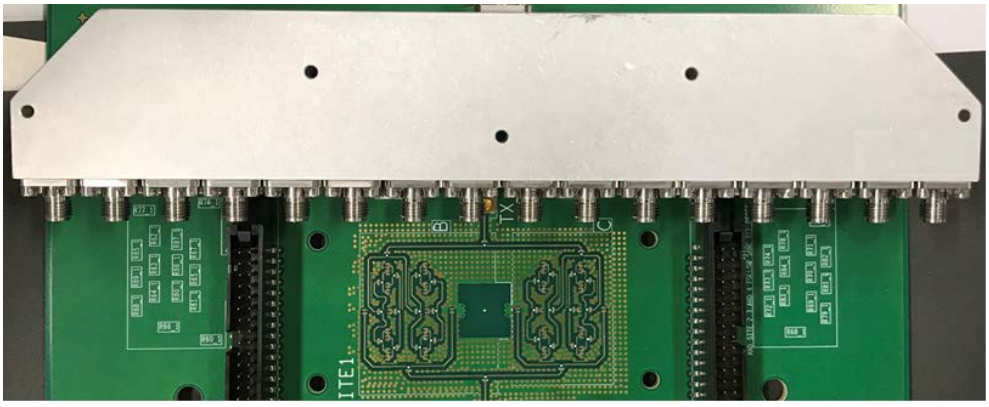


Figure 8: Size comparison of a single DUT with two 1:16 implemented Wilkinson combiners compared with an off the shelf 1:16 Wilkinson combiner in a coaxial package.

In Figure 8 it is possible to observe that the size difference is very significant. But on the other hand, the performance difference will also be significant with the larger coaxial packaged 1 to 16 Wilkinson showing a much better performance. There is always a trade-off.

We will then start by showing three examples of implementing a single 2-way Wilkinson combiner/divider element targeted for 5G applications (target design was 20-40 GHz). The three examples are shown in Figure 9.

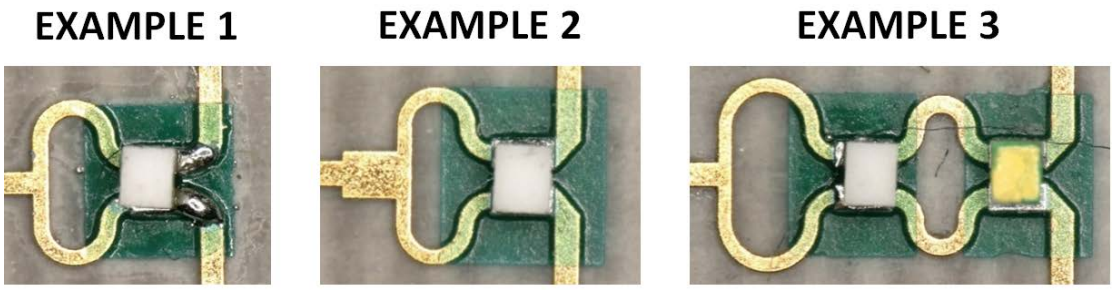


Figure 9: Implementation examples of single 2-way Wilkinson combiner/divider.

Example 1 is the easiest layout for a Wilkinson power divider. The quarter-wave transformers are curved to reduce coupling between them. In Example 2 there is only a small modification where a short line with a different width in front of the quarter-wave transformers is used to further improve the input matching. Example 3 is the most complex example since it consists of two power divider stages. In general, such a multi-stage Wilkinson power dividers have a higher bandwidth than single-stage Wilkinson power dividers. These are just three examples we have chosen to investigate because of their implementation simplicity and small size.

Figure 10 compares the performance of an ideal implementation of the three examples shown in Figure 9. On the figure left y-axis, in black, S21 is equal to S31. On the right y-axis: S11 (common port) in shown in blue, S22 is equivalent to S33 (output ports). S32 (output-ports isolation) in shown red. Note that S21 and S11 of example 2 and 3 are coincident.

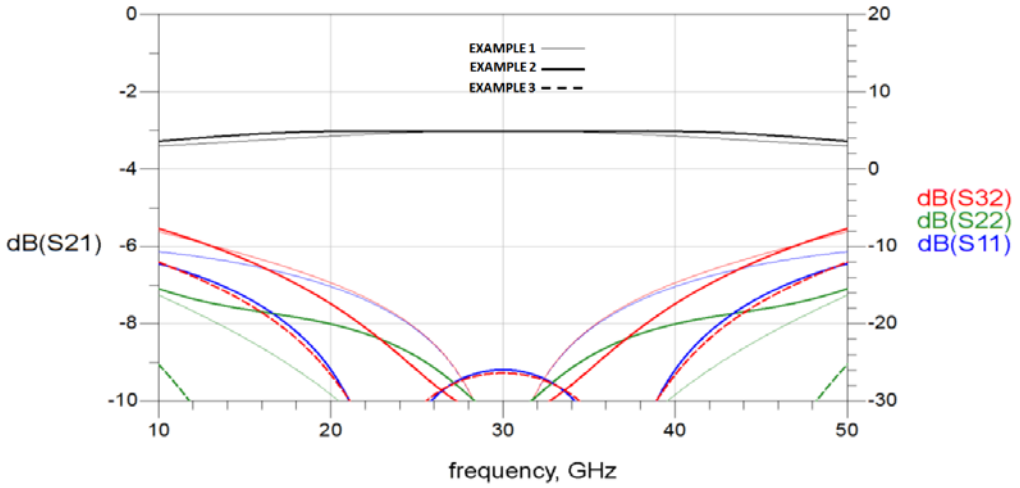


Figure 10: Calculated response for an ideal model of the three Wilkinson elements shown in Figure 9.

Figure 11 shows the performance comparison of the three examples shown in Figure 9 but using a more detailed simulation model. It can now be seen a degradation on each of the parameters compared with the ideal case shown in Figure 10.

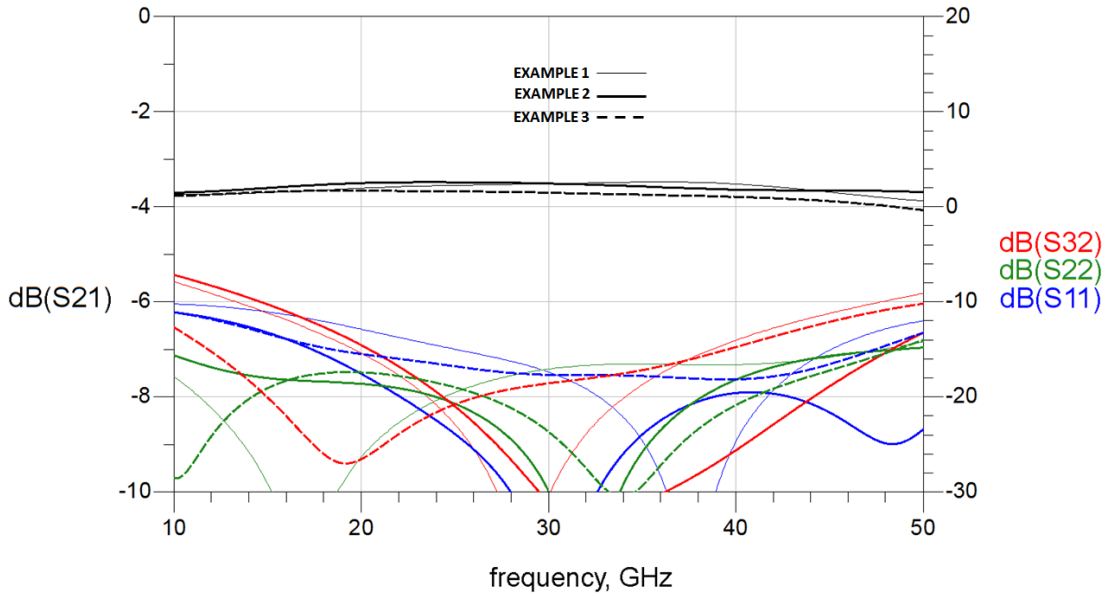


Figure 11: Calculated response for a more realistic simulation model of the three Wilkinson elements shown in Figure 9.

The key metrics when evaluating a combiner/divider is its phase matching which in the case of a Wilkison simulation model is always perfect, the return loss at each port and the loss matching across the frequency range interest. To better compare the examples, Table 1 and Table 2 show the insertion and return loss of the common port for the three examples at five different frequencies.

	20 GHz	**28 GHz**	**30 GHz**	**39 GHz**	**40 GHz**
Example 1	3.61 dB	3.53 dB	3.52 dB	3.50 dB	3.52 dB
Example 2	3.50 dB	3.50 dB	3.51 dB	3.63 dB	3.64 dB
Example 3	3.66 dB	3.70 dB	3.70 dB	3.78 dB	3.79 dB

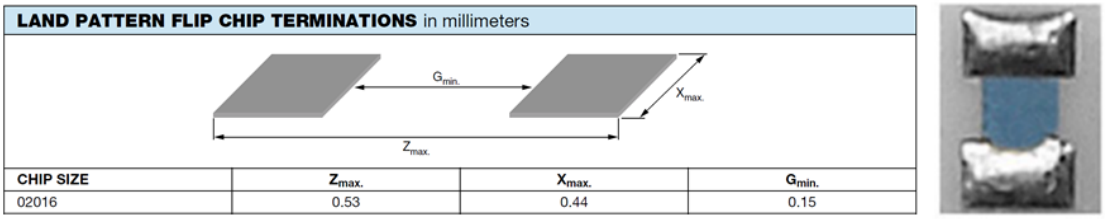
Table 1: Comparison of the simulated insertion loss for each Wilkinson example.

	20 GHz	**28 GHz**	**30 GHz**	**39 GHz**	**40 GHz**
Example 1	12.81 dB	16.25 dB	17.40 dB	29.51 dB	24.66 dB
Example 2	17.58 dB	30.08 dB	39.03 dB	19.91 dB	19.59 dB
Example 3	15.49 dB	17.48 dB	17.68 dB	18.15 dB	18.15 dB

Table 2: Comparison of the simulated return loss for the common port each Wilkinson example.

The results show as expected that example 2 has an overall improved return loss on the common port compared with example 1. Example 3 on the other side, shows slight less variation on the insertion loss compared with the other examples. These differences might seem small when comparing single elements but as will be shown later, they do amplify once one starts to aggregate the elements in a more complex Wilkinson combiner (e.g. a 1 to 8 Wilkinson combiner/divider).

One important question when designing a Wilkinson power divider is which type of resistor to use. In the examples provided in this paper, we used the Vishay Sfernice line (e.g. CH02016-100RGFT for a 100 Ohm Resistor). The chosen footprint is 02016 and its dimension are shown in Figure 12. The flip chip version was used as shown on the picture in Figure 12. The resistor is specified to 50 GHz.



CHIP SIZE	$Z_{max.}$	$X_{max.}$	$G_{min.}$
02016	0.53	0.44	0.15

Figure 12: Land pattern specification for the used Vishay resistor.

One practical challenge related to using such a resistor is its assembly. Although for maximum performance one would wish to avoid any solder mask on the signal traces, due to its impact on high-frequency signals [8], from an assembly point of view this is not practical since it reduces significantly the reliability. This means that a proper solder mask has to be used around the assembly area as shown in Figure 13. Another assembly problem shown in Figure 13 is the risk that if too much solder mask is used, the resistor will be lifted higher which can also impact performance. Finally, Figure 14 shows another possible assembly problem that requires special attention. Given the small separation between the resistor pads, excess solder can also result in the creation of solder bridges that create a short between the resistor pads. Note that checking for these solder bridges is very hard because at DC there is always a short between those two pads.

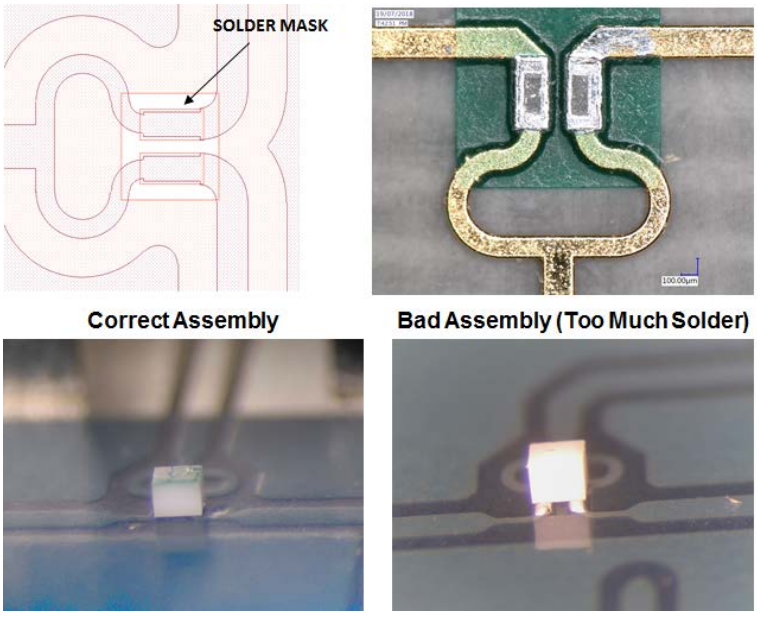


Figure 13: Assembly challenges with the Wilkinson combiner/divider resistor.

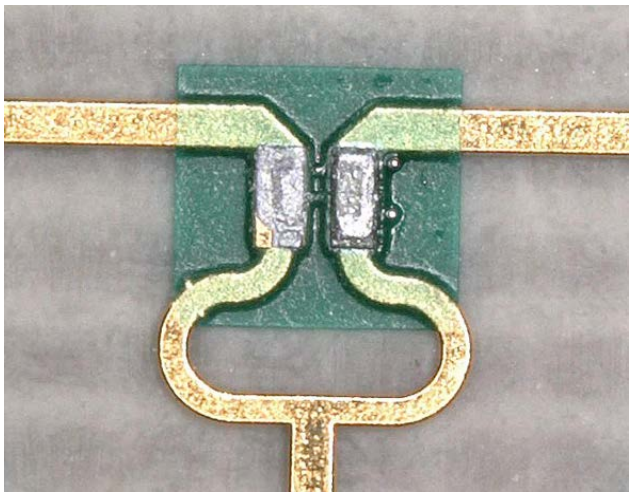


Figure 14: Solder shorts between the pads of the Wilkinson combiner/divider pads.

These combiner elements were implemented and manufactured in a PCB fab house specialized in ATE PCB test fixtures. In this section, we will present the results obtained using a 9.5 mil trace width microstrip with standard RTF copper foil in a Megtron 6 dielectric with 1078 spread glass. Figure 15 shows a picture of the manufactured test coupons for the Wilkinson combiner examples shown in Figure 9. A 1.85 mm edge mounted coaxial connector was used with fully 3D EM optimized footprint.

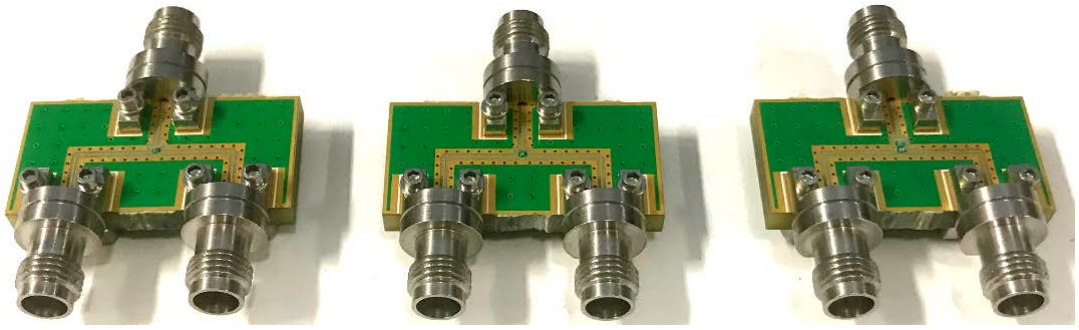


Figure 15: Manufactured test coupons for the Wilkinson combiner examples 1, 2 and 3 shown in Figure 9.

Figure 16 and Figure 17 show the measured results for the three examples implemented in the Megtron 6 test coupons shown in Figure 15. Note that the connectors were not de-embedded in the measured data.

From the measurement results shown in Figure 16 and Figure 17, it can be observed that the transmission is very similar for the three different Wilkinson power divider types. Example 1 has the worst input and output matching as well as the worst isolation. Example 2 has a better input and output matching and isolation compared to Example 1. This is expected as the short line in front of the quarter-wave transformers was added to improve the matching. Example 3, the two-stage Wilkinson 2 power divider, has the best input matching and isolation. The output matching is similar to Example 2.

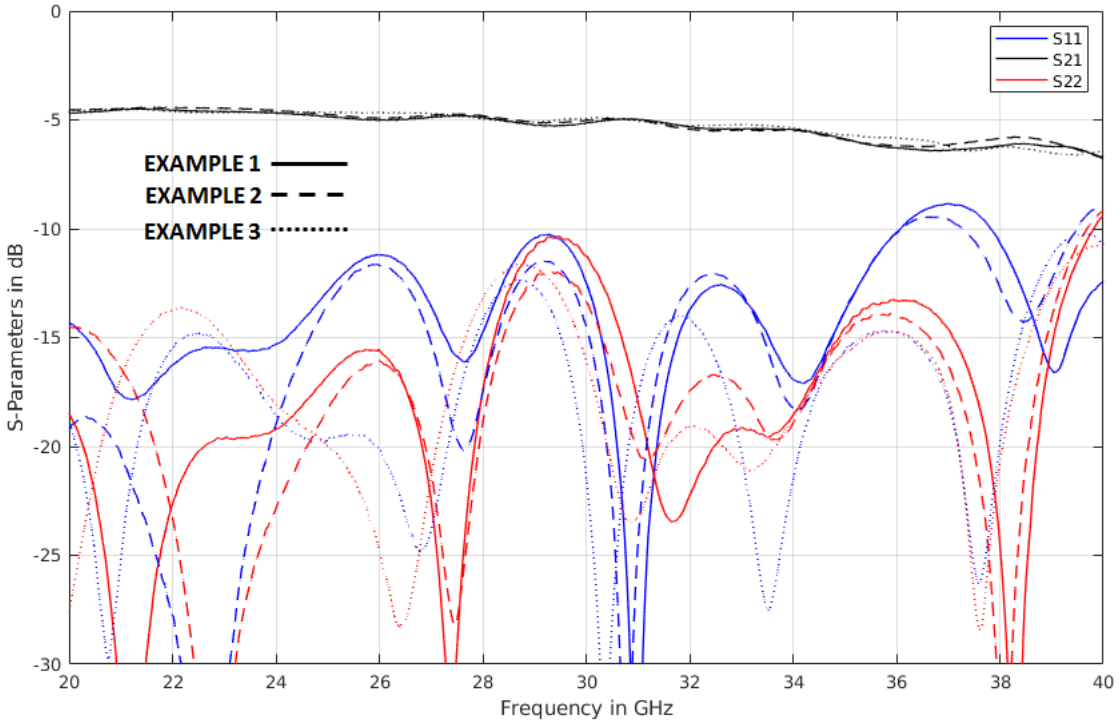


Figure 16: Comparison of the measured insertion loss and return loss of the common port for the three examples.

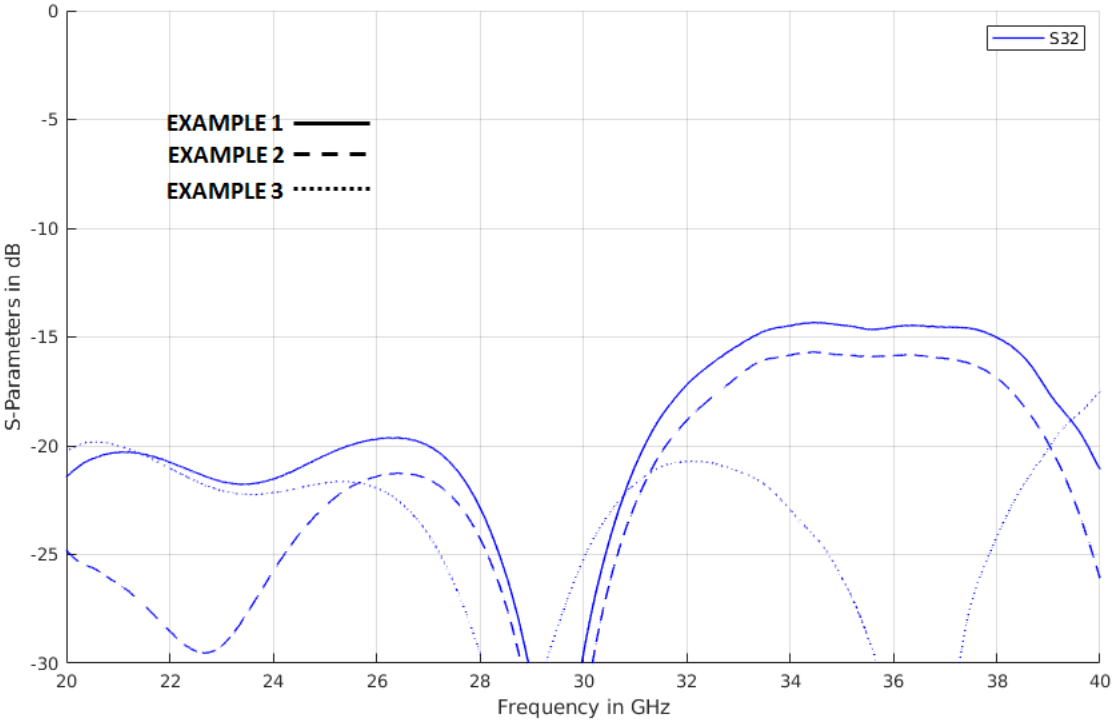


Figure 17: Comparison of the measured isolation between port 2 and 3 of the three implemented examples.

To further show the differences between the example 1 and example 2 elements, a 1 to 8 combiner structure was implemented as shown in Figure 18 using both types.

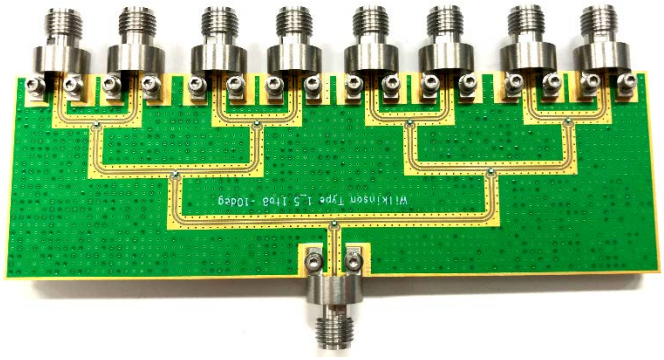


Figure 18: A 1 to 8 Wilkinson combiner/divider test coupon.

Figure 19 shows the simulated results for the two test coupons. The results show that although when looking at the single element performance the differences between example 1 and 2 do not appear dramatic, when implementing a more complex Wilkinson divider these differences accumulate resulting in a much more significant difference between both implementations.

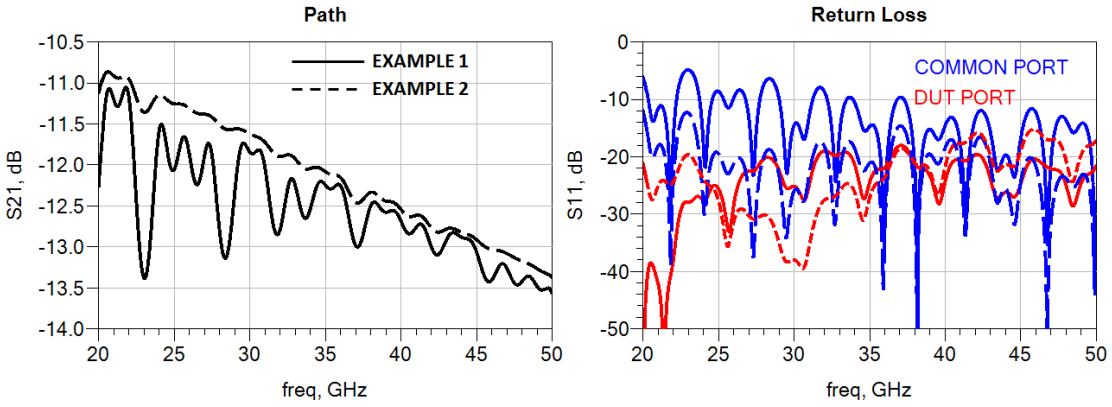


Figure 19: Simulated results comparing a 1 to 8 Wilkinson combiner/divider implemented with the example 1 and example 2 elements.

Figure 20 shows the measured results from the two manufactured test coupons. Although the 1 to 8 Wilkinson divider using the example 2 element shows a little better insertion loss stability as observed on the simulations, the measured difference is not as strong as shown in the simulation. Note that in these measurements the connectors were not de-embedded. Furthermore, the return loss results do not show the clear improvement that was expected with the example 2 element. One reason for the lack of expected performance improvement with the example 2 element is of course its manufactured implementation. Figure 21 shows a microscope picture of one of the example 2 elements in the 1 to 8 Wilkinson divider/combiner. The measured dimensions show a difference to the design parameters. To further complicate matters, because of the microstrip trace trapezoidal form, the dimensions measured from the top correspond only to the top dimension of the trace trapezoid, with the copper trace dimension on the bottom having slightly different dimension as shown in Figure 22.

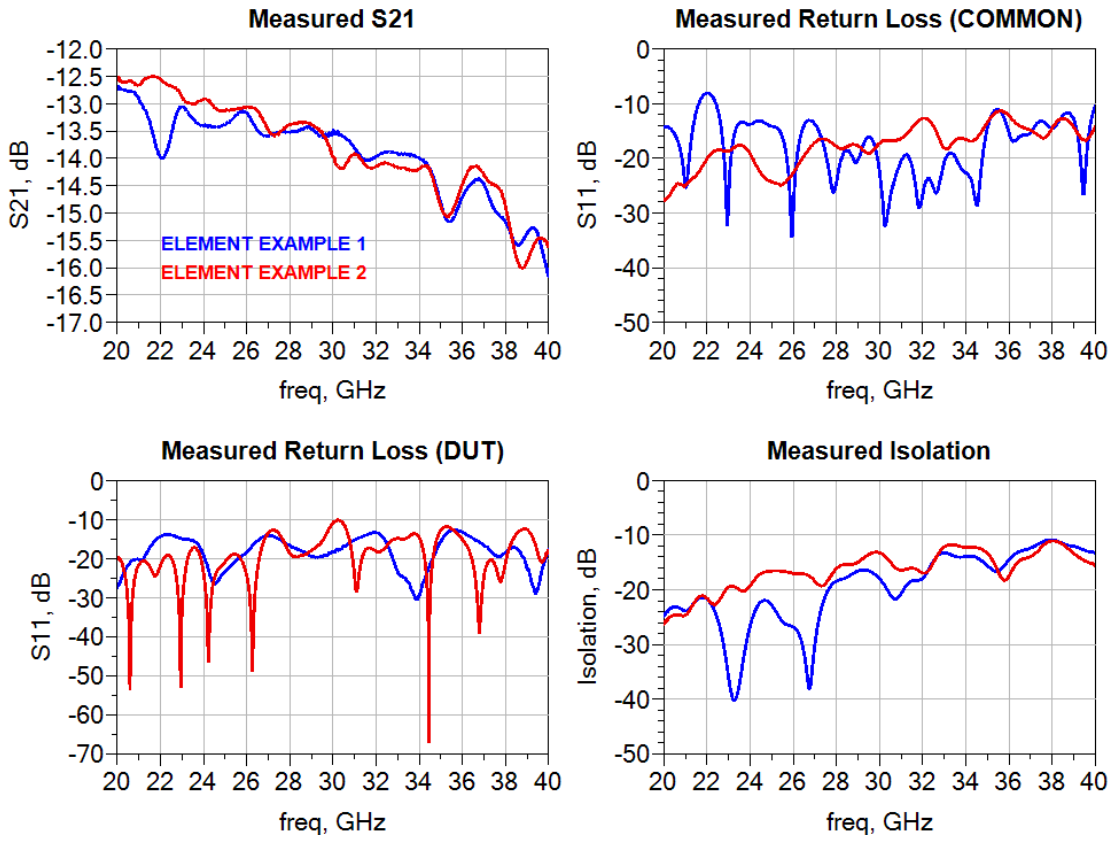


Figure 20: Measured results comparing the 1 to 8 Wilkinson combiner/divider implemented with the example 1 and example 2 elements.

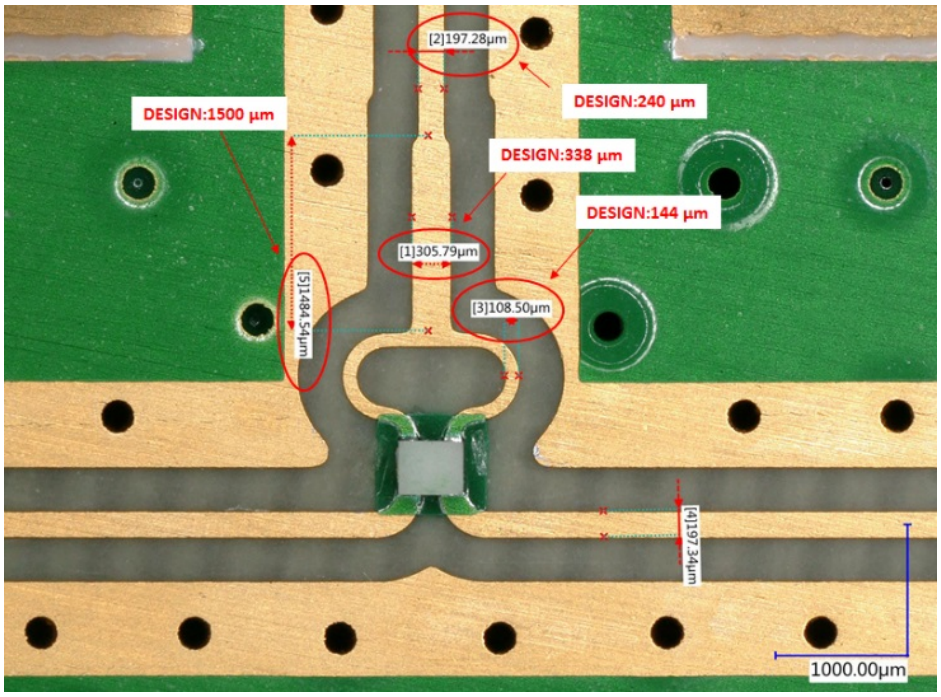


Figure 21: Microscope picture showing the measured and designed dimensions for one example 2 type element in the measured 1 to 8 Wilkinson combiner/divider.

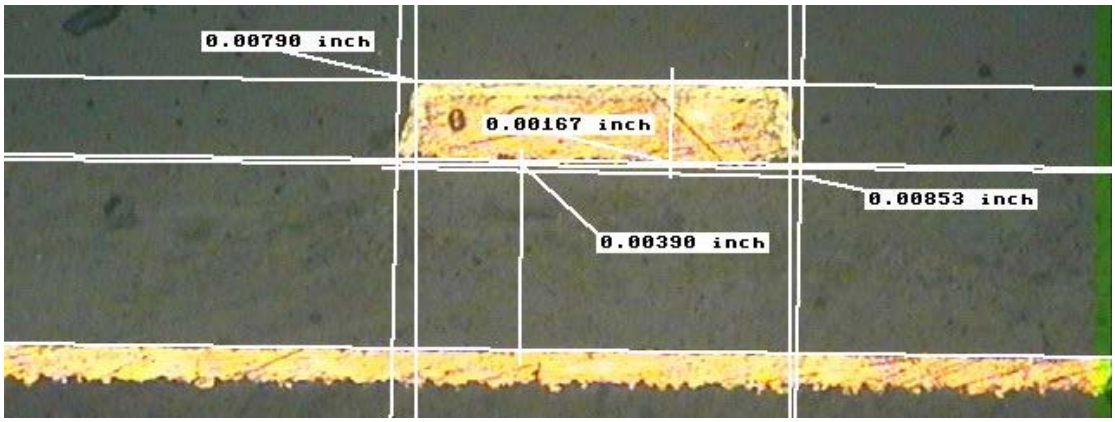


Figure 22: Microstrip cross-section of a 50 Ohm trace section of one of the test coupons showing the expected trapezoidal form.

Another important point is the insertion loss and phase matching between the different paths. In this case, because the chosen element has perfect matching from a theoretical point of view, it will be the manufacturing variation that will determine how good the two paths on the combiner/divider are matched. Figure 23 shows the results for both cases. The measured difference between both cases cannot be used to make any assumption if one design is more immune to manufacturing variation than the other. For this we would need a much larger statistic sample of manufactured boards. The important point is that in both cases, the measured loss and phase matching were reasonable and would be acceptable for an ATE PCB test fixture for volume production of a 5G application.

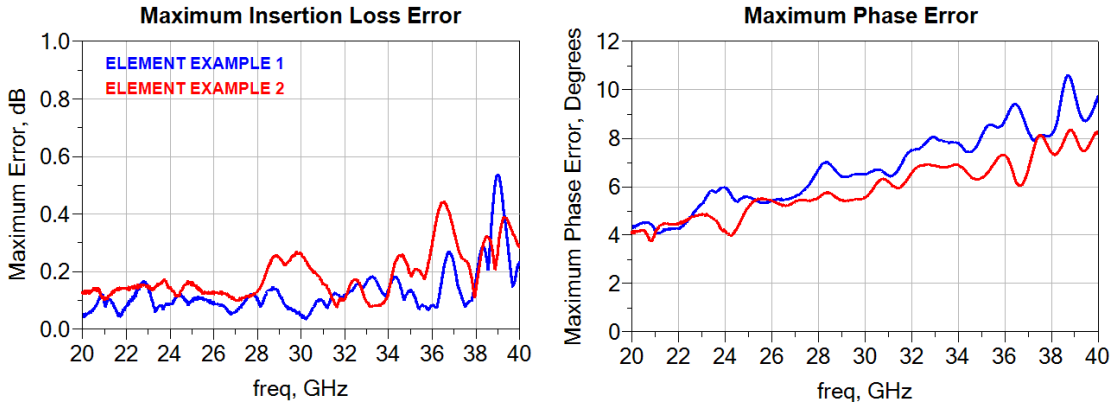


Figure 23: Measured results showing the insertion loss and the phase matching between the 8 branches of the 1 to 8 Wilkinson combiner/divider for both example 1 and 2 cases.

Finally, it is important to understand that the design decision of using a small Wilkinson element with a standard PCB test fixture dielectric material and manufacturing process degrades the performance compared with the standard off the shelf Wilkinson combiners implemented using much larger element topologies and higher performance materials. This is shown in Figure 24 which compares a off the shelf 1 to 8 Wilkinson combiner/divider to the 1 to 8 test coupons implemented with example 1 and 2 Wilkinson elements.

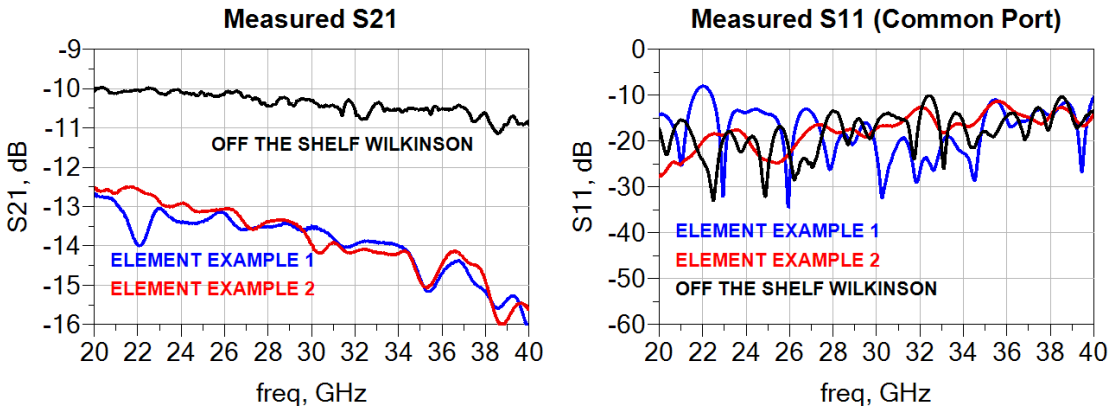


Figure 24: Comparison of the two Wilkinson 1 to 8 implementations using example 1 and example 2 elements with a state of the art of the shelf 1 to 8 Wilkinson combiner/divider in a connectorized package.

Implementation Examples: Hybrid Ring

As mentioned on the previous section, hybrid ring based combiners/dividers are able to work at higher frequencies than traditional Wilkinson combiners but with a smaller bandwidth. We target this type of design for WiGig applications to a frequency band of 56 to 72 GHz. Unfortunately, in this frequency ranges it is not easy to get off the shelf combiners in coaxial packages although there are some vendors that are able to provide some units (e.g. 1 to 2 or 1 to 4) but usually they are done by special request and not part of the catalog.

Like on the Wilkinson combiners examples of the previous sections, we will start by showing two examples of implementing a single a single 2-way hybrid ring combiner/divider element targeted for the WiGig frequency range. The two examples are shown in Figure 25. The shape of the ring in both examples is not exactly circular, due to the T-junctions, which are rectilinear. The layout of example 2 looks more regular due to the smaller size of the T-junctions. In this case, trapezoidal tapers have been added, in order to minimize the length of the T-junction and simultaneously geometrically match the width of the 50 Ohm lines.

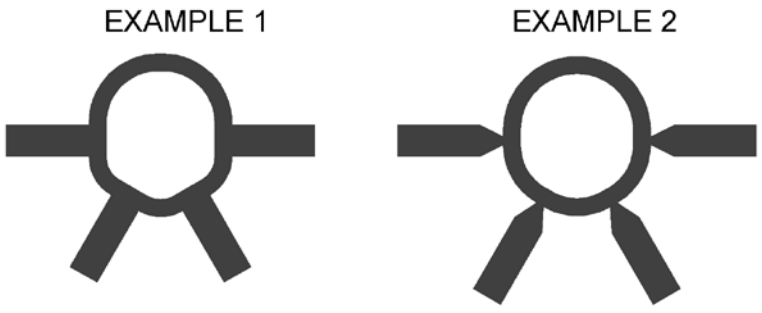


Figure 25: Implementation examples of single 2-way hybrid ring combiner/divider.

Figure 26 shows the simulated response of the two hybrid ring (rat-race) combiners/dividers examples in Figure 25, using the port assignment as defined in Figure 3. On the figure left y-axis, in green S21 is equal to S41. On the figure right y-

axis S11 is equal to S22 in black and S33 is equal to S44 in blue. The performances of example 2 seems worse, but the simulation of that case is more reliable. This is because of the smaller size of the T-junctions, particularly considering the effectively realized shape as will be shown later in Figure 30.

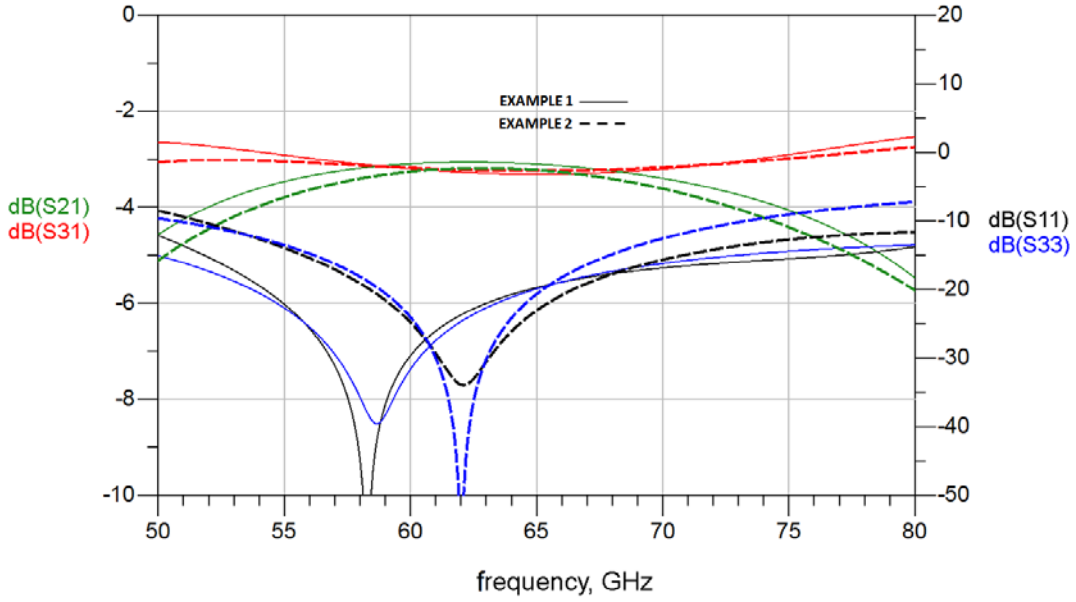


Figure 26: Simulated response using a simplifies model of the two hybrid ring examples shown in Figure 25.

We implemented example 2 of the hybrid ring using a Megtron 6 dielectric material. A 9.5 mil trace width microstrip was used for the 50 Ohm sections, with standard RTF copper foil. A 1078 type spread glass was used. Figure 27 shows a picture of the manufacture test coupon with a coaxial termination on the isolation port. A 1 mm edge mounted coaxial connector was used (to allow accurate measurements to 80 GHz) with fully 3D EM optimized footprint.

Figure 28 shows the simulated and measured results for this structure. The connectors were not de-embedded from the measured data, so a full 3D EM simulation was done including the connector model as shown in Figure 29. The used PCB parameters on the simulation (dielectric constant and loss tangent) were based on tuned values from a previous test coupon using the procedure described in [10]. This is critical to obtain accurate simulation results.

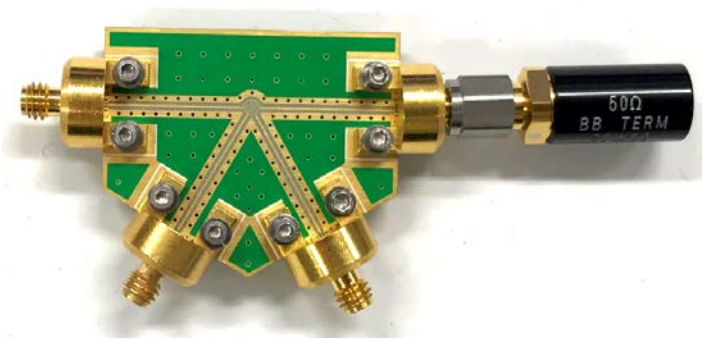


Figure 27: Implementation of a hybrid-ring structure using a hybrid ring test coupon.

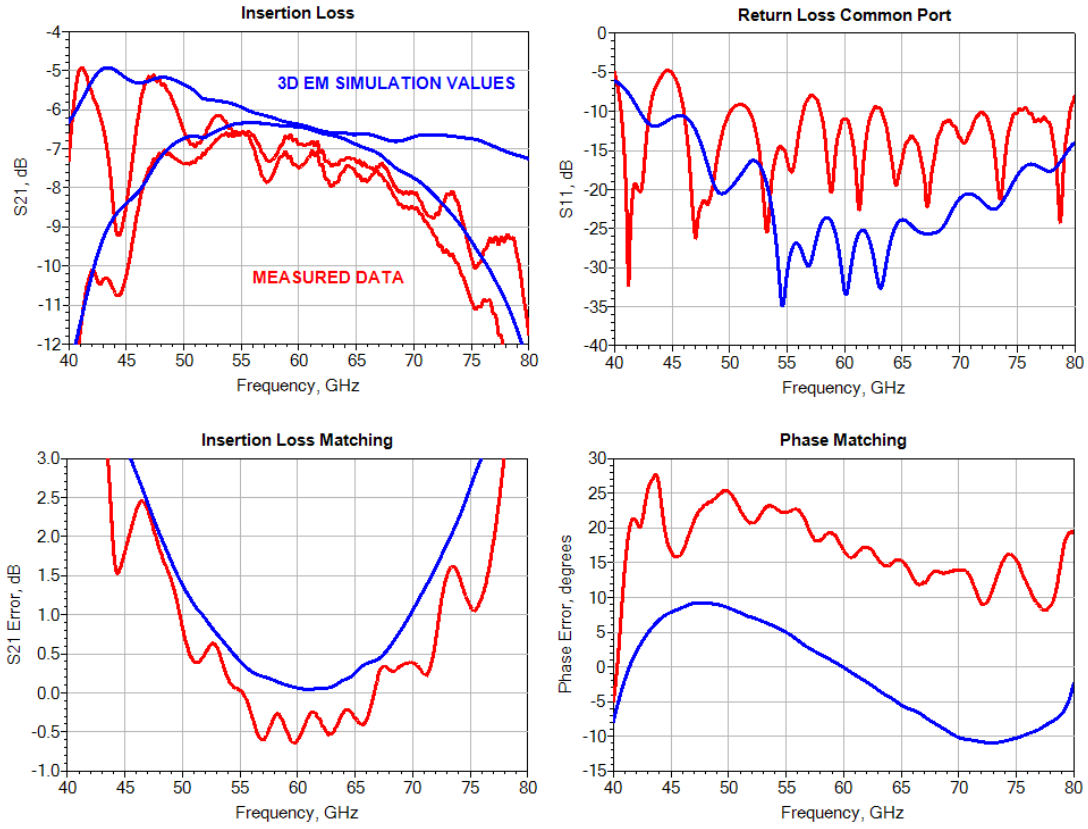


Figure 28: Results of the hybrid ring test coupon simulation and measurement.

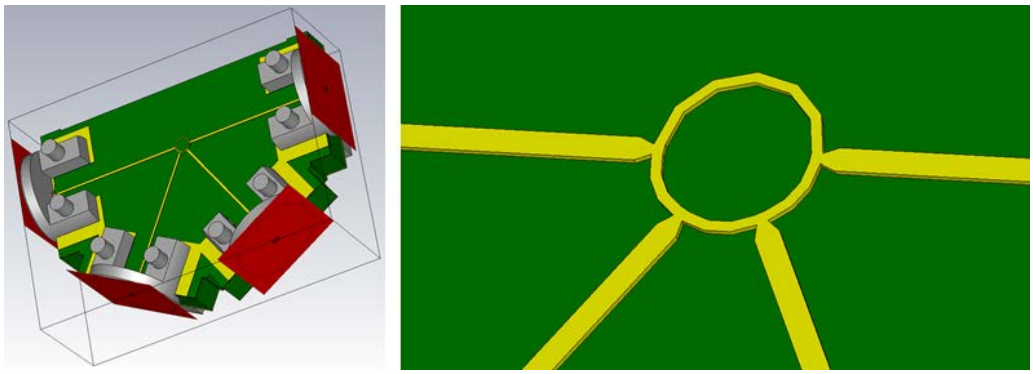


Figure 29: Simulation model.

The results show a reasonable correlation to simulation even when assuming the structure etching was perfect. The target bandwidth of the hybrid ring (56 to 72 GHz) was almost achieved with less than 1 dB measured amplitude imbalance and less than 25 degrees measured phase imbalance in that frequency range between 56 and 70 GHz.

As mentioned before, the simulation assumes the etched structures were perfect. But when analyzing the implemented structures with a microscope as shown in Figure 30, one can see that there is some mismatch between the design parameters and the etched

structures. Note that the dimensions measured by the microscope do not correspond exactly to the true geometry of the microstip trace due to its trapezoidal format as shown in Figure 22. Also, although a spread glass type was chosen for the Megtron 6 dielectric, at these very high frequencies, the effect of a fiber weaved material cannot be dismissed, and it is not included on the simulation.

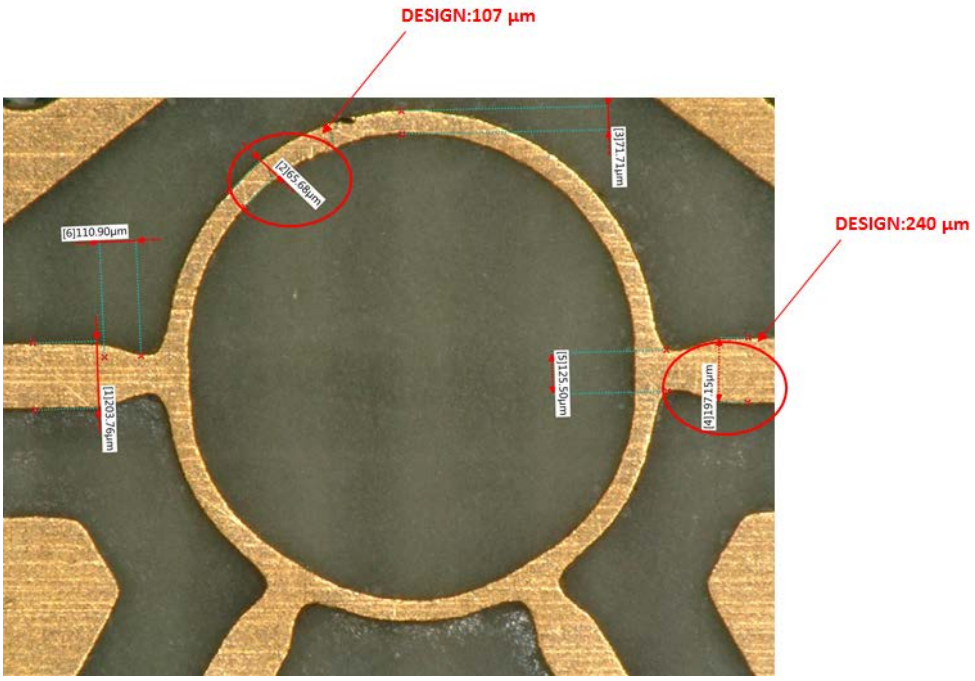


Figure 30: Manufactured example showing the variations between the design target and the manufactured traces.

One important question when implementing a hybrid ring combiner for ATE PCB test fixture applications is the issue of how to implement the load that is needed on one of the ports since using a coaxial load as on the example in Figure 27 is not feasible. Note that theoretically we could use a lossy signal trace with an open at the end. As long it is long enough to fully attenuate the reflected waveform it would do the job. The problem is that we usually do not have the space needed for such a long signal trace. So basically, there are two options to create the load: use a 50 Ohm resistor or an RF absorptive material.

To test the different options, the test coupon shown in Figure 31 was manufactured to allow the measurement of the return loss of the different options. For the RF absorptive material, the SB1004 material from ARC Technologies was used. For the SMT resistor, the same Vishay resistor already discussed previously on the Wilkinson combiner case was used although in this case with a 50 Ohm value.

The measured results in Figure 32 show that both options show reasonable performance to serve as load on the isolation port of a hybrid ring topology. Note that both options could be merged, i.e. using a SMT resistor together with a RF absorptive material with a pocket created to accommodate the SMT resistor. From an ATE test fixture PCB manufacturing point of view, the SMT resistor is preferred although as described previously, it also presents assembly challenges due to its geometry.

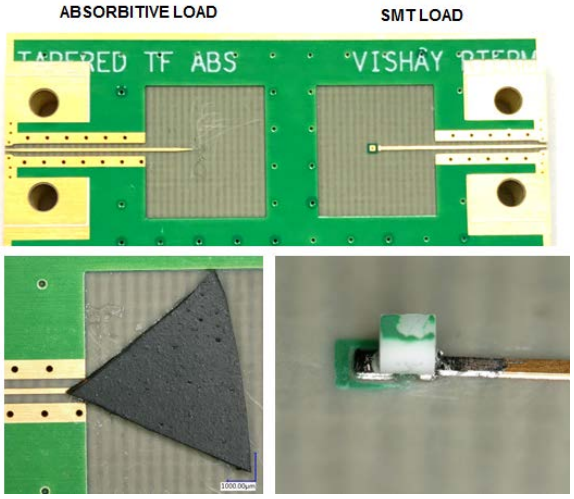


Figure 31: Manufactured test coupon to evaluate the performance of the different options to implement a termination load on the isolation terminal on the hybrid ring combiner/divider.

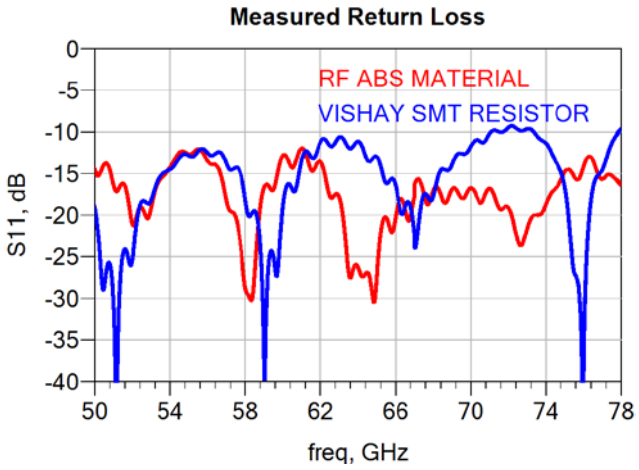


Figure 32: Comparison of the measured return loss between a termination load using a SMT resistor and an RF absorptive material.

A 1 to 4 hybrid ring based combiner/divider was implemented using the Vishay SMT resistor as the termination load as shown in Figure 33.

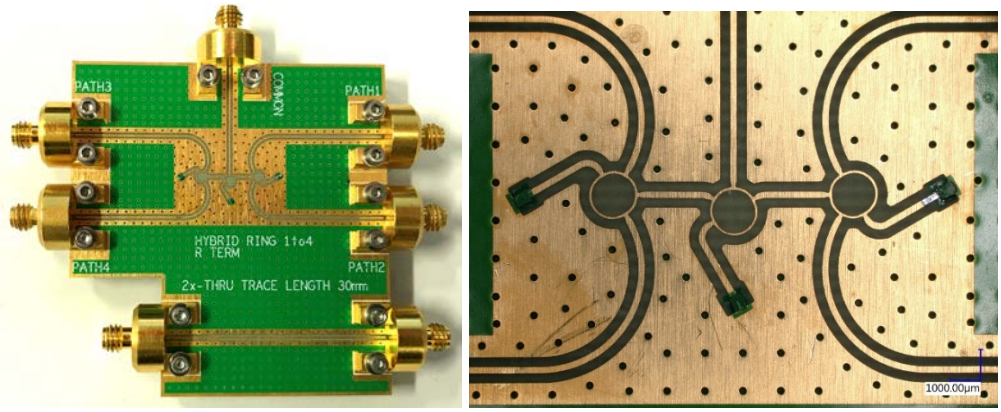


Figure 33: Manufactured example of a 1:4 hybrid ring based combiner/divider with a Vishay SMT resistor as load. A 2x-thru trace is also included for de-embedding.

Figure 34 shows the simulated results and Figure 35 shows the measured results from the manufactured test coupon. The connectors were not de-embedded from the measured results. The results show a reasonable correlation between measurement and simulation (considering that the connector is part of the measurement but not of the simulation in this case). The manufactured coupon also has a good amplitude and phase matching in the frequency range of 56 GHz to 70 GHz.

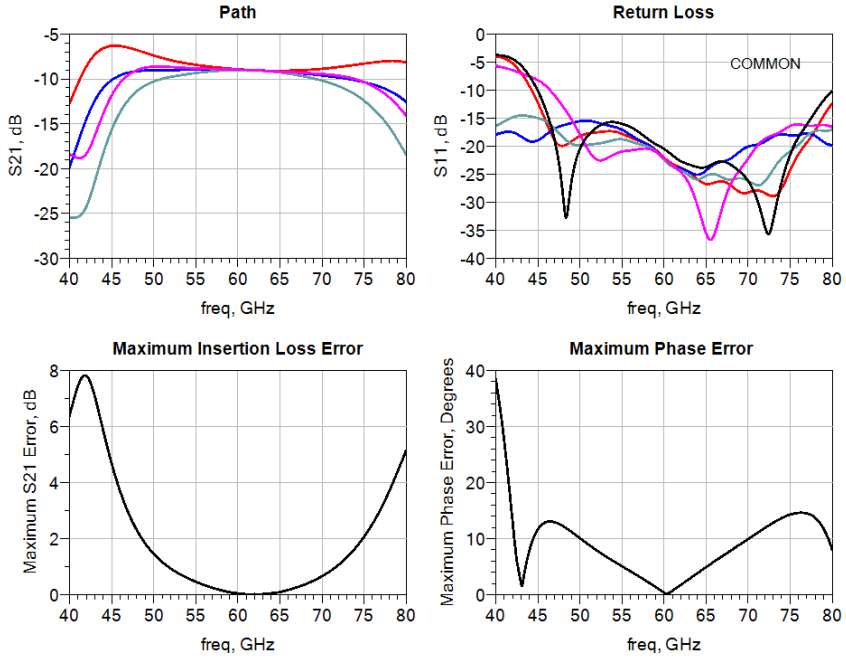


Figure 34: Simulated results from the 1 to 4 combiner/divider based on the hybrid ring topology.

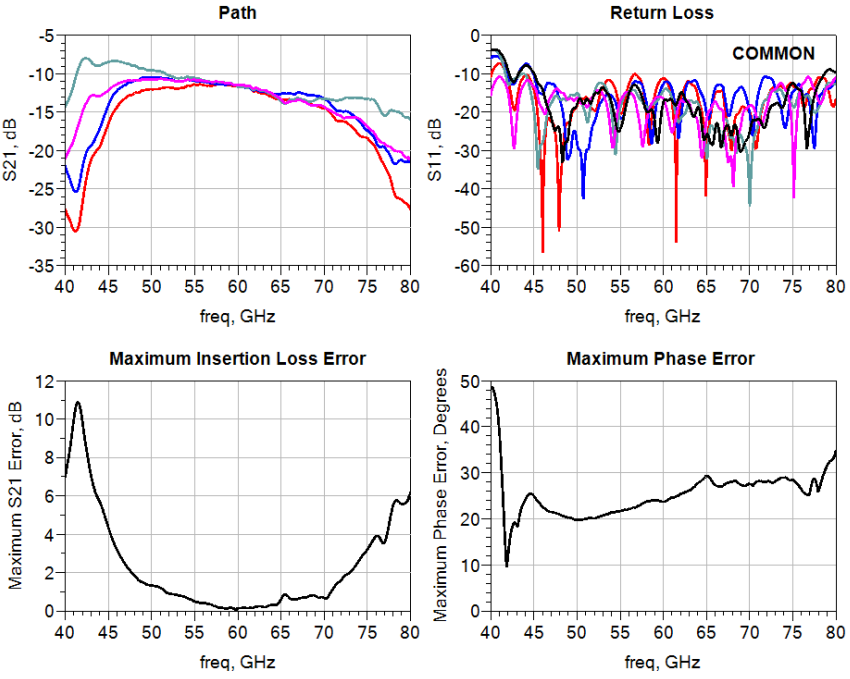


Figure 35: Measured results from the 1 to 4 combiner/divider implemented on a Megtron 6 test coupon.

Figure 36 shows a more detailed comparison for each path insertion loss between simulation and measurement, but this time with the connector and a 15 mm piece of the microstrip de-embedded from the measured data to remove the connector effect. The de-embedding was done using the 2x-thru technique [11] since a 2x-thru de-embedding structure was including on the coupon as can be observed in Figure 33. One can see that the matching to simulation gets worse after 60 GHz. But it is important to note that although the connector effects were removed, as shown in Figure 37, the etched structure does not correspond exactly to the target design which impact the simulation correlation. This is always a major challenge at these mmwave frequencies with standard ATE PCB test fixture manufacturing processes.

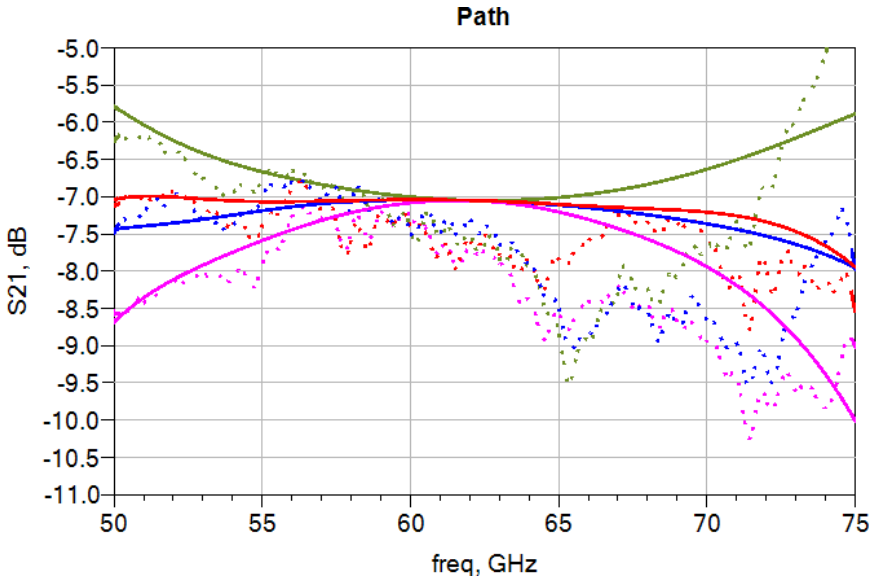


Figure 36: Comparison between simulation and measurement with connectors and 15 mm of microstrip de-embedded from the measurement.

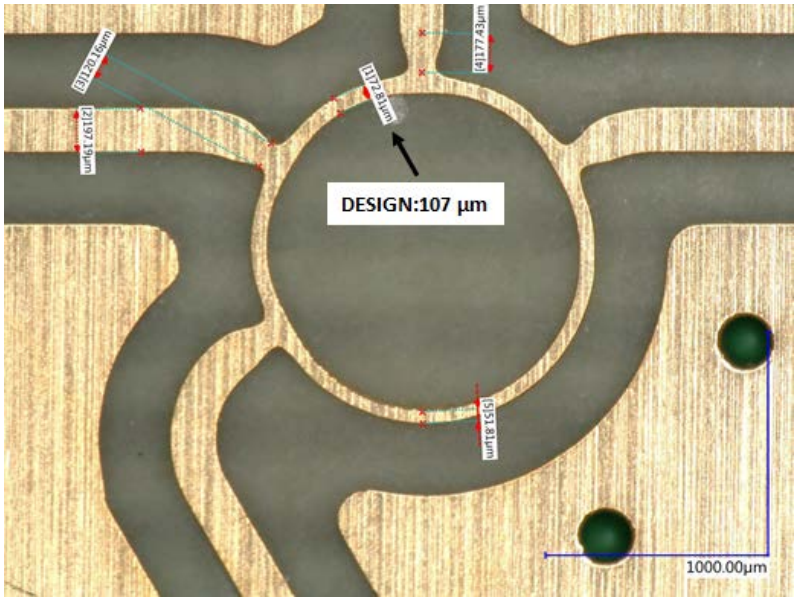


Figure 37: Microscope picture of the hybrid ring at the center of the 1 to 4 combiner/divider test coupon.

Conclusions

This paper has presented a review of some of the combiner/divider design approaches for mmwave applications on ATE systems. Special attention is given to the Wilkinson and hybrid ring (rat-race) combiner approaches because of their ease of implementation on ATE PCB test fixtures. ATE PCB test fixtures present specific challenges which need to be considered in advance when designing a combiner/divider for 5G/WiGig applications. In this context, some of the challenges are new to the ATE test fixture design community. The discussion presented in this paper cannot be considered complete since the importance of the 5G/WiGig applications will for sure generate design improvements and new ideas not only on the combiner/divider topologies but also on the PCB manufacturing.

Acknowledgments

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References

[1] Jong Ik Oh, "mmWave(5G) Test Strategy," in 19th *Korea Conference*, 2018.

[2] D. Pozar, *Microwave Engineering*, 4th ed, Wiley 2011.

[3] E. J. Wilkinson, "An N-Way Hybrid Power Divider," *IRE Transactions on Microwave Theory and Techniques*, Vols. MTT-8, pp. 116-118, 1960.

[4] Frank Gustrau, *Hochfrequenztechnik: Grundlagen der Mobilen Kommunikationstechnik*, Carl Hanser Verlag GmbH & Co. KG, 2013.

[5] M.-S. Kang, Y. Kim and Y.-C. Yoon, "An Unequal Wilkinson Power Divider with A High Dividing Ratio," in *42nd European Microwave Conference*, Amsterdam, 2012.

[6] Seymour B. Cohn, "A Class of Broadband Three-Port TEM-Mode Hybrids," in *IEEE Transactions on Microwave Theory and Techniques*, February 1968.

[7] John Coonrod, "An Overview of Glass-Weave Impact on millimeter-wave PCB Performance," Roger Corporation, 2018.

[8] Jose Moreira and Hubert Werkmann, *An Engineer's Guide to Automated Testing of High-Speed Interfaces*, 2nd ed, Artech House 2016.

[9] Rogers Corporation, "Copper Foil Surface Roughness and its Effect on High Frequency Performance," PCB West, 2016.

[10] Heidi Barnes, Jose Moreira and Manuel Walz, “Non-Destructive Analysis and EM Model Tuning of PCB Signal Traces using the Beatty Standard,” DesignCon, 2017.

[11] Heidi Barnes, Eric Bogatin, Jose Moreira, Jason Ellison, Jim Nadolny, Ching-Chao Huang, Mikheil Tsiklauri, Se-Jung Moon and Volker Herrmann, “A NIST Traceable PCB Kit for Evaluating the Accuracy of De-Embedding Algorithms and Corresponding Metrics”, DesignCon 2018.