# DesignCon 2019

# Simulation and measurement correlation of power supply noise induced jitter for core and digital IP blocks

Hyo-Soon Kang, Intel Corporation
[hyosoon.kang@intel.com]

Guang Chen, Intel Corporation

Ashkan Hashemi, Intel Corporation

Wern Shin Choo, Intel Corporation

David Greenhill, Intel Corporation

Wendem Beyene, Intel Corporation

## Abstract

Power supply noise induced jitter (PSIJ) is one of the major sources of timing uncertainties in high-speed electronic systems. In this paper, the PSIJ analysis methodology for core and IP digital blocks is developed using the frequency-dependent jitter transfer function. The PSIJ analysis results are also correlated with measurements in which clock and data paths are designed in FPGA chips. The frequency-dependent jitter transfer function, which translates voltage noise to jitter, is verified with delay measurement at different voltages. With the integration of the device core operation, power supply noise is generated, and the induced jitter is measured. By changing the noise frequency, the frequency-dependent jitter is correlated with measurements.

## Author(s) Biography

**Hyo-Soon Kang** is a Signal and Power Integrity engineer at Intel Corporation. His responsibilities include the timing budgeting of high-speed links and the power supply noise induced jitter analysis on analog interface and core logic. From 2009 to 2017, he was with Package Development Team in Samsung Electronics Ltd., Korea. His research interests were in the area of signal integrity (SI) and power integrity (PI) of semiconductor packages. He received the B.S., M.S., and Ph.D. degrees in Electrical and Electronic Engineering from Yonsei University, Korea, in 2002, 2004, and 2009, respectively.

**Guang Chen** is a design engineer with Silicon Systems Development Department at the Programmable Solutions Group (PSG), Intel Corporation, where he is responsible for driving signal/power integrity co-design effort for the key FPGA products with focus on both silicon and system level power integrity solutions. Prior to this, he was with Technical Service Dept. at Altera Corporation, providing system SI/PI solutions for customer Altera FPGA applications. He holds a Ph.D. in Electrical Engineering from University of Arizona. His professional interests include power integrity and signal integrity, high-speed interconnects and channel modeling.

**Ashkan Hashemi** is an SoC design engineer at Intel Programmable Solution Group (PSG). His responsibilities include both chip and system level signal/power integrity-related analysis of flagship FPGA products as well as Intel PSG synergy products. He received the Ph.D. degree in electrical engineering from the Missouri University of Science and Technology (Missouri S&T), Rolla, MO, USA, in 2016.

**Wern Shin Choo** is a validation engineer with Platform Validation Engineering Department at the Programmable Solutions Group (PSG), Intel Corporation, where he is responsible for validating the signal/power integrity for the key FPGA products on both silicon and system level power integrity solutions. He received the B.S. degrees Electronic Engineering from Multimedia University, Malaysia in 2011.

**David Greenhill** is a Senior Director at Intel Programmable Solutions Group. He currently leads 7nm and 14nm FPGA design teams. He previously worked on mobile processors at TI and server processors at Sun Microsystems. At Sun he worked on the development of 8 generations of Sparc processors and server systems. He has served on the ISSCC program committee. He holds a BSc in Physics from Imperial College, London.

**Wendem Beyene** received his B.S. and M.S. degrees in Electrical Engineering from Columbia University, and his Ph.D. degree in Electrical and Computer Engineering from University of Illinois at Urbana-Champaign. In the past, he was employed by IBM, Hewlett-Packard, Agilent Technologies and Rambus Inc. He is currently with Intel Corporation working on modeling and analysis of power distribution and signaling systems of core and I/O subsystems of FPGA chips.

# I. Introduction

Power supply noise induced jitter (PSIJ) analysis methodology have been widely studied for the timing analysis of high-speed serial and parallel interfaces and digital core timing [1-2]. In the static timing analysis (STA), delay variant due to voltage noise is applied in the analysis and this approach has pessimism which degrades Fmax severely. To overcome this pessimism, clock/data path-based jitter transfer function, dynamic noise modeling and jitter calculation methodologies with consideration of jitter tracking was proposed [1].

The PSIJ analysis consists of modeling of system-level power distribution network (PDN), generation of current noise waveforms, and calculation of frequency-dependent jitter transfer function. To verify the accuracy of the PSIJ methodology, jitter transfer function correlation between path-based analysis and HSPICE simulation was performed in [1,3], however, direct measurement correlations of jitters have not been reported as of yet.

This paper demonstrates simulation and measurement correlation results of PSIJ for core and digital IP blocks. The overall PSIJ analysis methodology and timing impact to clock and data paths are described in the next section. For the measurement correlations, an Intel field-programmable gate array (FPGA) chip is used to design clock and the data paths [4]. With the integration of core operating circuits in the FPGA design, core noises with several operating frequencies were generated and modeled taking advantage the FPGA programmability. By varying the noise frequency, period jitter of clock signal and the *Fmax* degradation of data path which are dependent on frequency can be measured and correlated.

# II. Power Supply Noise Induce Jitter

*1. Introduction to Power Supply Noise Induced Jitter Analysis*

PSIJ analysis consists of several simulation and modeling steps as shown in Figure 1. For the accurate power noise modeling, accurate modeling of the system-level power distribution network (PDN) is required including on-die, package and board models. With the current profile the circuit consumes, voltage noise can be calculated by multiplication of impedance and current spectrums. The current profile can be obtained by circuit simulations of the completed design, if available, or equation-based modeling by considering the operating frequency and circuit activity scenarios [1].

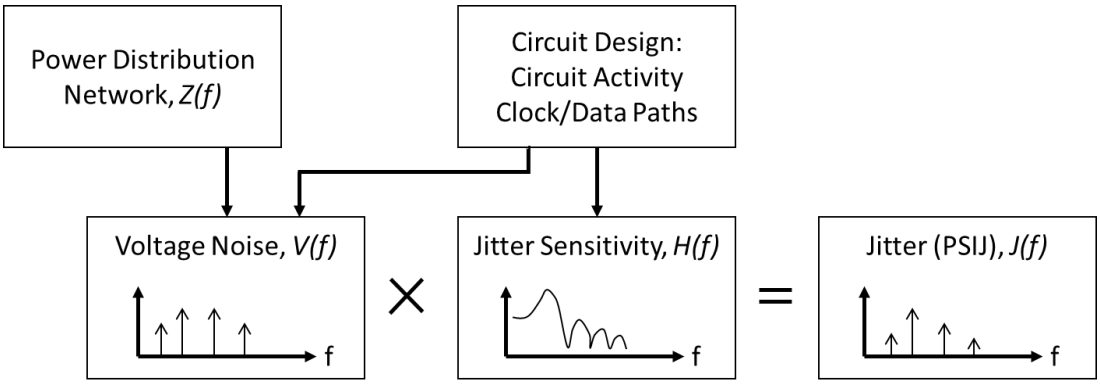



**Figure 1 Simulation flow of power supply noise induced jitter (PSIJ) analysis**

The jitter transfer function can be obtained by circuit simulations by injecting the power supply of the subcircuit with frequency-varying sinusoidal noise and measuring jitter response at the desired output. It can also be analytically derived by an equation (1) for open-loop subcircuit paths [1]. The DC delay sensitivity ($H_0$), is calculated from two different delay values at different voltages, and open-loop delay ($\tau_d$) of the subcircuit path, and the frequency-dependent jitter transfer function can be easily calculated as:

$$H(f) = \frac{j}{2\pi f \tau_d} H_0 \left[1 - e^{-j2\pi f \tau_d}\right], \quad \text{where} \quad H_0 = \frac{\tau_{Vmin} - \tau_{Vmax.}}{Vmax - Vmin} \tag{1}$$

The magnitude of the jitter sensitivity can be simplified as:

$$|H(f)| = H_0 \left|\frac{\sin(\pi f \tau_d)}{\pi f \tau_d}\right| = H_0 |\mathrm{sinc}(\pi f \tau_d)|. \tag{2}$$

Figure 2 shows typical plots of jitter transfer functions derived from equation (2) with different path delay values. When the path delay is large, the DC sensitivity ($H_0$) is high, thus more sensitive to the low-frequency noise. However, the large path delay induces the low-frequency null point in the frequency-dependent jitter transfer function which can be less-sensitive to high-frequency noise. Therefore, large path delay does not always induce the worst-case jitter as in STA in which longer delay means larger jitter impact.

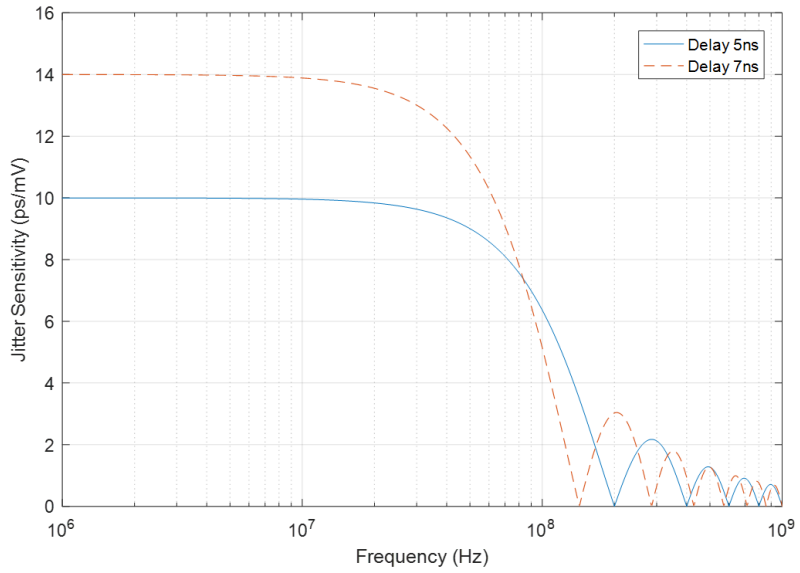



**Figure 2 Frequency-dependent jitter transfer functions**

*2. Period jitter impact due to power supply noise*

For timing analysis of clock network, period jitter (PJ) is an important parameter that represents the clock signal quality. The jitter transfer function of period jitter can be expressed by equation (3) and (4) [1]. By the definition of period jitter, the deviation of the clock period, the jitter transfer function of PJ can be calculated by subtracting the jitter of consecutive edges: rise-to-rise or fall-to-fall edge:

$$H_{period}(f) = H(f)(1 - e^{-j2\pi f T_{clk}}). \quad (3)$$

The magnitude of the jitter sensitivity can be simplified as:

$$\left|H_{period}(f)\right| = 2H_0|\mathrm{sinc}(\pi f \tau_d)| \cdot |\sin(\pi f T_{clk})| \quad (4)$$

Figure 3 shows the time interval error (TIE), which can be calculated by open-path sensitivity equation (2), and period jitter sensitivities by equation (4). Due to the jitter tracking effect, the jitter sensitivity has low value in low frequency region, thus the low-frequency noise impact to period jitter becomes smaller.

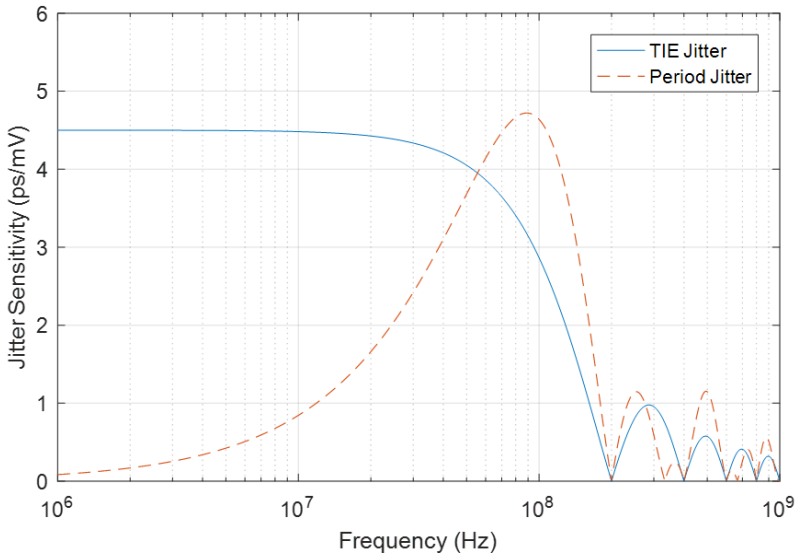


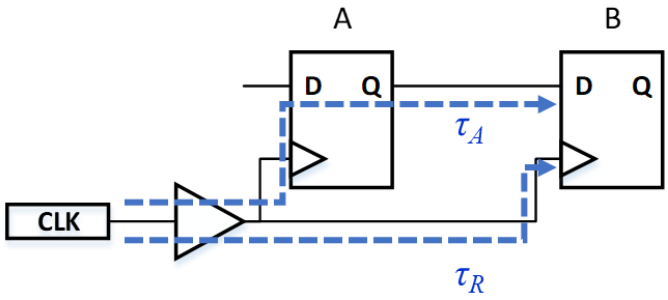

**Figure 3 Jitter transfer function for Period Jitter (PJ) when clock delay is 5ns, DC sensitivity is 4.5ps/mV, and clock frequency is 333MHz.**

*3. Timing impact to data paths*

In the digital blocks, clock is distributed and triggered for data signals as shown in Figure 4. The clock and data timing relationships for setup and hold time are depicted in Figure 5. For setup time, the data is captured by the 1-cycle next clock edge from the launch edge. For hold time, the data is capture with the same clock edge which generated data. With these relationships, the jitter transfer functions for setup and hold time can be expressed by equations (5) and (6) [1].

$$H_{setup}(f) = \frac{j}{2\pi f \tau_A} H_0^A \left[1 - e^{-j2\pi f \tau_A}\right] - \frac{j}{2\pi f \tau_R} H_0^R \left[1 - e^{-j2\pi f \tau_R}\right] e^{-j2\pi f T_{clk}} \quad (5)$$

$$H_{hold}(f) = \frac{j}{2\pi f \tau_A} H_0^A \left[1 - e^{-j2\pi f \tau_A}\right] - \frac{j}{2\pi f \tau_R} H_0^R \left[1 - e^{-j2\pi f \tau_R}\right] \quad (6)$$




$\tau_A$: time delay for arrival path
$\tau_R$: time delay for required path

**Figure 4 Block diagram of mesochronous clocking scheme**

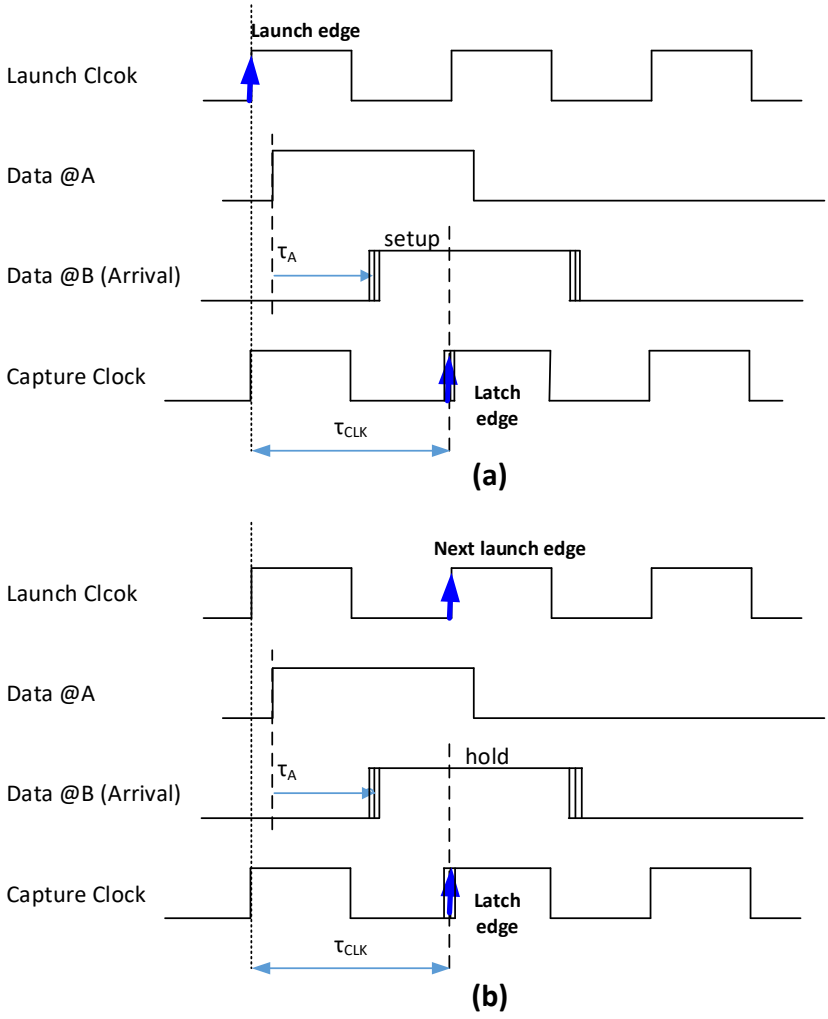



**Figure 5 Clock and data timing diagram of launch and capture clocks for (a) setup and (b) hold time**

## III. FPGA Designs and Measurements

To measure power supply noise induced jitter and correlate it with simulations, the Intel Stratix 10 FPGA chip is used [4]. By programming the FPGA chip, several clock and data path designs are implemented, and the core logic operation is integrated for noise generation.

*1. Clock path design*

For the measurement of clock PSIJ, three different clock routing paths are designed in the FPGA as shown in Figure 6. All the designs use the same clock PLL source and output buffer to compare only the clock routing length effect. Figure 7 describes the clock routing path. The clock generated in the PLL go through the global clock network and then the output buffers in order to measure the signal jitter using an oscilloscope.

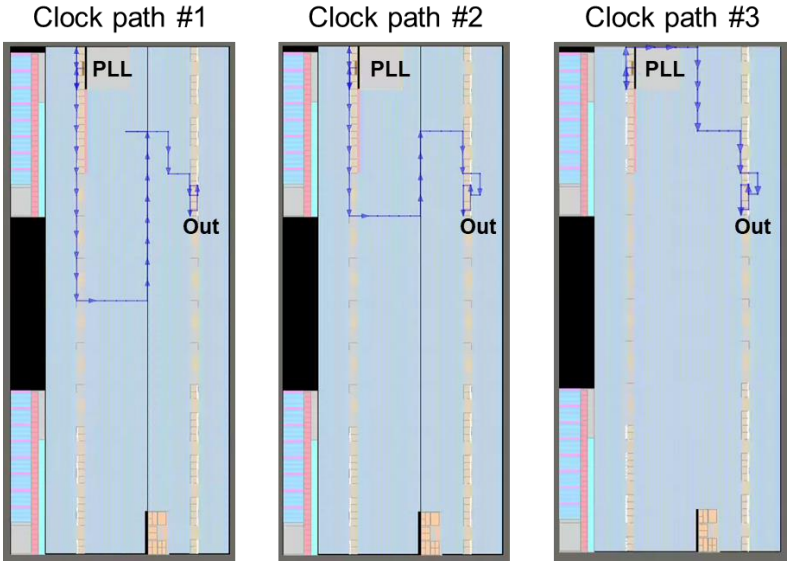



**Figure 6 FPGA designs for clock jitter measurements: different clock path routings for 3 different latencies**

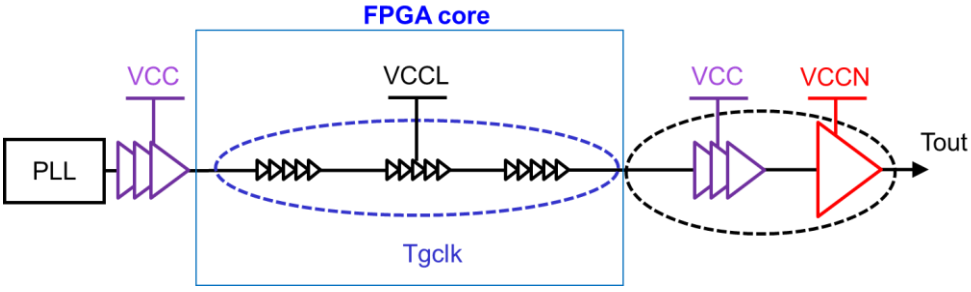
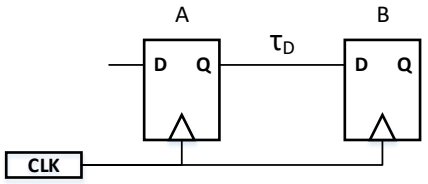


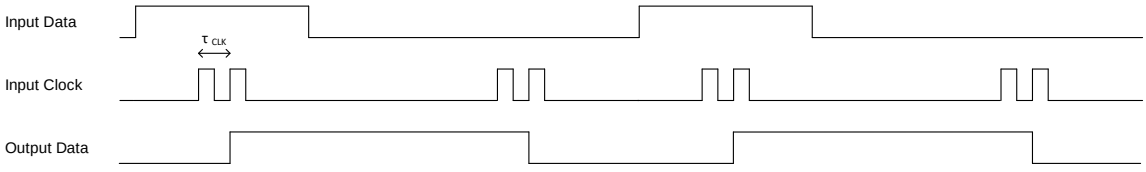

**Figure 7 Clock path from PLL to output buffer**

*2. Register-to-Register designs and Fmax measurements*

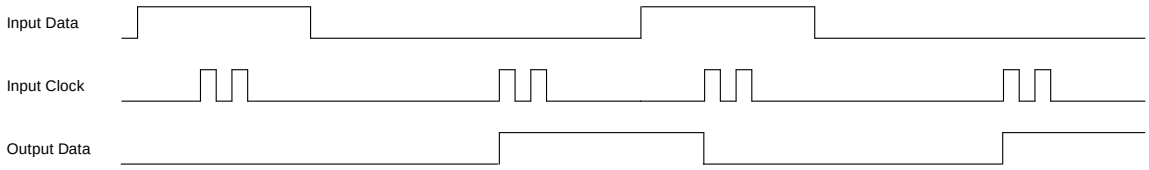
In the FPGA, register-to-register designs are implemented to measure data path delays. Figure 8 shows the block diagram and input/output data pulse timing which depends on the clock period and data delay relationship. The same clock signal is applied to the two registers and clock/data patterns are fixed in order to determine data transfer pass or fail conditions. If the data delay ($\tau_D$) is smaller than the clock period ($\tau_{CLK}$), the data can be transferred to output register (register B). However, if the data delay ($\tau_D$) is larger than clock period ($\tau_{CLK}$), the data cannot be captured by clock pulses and data cannot be transferred. In the measurements, data delay is fixed by the register-to-register design, thus clock frequency ($\tau_{CLK}$) is varied. At the beginning, the clock frequency is set to low ($\tau_{CLK} > \tau_D$) and data can be transferred correctly. With increasing the frequency, the data transfer start to fail when the clock period become lower so that the data delay ($\tau_{CLK} \approx \tau_D$). The maximum frequency right before data transfer starts to fail can be defined as *Fmax* ($1/\tau_D$).




(a) Register-to-register design with data delay, $\tau_D$




(b) $\tau_D < \tau_{CLK}$ : Transfer pass




(c) $\tau_D > \tau_{CLK}$ : Transfer fail

**Figure 8 Register-to-register design and input clock/data pulse patterns for data delay measurements. Data transfer pass (a) and fail (b) conditions regarding the clock period and data delay relationship.**

*3. Noise generations and measurements*

To measure the power supply noise impact to the jitter, a large number of programmable core logics are configured as grey code counter (GCC) design in the FPGA core, which is toggled by a single huge clock tree. As this GCC design being clocked, a periodical noise is generated on the FPGA core and this noise is used for the voltage noise correlation and frequency-dependent jitter transfer function characterization. By changing the input reference clock frequency, the noise frequency can be controlled. The generated noise waveform and noise amplitude are being logged and measured through the sense line of the FPGA core voltage rail using an oscilloscope, and later on being used to correlate with simulated noise waveform.

# IV. Simulation and Measurement Correlation

*1. Voltage noise modeling with correlation of measurement*

Voltage noise model is generated by system-level power delivery network modeling and current profile generation. Figure 9 shows the simplified schematic of FPGA core PDN. With consideration of the FPGA floor plan, the core PDN is divided into 3-zones and modeled accordingly. For the current profile modeling of the core power, triangular shape is used in our analysis. From the measurement of dynamic power of the FPGA core, charge per cycle is calculated and used for current profile modeling. The total area of triangular current profiles in Figure 10 is same with the calculated charge per cycle.

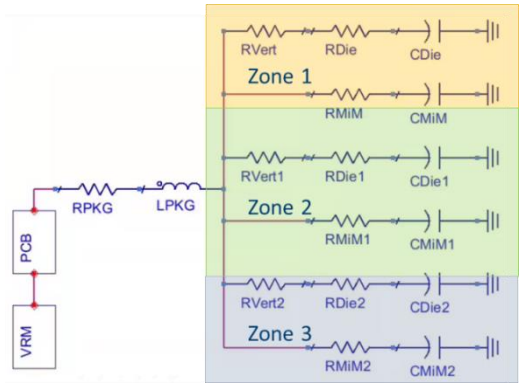



**Figure 9 Simplified schematic of the FPGA core PDN.**

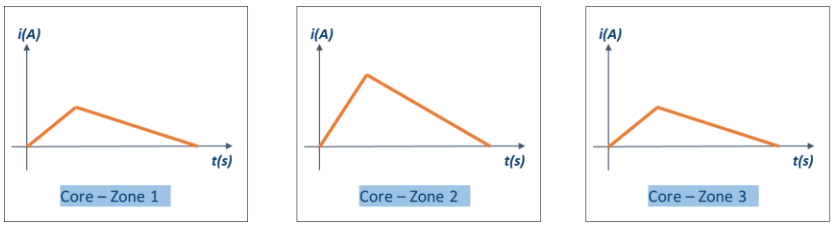
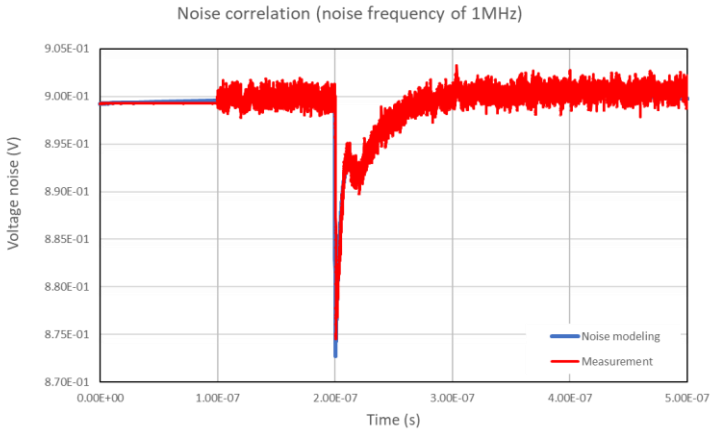
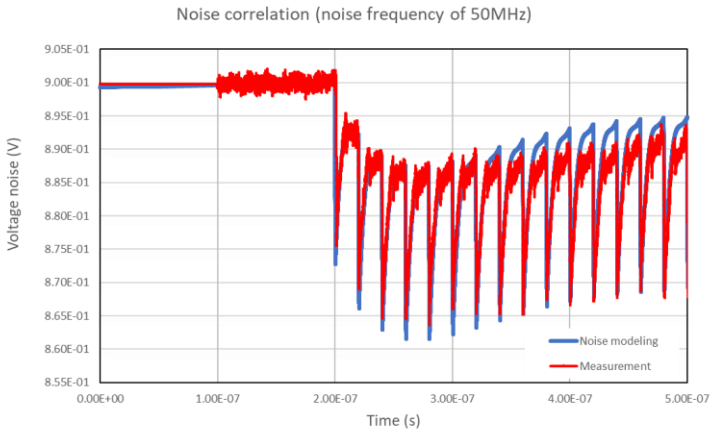



**Figure 10 Current profile modeling**

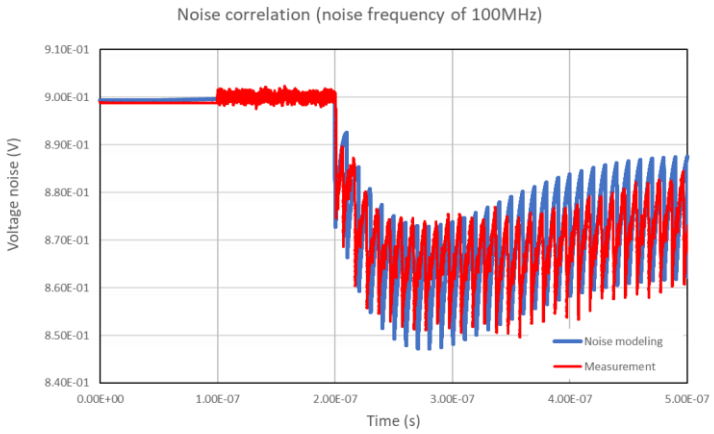
With the PDN model and generated current profile, voltage noise is simulated and compared with the measured waveform. Figure 11 shows the voltage noise comparison between modeling and measurement at different noise frequencies. It is seen that the first droop and overall shape are well matched, however there are discrepancy due to low-frequency noise profile caused by the board PDN.




(a) Noise frequency of 1MHz




(b) Noise frequency of 50MHz




(c) Noise frequency of 100MHz

**Figure 11 Voltage noise comparison between simulation and measurement at different noise frequency conditions**

*2. Clock path jitter correlation*

For the analysis of PSIJ, jitter transfer function as well as voltage noise profile is required as in equation (1). Jitter transfer function can be obtained by DC delay sensitivity and absolute delay of clock path. To measure DC delay sensitivity, applied DC voltage is changed and the relative output pulse delay differences to nominal voltage delay are measured. The DC delay sensitivity is then being calculated by the formula, $DC\ Delay\ Sensitivity = \frac{\Delta \text{delay}}{\Delta voltage}$. Figure 12 shows two clock signal waveforms at 333MHz measured by an oscilloscope with different DC voltages. To correlate the clock path delay and DC sensitivity, a Static Timing Analysis (STA) tool, Intel Quartus TimeQuest Timing Analyzer, is used and the data is compared with measured sensitivity in Table 1. With the comparison of DC sensitivity from STA and measurement, it is seen that the STA data is larger than the actual device measurement result due to the process variation existed in fabricated devices. For the input of PSIJ analysis, absolute delay and sensitivity values from TimeQuest STA are scaled by -20% with the comparison data from measurement and STA as shown in the Delta in Table 1. Using the equation (3), the period jitter transfer function is calculated, and frequency-dependent jitter is simulated with the voltage noise profile, which is correlated with measurement in Figure 11. With the periodic noise generation from the GCC logics toggle, period jitters with respect to noise frequency are expected to follow frequency-dependent jitter transfer functions. Figure 13 shows period jitter comparison between the simulations and measurements. The simulated jitter as a function of noise frequency is well correlated with the measurement result, thus the methodology of jitter transfer function analysis is verified with measurements. Because the clock frequency of 333MHz is used, the jitter transfer function has null point at this frequency as in equation (3), thus PSIJ becomes smaller with the noise frequency of 333MHz. The discrepancy between simulation and measurements is due to the different jitter components included in the simulation and measurement. The simulation only includes the PSIJ, whereas the measurement captures all the circuit jitters including PLL PJ.

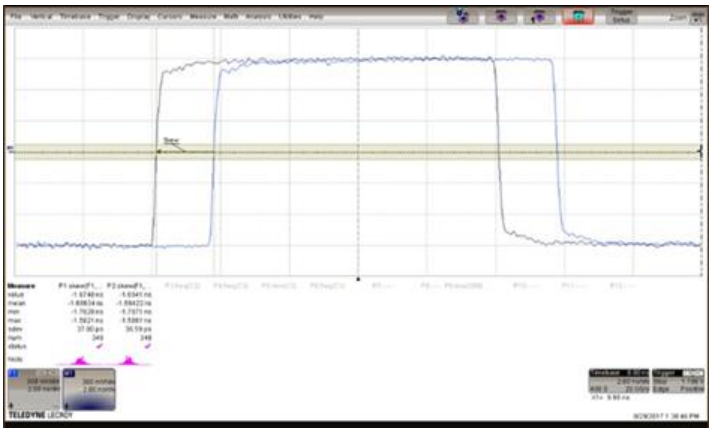
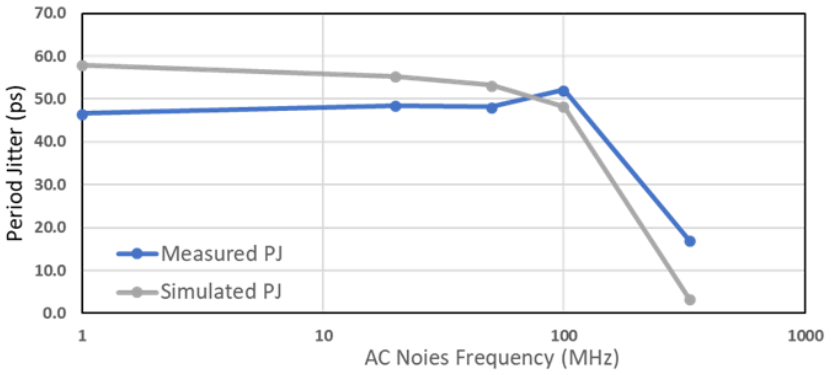


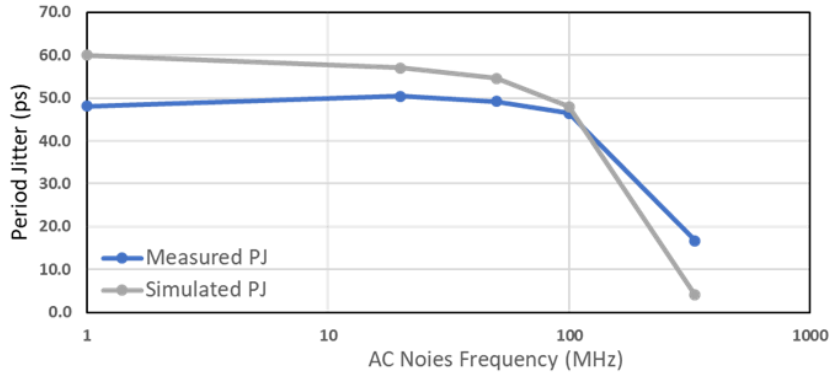
**Figure 12 Delay sensitivity measurement with oscilloscope**

| Clock path design | TimeQuest Delay Sensitivity (ps/mV) | Measurement Delay Sensitivity (ps/mV) | Delta |
|---|---|---|---|
| Path #1 | 12.79 | 10.51 | -18% |
| Path #2 | 14.54 | 11.66 | -20% |
| Path #3 | 16.54 | 13.09 | -21% |

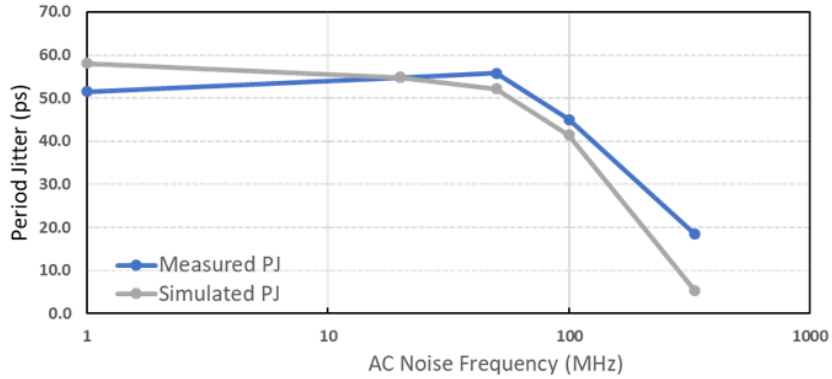
**Table 1 Delay sensitivity comparison between Time Quest and measurement**




(a) PSIJ correlation for clock path #1




(b) PSIJ correlation for clock path #2




(3) PSIJ correlation for clock path #3

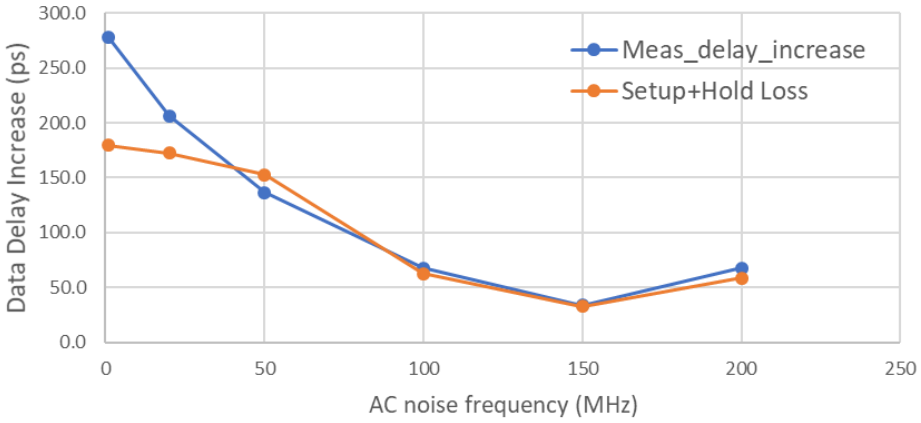
**Figure 13 Period jitter correlation with varying noise frequency**

*3. Data path timing impact correlation*

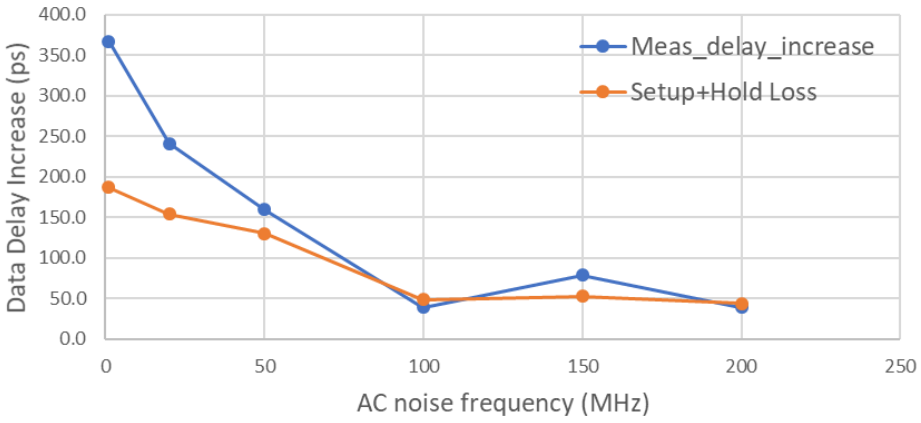
Using the register-to-register designs shown in Figure 8, power supply noise impact to Fmax ($1/\tau_D$) is characterized. As described before, data path delay ($\tau_D$) can be calculated by measuring the maximum frequency (*Fmax)* at which data can be transferred. Table 2 is measured data path delay at different voltages. Data setup and hold time loss due to power supply noise can be simulated with jitter transfer function equations (5), (6) and voltage noise profile shown in Figure 11. In the equation (5) and (6), another required parameters for PSIJ analysis are clock delay and dc sensitivity. Similar to the clock path correlation methodology, Intel Quartus TimeQuest Timing Analyzer is used to obtain the clock path information. In our register-to-register design, clock path delay is 5.5ns and DC delay sensitivity is 5.5ps/mV at DC voltage of 0.84V. Based on the clock and data delays/sensitivities of the register-to-register design, setup and hold time loss due to core voltage noise is simulated and compared with measured data, which is delay increase due to the noise, as shown in Figure 14. The frequency-dependent characteristics of setup and hold time losses have similar tendency of jitter transfer functions because of the generated periodic core noise. As shown in Figure 14, the frequency-dependent jitter characteristics of simulation and measurement have similarity, however there are large discrepancies for low frequency noise (1MHz and 20MHz). One explanation for these discrepancies is jitter accumulation due to low-frequency harmonic noise, however further research to figure out the origin is required.

| Voltage | Data path delay (ns) |
|---|---|
| 0.75 | 8.96 |
| 0.79 | 8.31 |
| 0.84 | 7.72 |

**Table 2 Measured data path delay at different voltages**




(a) Data delay impact at voltage of 840mV




(b) Data delay impact at voltage of 790mV

**Figure 14 Comparison of data delay increase (Fmax degradation) from simulation and measurement**

## IV. Conclusions

The simulation and measurement correlations of power supply noise induced jitter are presented. Using the FPGA, clock and/or data path designs are implemented, and core logic operation is integrated to generate noise. Major benefit of using the FPGA is the flexibility of design and controllability of noise profile. From the global clock path design, period jitter caused by periodic noise is measured and compared with the simulation results. The tendencies of period jitter with respect to noise frequency are well matched for simulation and measurement. With the register-to-register design, data path increases (*Fmax* degradation) due to core noise are characterized. The frequency dependent characteristics of simulation and measurement have similar trend, however discrepancies at low frequency noise need to be further analyzed. From these correlation works, the PSIJ analysis methodology including jitter transfer function accuracy can be experimentally verified.

## References


[1] T. Rahal-Arabi, G. Taylor, M. Ma, and C. Webb, "Design and validation of the Pentium® III and Pentium® 4 processors power delivery," *VLSI Symposium*, June 2002, pp. 220-223.

[2] R. Schmitt, et al., "Analysis of supply noise induced jitter in Gigabit I/O interfaces," in IEC DesignCon, Santa Clara, CA, 2007.

[3] Y. Shim and D. Oh, "System Level Modeling of Timing Margin Loss Due to Dynamic Supply Noise for High-Speed Clock Forwarding Interface," *IEEE Transactions on Electromagnetic Compatibility*, Vol. 58, No. 4, Aug. 2016, pp. 1349-1358.

[4] https://www.intel.com/content/www/us/en/products/programmable/fpga/stratix-10.html