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An Efficient Power and Signal Integrity Combo Simulation and Correlation for DDR4 and Beyond

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Abstract

The demands on system memories have been steadily increasing as new applications such as machine learning for artificial intelligence are emerging. Memory technology scales by improving peak performance and increasing clock frequency to maximize bandwidth, while exploiting process technology to reduce operating voltage. For example, DDR3 VDDQ is 1.5V and DDR4 VDDQ is 1.2V. This reduction in power supply headroom, coupled with additional noise introduced on the power rails due to the increased data rate can adversely affect the overall system performance. Therefore, understanding the power supply integrity together with signal integrity is ever more important and critical as the system scales to DDR4 top speed and beyond.

This paper proposes an alternative to the existing traditional method for performing a combined power and signal integrity simulation. The existing method, the Alpha method, usually leads to conservative estimation of system timing. In addition, this traditional method does not reflect actual power noise according to the real usage model. This paper proposes an efficient combo simulation by injecting realistic power supply noise tones according to the system usage model. The power supply noise that causes output jitter will be modeled as a power induced jitter transfer function. The power network is based on a real design and the stimulus, which forms the aggressor disturbance on the victim lines, is based on real usage model from the memory controller unit. The paper will show the method to optimally capture the necessary feature behavior for the modeling. The induced jitter will then be combined with signal integrity simulation to analyze the aggregated signal jitter impact to the system.

Key Terms—DDR4 IO interface, Power Supply Induced Jitter Transfer, Jitter Specifications

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Juan Wang is a Staff Signal Integrity engineer at Xilinx Inc. She has been focusing on memory interface timing analysis such as DDR4/DDR3/RLDRAM3 and corresponding lab verification. Prior to Xilinx, she worked for Juniper as signal integrity engineer for more than 5 years supporting system design 10GE/XFI/XLAUI/SFI/sGMII/rGMII/PCIE/DDR3 signal integrity modeling, simulation and measurements. Juan received her MSEE from University of Missouri-Rolla and Tsinghua University.

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1. Introduction

The demands on system memories have been steadily increasing as new applications such as machine learning for artificial intelligence are emerging. Memory usages can range from high performance requirement to lower power applications, as illustrates in Figure 1. However, the performance of the memory devices has been improving in order to meet the system performance requirement across the usage spectrum.

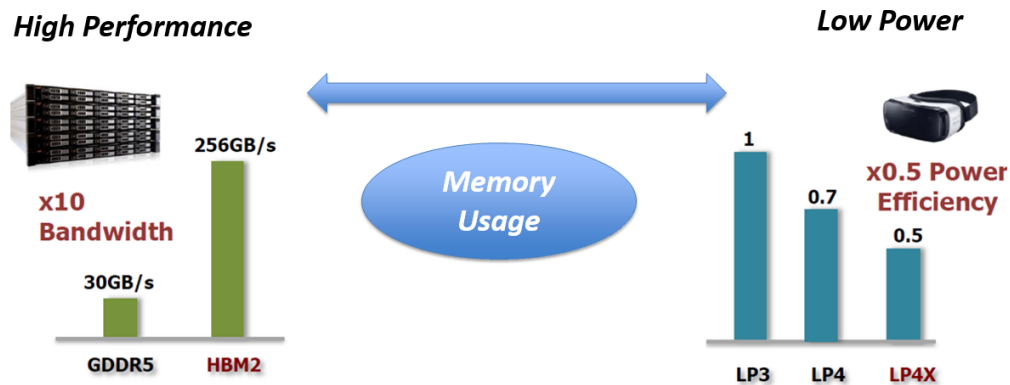


Figure 1 Memory System Usage

Memory technology scales by enhancing peak performance and increasing clock frequency to maximize bandwidth (as shown in Figure 2), while exploiting process technology to reduce operating voltage (as shown in Figure 3). For example, DDR3 VDDQ is 1.5V and DDR4 VDDQ is 1.2V. This reduction in power supply headroom, coupled with additional noise introduced on the power rails due to the increased data rate can adversely affect the overall system performance. In addition, the per-die density of DRAM capacity has been increasing steadily as shown in Figure 4. Therefore, understanding the power supply integrity together with signal integrity is ever more important and critical as the system scales to DDR4 top speed and beyond.

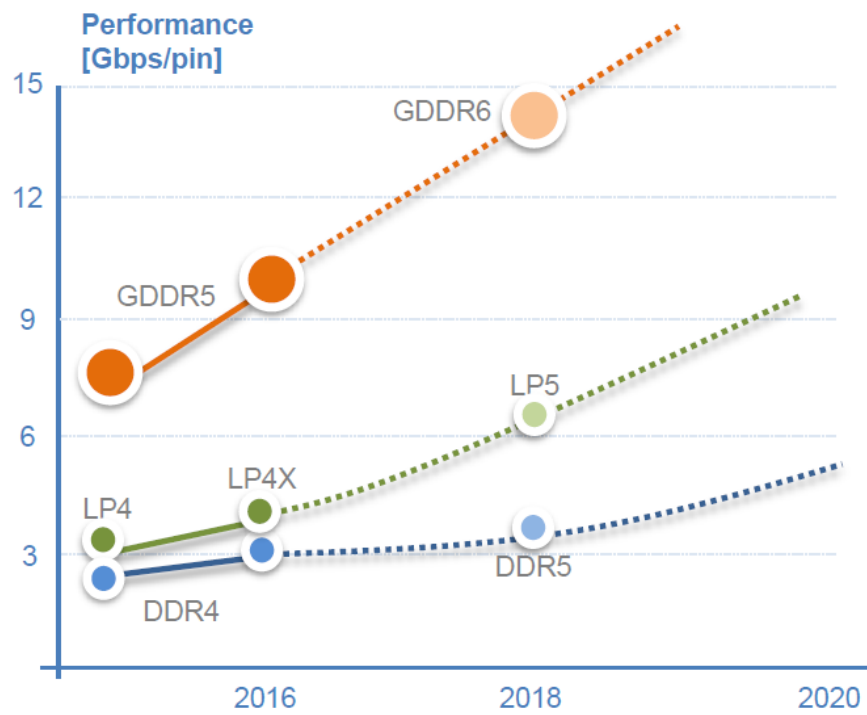


Figure 2 Memory IO Speed Trends and Projection across Different Standards [1]

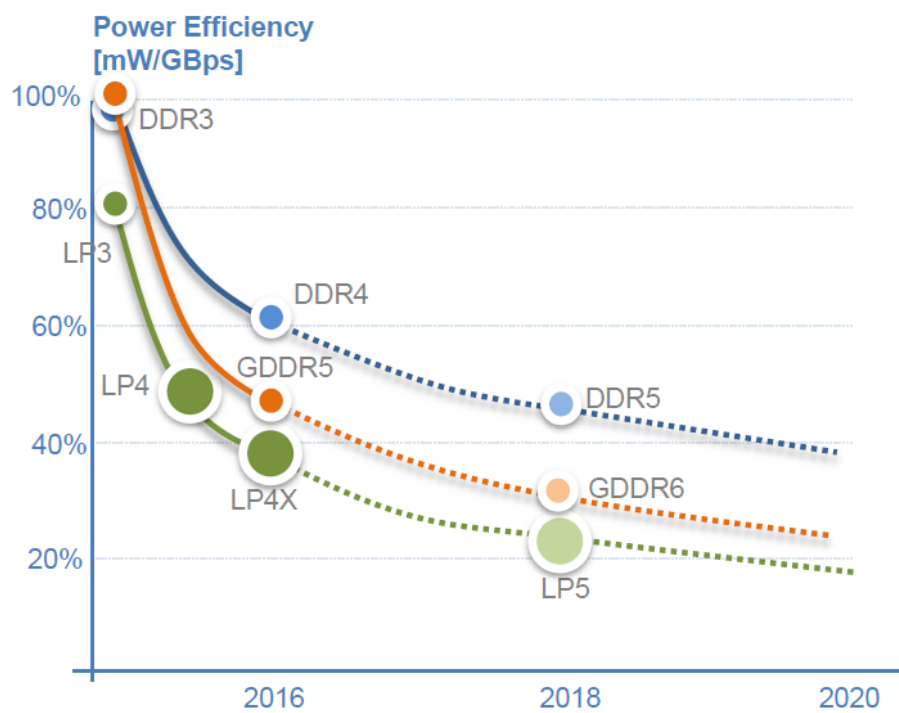


Figure 3 Power Efficiency Trends [1]

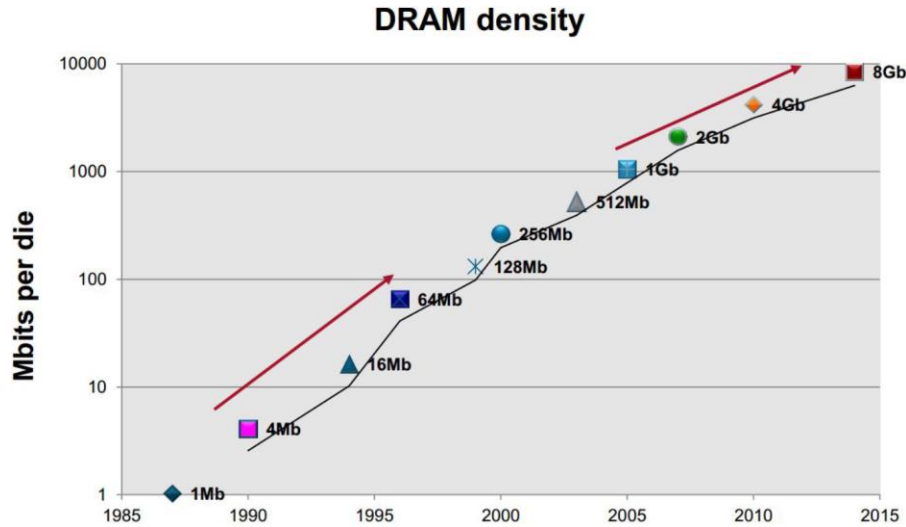


Figure 4 Monolithic Memory Density Trends [2]

This paper proposes an alternative to the existing traditional method for performing a combined power and signal integrity simulation. The existing method, the Alpha method, usually leads to conservative estimation of system timing. In addition, this traditional method does not reflect actual power noise according to the real usage model. This paper proposes an efficient combo simulation by injecting realistic power supply noise tones according to the system usage model. The power supply noise that causes output jitter will be modeled as a power induced jitter transfer function. The power network is based on a real design and the stimulus, which forms the aggressor disturbance on the victim lines, is based on real usage model from the memory controller unit. The paper will show the method to optimally capture the necessary feature behavior for the modeling. The induced jitter will then be combined with signal integrity simulation to analyze the aggregated signal jitter impact to the system.

Section 2 will describes the traditional jitter estimation method and how it leads to more conservative timing jitter estimation. Then, section 3 will show how to combine the power noise impact to channel jitter simulation. In this section, the IO power supply jitter response to supply voltage noise will be discussed which enables a simplified modeling approach to capture the power noise effects onto the channel jitter. The jitter effects under realistic memory operations will be compared and discussed. Section 4 will show the lab measurement and correlation. Section 5 will summarize the key points.

2. Traditional Jitter Estimation

Traditionally, the channel jitter and power noise induced jitter are analyzed separately. Then, the jitter quantities are added together.

For the power noise, a method called alpha factor model is used to estimate circuit buffer jitter induced by power supply noise. For a selected circuit block, the nominal circuit

delay under nominal supply voltage is represented by t_d . When the supply voltage experiences a change of voltage ΔV , the circuit delay will become $t_d + \Delta t$. The nominalized power supply induced jitter sensitivity (α) is shown below [3],

$$\alpha = \frac{\Delta t / t_d}{\Delta V / V_{dd}} \quad (1)$$

The change of the delay is regarded as the power supply induced jitter. The change of the voltage is assumed to be DC level and can be used as the power droop specification. Then the power noise induced jitter under this worst case DC level will be calculated as

$$\Delta t = \alpha \cdot \Delta V \cdot (t_d / V_{dd}) \quad (2)$$

For system timing analysis, the configuration will be simulated for a selected platform. The signal jitter obtained from the channel simulation will be added to the circuit power noise induced jitter. If the total jitter is less than the system jitter specification, the system should be within the timing budget. Then, the ΔV will become the allowed voltage droop specification under any operation conditions.

Since the power induced jitter is assumed to be a static DC droop, the estimation of this jitter is pessimistic. As the operation frequency scales up, this conservative estimation may lead to over design.

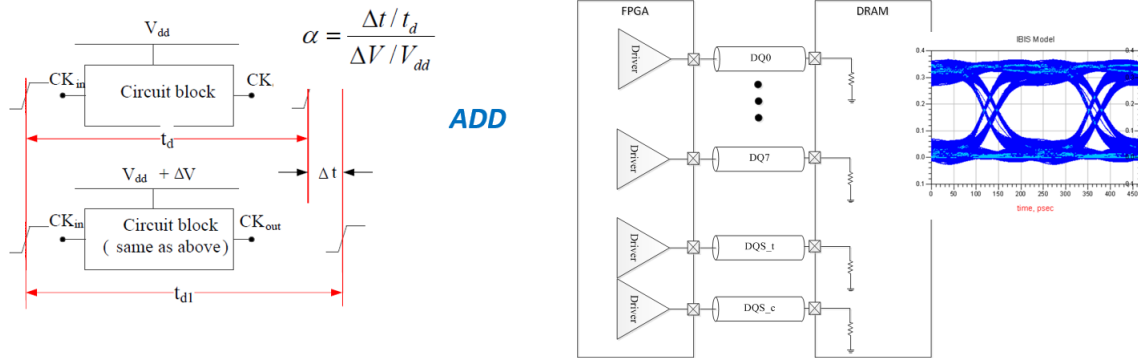


Figure 5 Jitter estimation based on Alpha Method [3]

3. PDN Model with Element IO Model Concepts

The section will describe the power induced jitter with channel jitter simulation modeling.

Figure 6 shows a single stage inverting IO buffer transmitting a Logic One and a Logic Zero. When power noise is present, the output transition will be displaced from its nominal output transition position causing jitter.

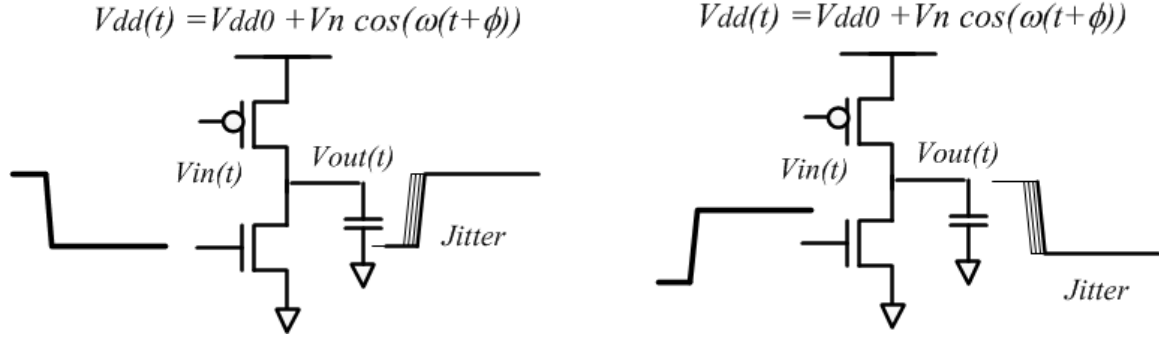


Figure 6 Power Noise Induced IO Buffer Jitter

In previous publication, Hwang et.al.[5] provided a closed form analytical expression that related power and ground noise to single ended buffer. The power noise induced jitter transfer functions due to power noise that has a noise frequency of ω is listed below.

$$H_{H \rightarrow L}^{Power}(\omega) = \frac{C}{G_{mn} + \lambda_n} \frac{1}{\sqrt{C^2 r_{onp}^2 \omega^2 + 1}} \frac{1}{V_{dd}} \times \angle(-atan2(Cr_{onp}^2, 1)) \quad (3)$$

$$H_{L \rightarrow H}^{Power}(\omega) = \frac{C}{\frac{1}{2\lambda_p} + G_{mp}} \frac{(\lambda_p + g_{mp})}{\lambda_p^2 + C^2 \omega^2} \frac{1}{V_{dd}} \times \sqrt{A(\omega)^2 + B(\omega)^2} \angle(\pi - atan2(B(\omega), A(\omega))) \quad (4)$$

where G_{mn} is the large signal gain, λ_n , λ_p are the channel modulation parameters g_{mp} trans-conductance of the buffer, ω is the noise frequency and C is the capacitance load. The expressions $a(\omega)$ and $B(\omega)$ are related to IO buffer parameters as follows

$$A(\omega) = \lambda_p \cos \omega t + C \omega \sin \omega t - \lambda_p e^{-\frac{\lambda_p}{C} t}$$

$$B(\omega) = -\lambda_p \sin \omega t + C \omega \cos \omega t - C \omega e^{-\frac{\lambda_p}{C} t} \quad (5)$$

From equation (3), one can observe that the power noise jitter transfer function is inversely proportional to the large signal gain G_{mn} and the transfer function has a low pass filter characteristic versus noise frequency.

The Logic Low-to-High Power noise jitter transfer function is plotted in Figure 7. As the large signal gain increases, the power noise jitter transfer level in low frequency range reduces. Hence, the IO buffer is more immune to power noise induced jitter. Also, it can be observed that below certain noise frequency, the power induced jitter is relatively constant.

The expression (3) and (4) provide the key parameters that needs to be modelled such that the power noise induced jitter can be represented sufficiently in the element IO buffer model.

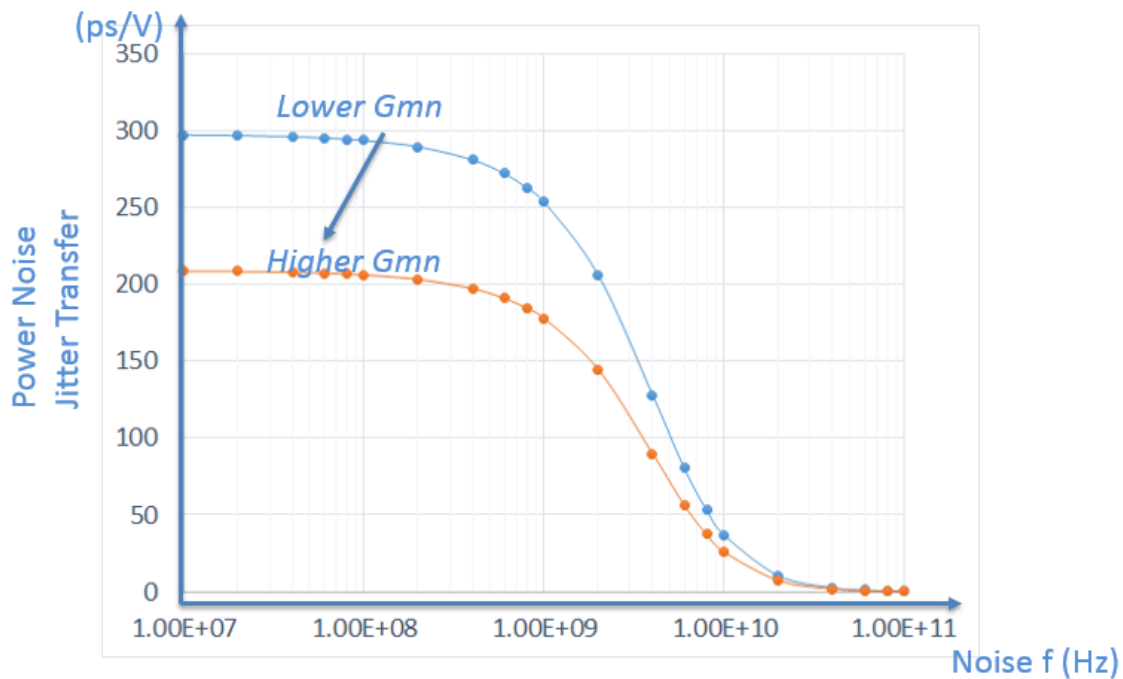


Figure 7 Jitter Transfer Characteristic over Noise Frequency

The element IO buffers are incorporated into a multi-bytes configuration. The combined configuration will mimic the different stages of memory operations. This approach is to quantify the signal & power integrity impact for these memory operation stages. Figure 8 shows the general concept of this approach.

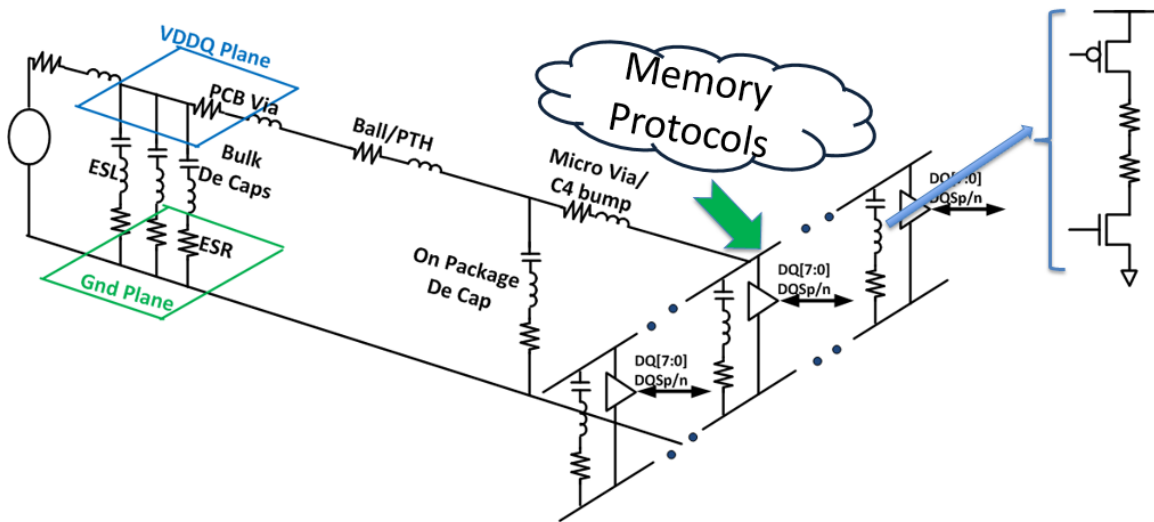


Figure 8 Incorporation of Power Noise Induced Jitter & Channel Simulation with Memory Protocol

4. Operation Specific Signal and Power Integrity Analysis

The operation specific jitter analysis will be examined in this section. The memory initialization and write operation are used to illustrate this approach.

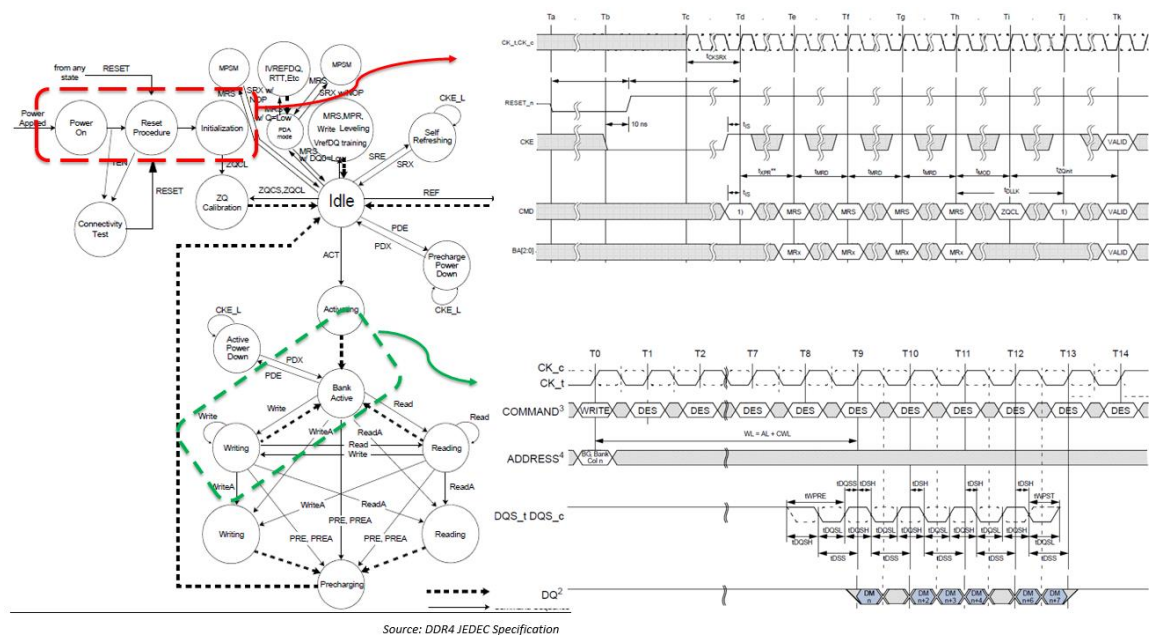


Figure 9 DDR4 Operation State Diagram (Red=Initialization), (Green=Write) [6]

During the initialization stage, the IO buffers for memory system clock is first powered on. While the rest of the IO buffers do not toggle. By the system protocol definition, the system clock enable (CKE) will be asserted after a defined time. Then, the Command/Address IO buffers will be toggled to program the DRAM device.

For the Write operation, an Activation Command is first issued and the corresponding address location will be send to the DRAM. After the defined Write CAS latency, the Write data will be transmitted to the DRAM.

From these two operation stages, it can expect that the power noise signature is very different. The voltage droops are compared between these two operations and it shows that the droop during initialization is lower than the write operations. This is because there are fewer IO toggling during initialization.

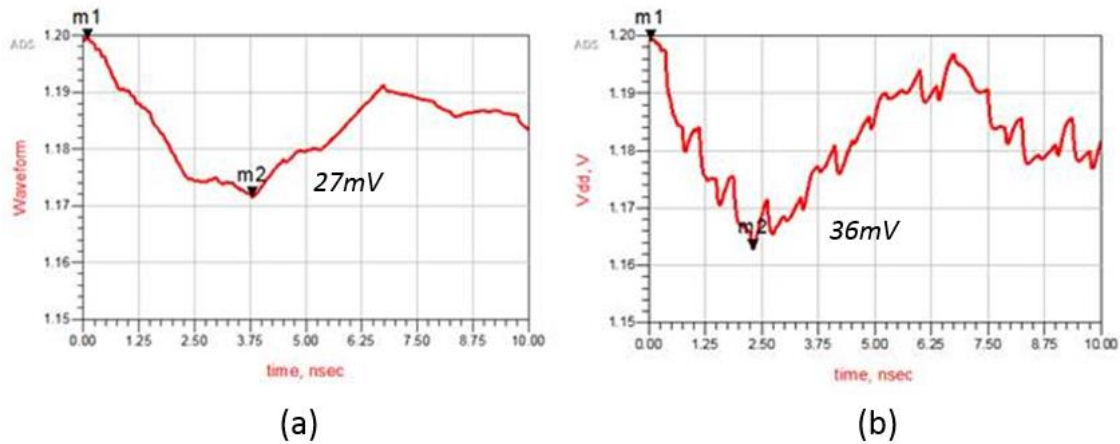


Figure 10 First Droop Comparison between Initialization and Write Operation

The DQ jitter simulation based on the same platform that will be described in section 5 was simulated and the result is shown in . This channel jitter includes the power noise induced jitter and channel inter-symbol interference in write operation. For this particular example, the jitter is about 19.8% UI.

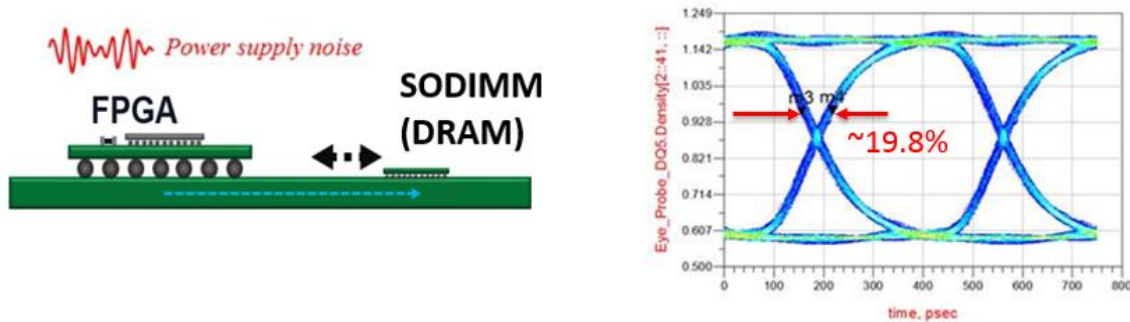


Figure 11 Write DQ Jitter (Channel ISI & Power Noise Jitter)

5. Test Platform Set Up and Measurement Results

The test platform for the correlation is a SODIMM platform shown in Figure 12. The system was running at 3200Mbps and the Write direction Eye Schmoos were collected. The functional Write eye schmoos are shown in Figure 13 (a) and (b) is the functional eye opening comparison between the measurement and simulation prediction.

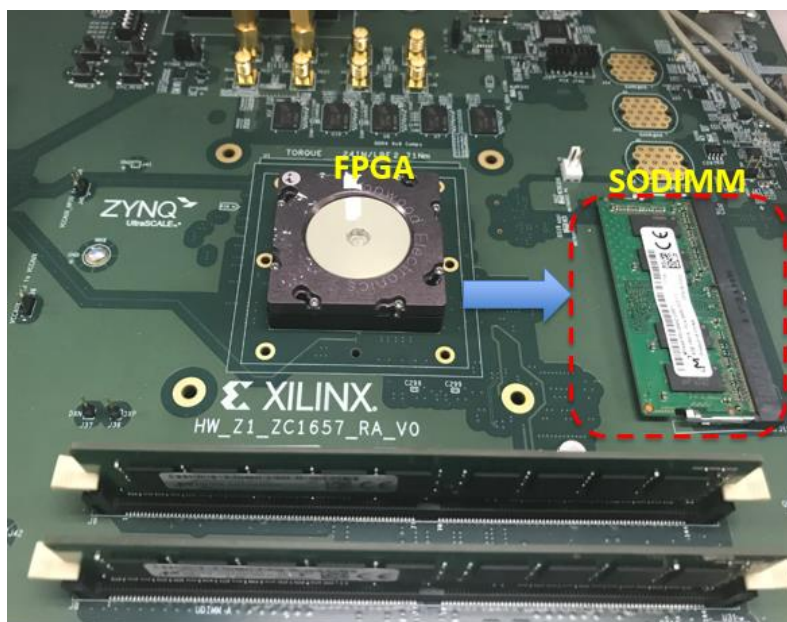


Figure 12 DDR4 SODIMM Test Validation Platform

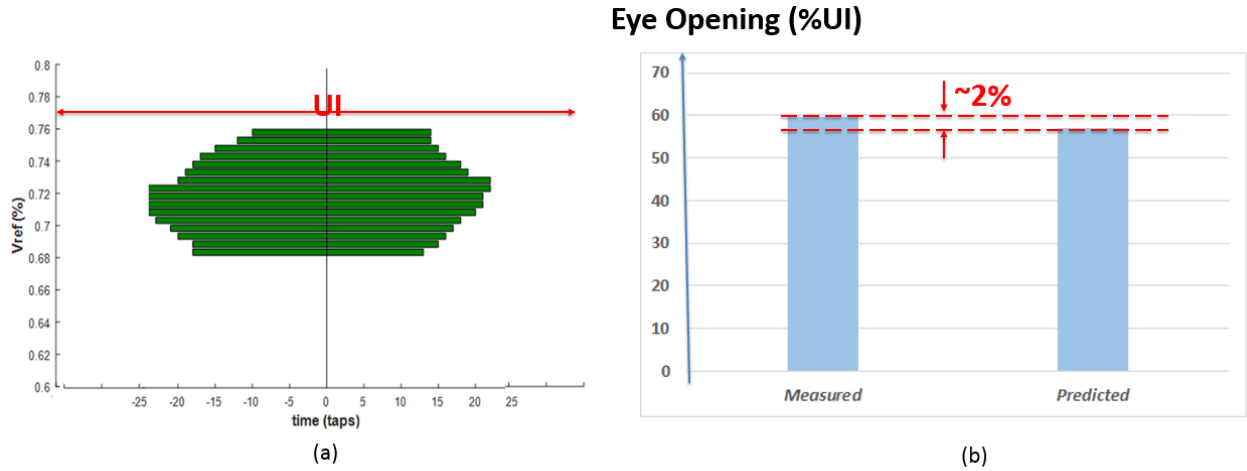


Figure 13 (a) Functional Eye Schmoos (b) Measurement vs Simulation Comparison

With the proposed approach, the correlation between measurement and simulation prediction is within 2% of the UI.

6. Summary and Conclusions

The paper proposed a combined method to include power noise induced jitter to channel jitter simulation. The modeling concept captures the key IO buffer parameters that represent the power noise to jitter transfer characteristic. In addition, the importance of linking the protocol operation stages to signal integrity analysis is discussed. The correlation was done on a selected DDR4 SODIMM configuration and the correlation results matched within 2% of the data UI.

The proposed method provides an easy way for design iteration which allows design re-optimization for power deliver network together with channel signal integrity design tradeoffs. The element modeling approach can be extended to memory IO standard beyond DDR4 for design tradeoff and exploration.

Based on the targeted specifications, a jitter accumulative top level behavior model for HBM system was developed. The predicted jitter trends in signal measured in the lab are in agreement with the top level jitter behavior model. This behavior model also allows system designers to assess the tradeoffs among the sub-system jitter performance.

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