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Asynchronously Pulsed Plasma for High Aspect Ratio Nanoscale Si Trench Etch Process

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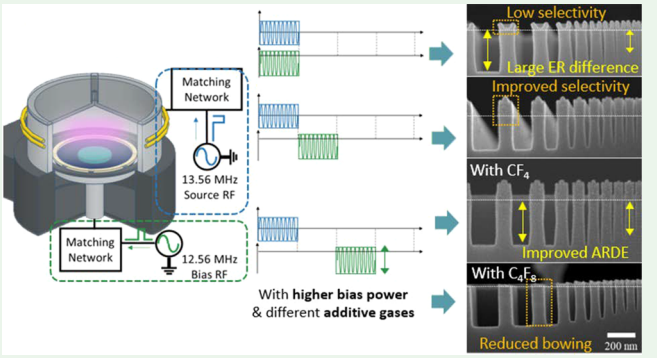
ABSTRACT: The fabrication of high aspect ratio Si trenches has been becoming difficult due to the decrease in critical dimension (CD) to deep nanoscale. Especially, aspect ratio dependent etching (ARDE), which decreases the etch rate as the pattern width gets smaller, makes process uniformity get worse. In this study, the effects of bias pulsing parameters during asynchronous pulsing, which alternatively applies the source power and bias power, as well as the effect of additive gas such as CF_4 and C_4F_8 on the nanoscale Si trench etch characteristics during Cl_2/Ar plasma etching were investigated. It was found that the bias pulsing parameters during the asynchronous pulsing, such as bias pulse duty ratio and bias pulse delay time, can affect the etch characteristics such as etch rate, etch selectivity, and ARDE by changing the ion dose and ion energy during the etching. However, the variation of bias pulse parameters during the asynchronous pulsing did not change the etch profile noticeably, and it showed bowed Si trench etch profiles. To improve the etch profile, the addition of fluorocarbon gas such as CF_4 and C_4F_8 was required, and by using C_4F_8 instead of CF_4, more anisotropic Si etch profile without sidewall bowing could be obtained due to the improved sidewall passivation by a fluorocarbon layer even though it degraded etch selectivity and ARDE. Therefore, it is believed that by controlling the bias pulsing parameters with additive gas, nanoscale Si trench etch characteristics can be more easily controlled.



KEYWORDS: *pulsed plasma, ICP plasma, silicon trench etching, asynchronously pulsed plasma, aspect ratio dependent etching (ARDE)*

1. INTRODUCTION

The feature size of electronic devices is continuously decreasing, and advanced patterning technology such as SADP (self-aligned double patterning), SAQP (self-aligned quadruple patterning), etc. is being adopted even for EUV (extreme ultraviolet) lithography technology to realize devices having a CD (critical dimension) of less than 10 nm.[1−4] In addition to the complexities involved in the extremely small-scale patterning process, the geometrical change of device structure from 2D to 3D makes the patterning process extremely difficult.[5−8] For this reason, there are many issues that occur during the plasma etching process, and one of the important issues that arises with increasing aspect ratio of the device feature is the ARDE (aspect ratio dependent etching) effect, which shows different etch depth depending on the pattern width, due to the ion/neutral shadowing, charging of the mask, Knudsen transport of neutrals, etc.[9−14]

Many studies have been conducted to investigate the source of the ARDE effect and to suppress it. For example, Imai et al.[15] reported the effect of bias power on ARDE and the positive charge-up model for contact hole etching. As the bias power increased, the overall etch rate (ER) was increased, but the etch depth differences among the different contact hole diameters were increased by charging up the contact holes. Doh et al.[16] reported the effect of the bias frequency on ARDE for SiO_2 contact hole etching by using ECR (electron cyclotron resonance) plasma. In this study, as the frequency of bias RF power was increased while maintaining the same bias voltage, the ARDE was effectively suppressed by increasing high energy ions incident on the substrate. Lai et al.[17] reported a physical model of the TDM (time division multiplex) plasma etching for high aspect ratio Si MEMS (microelectromechanical system) device that could effectively control ARDE. The TDM process consisted of a deposition step for passivation of polymeric species to the feature surface and a spontaneous etching step by F radical-based etching. In the above model, the etching step was divided into the polymer removal stage at the initial etching step and the isotropic etching stage similar to the BOSCH process.[18] By adjusting the

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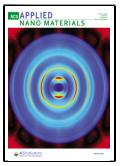

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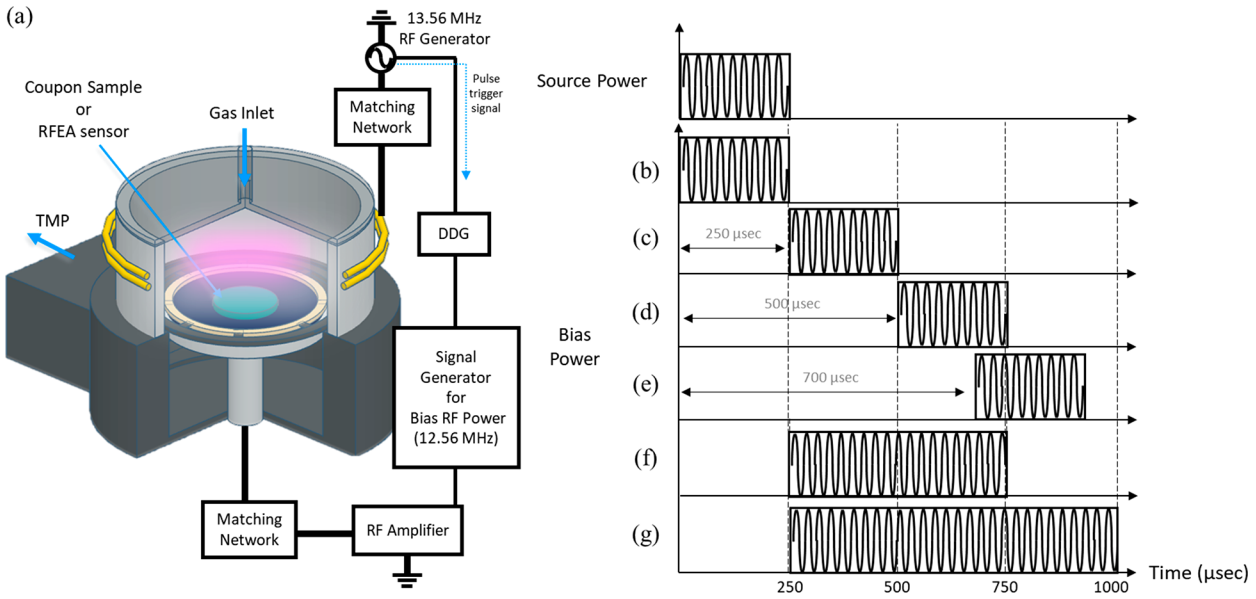

Figure 1. (a) Schematic diagram of the ICP etching system and (b–g) pulse conditions for the experiment.

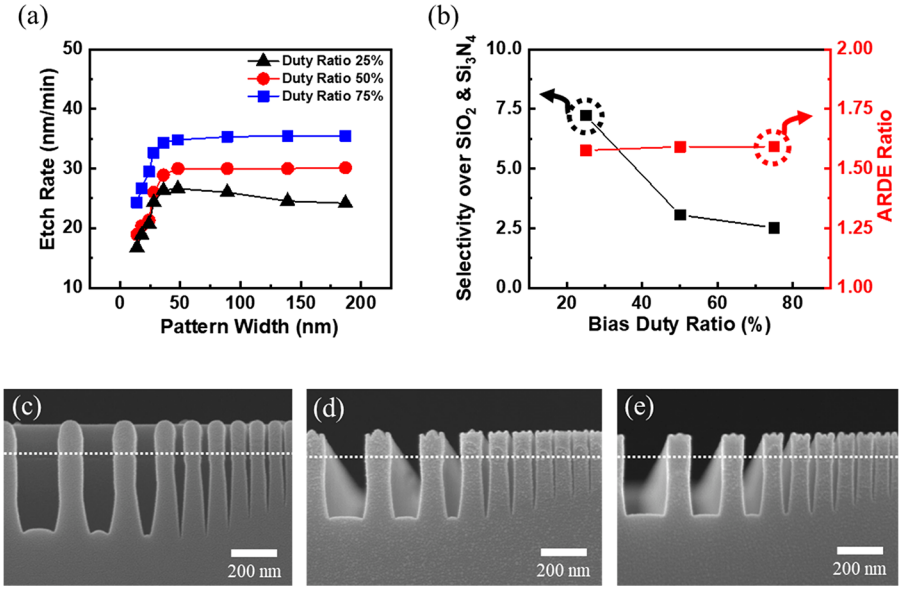

Figure 2. (a) Si etch rates as a function of pattern width for different bias duty ratios from 25 to 75% during the asynchronous pulsing. (b) Etch selectivity and ARDE ratio as a function of bias duty ratio. Cross-sectional SEM images of Si trenches etched with the bias duty ratios of (c) 25%, (d) 50%, and (e) 75% during the asynchronous pulsing. Source pulse duty was 25%, and bias duty delay time was 250 μs.

process step time, ARDE was controlled by finding the balance of passivation thickness and etched depth.

Through the above studies, to improve ARDE, it can be seen that controls of charging, ion energy distribution, and appropriate passivation/etching time are essential for nanoscale feature etching. Our previous study[19] also showed that asynchronous pulsing that alternatively applies source and bias powers within one pulse cycle can effectively suppress the ARDE effect and enable a highly selective etch process. The above advantages are from the cyclic etching behavior which involves repeated chemisorption and desorption, but to understand the asynchronous pulsing more clearly, variables of asynchronous pulsing (such as bias pulsing parameters during asynchronous pulsing) require further investigation. Also, it is found that the sidewall of nanoscale Si trench exposed during the asynchronously pulsed plasma needs to be protected during the etching. Therefore, in this study, in addition to the effects of various bias pulse parameters as some of the asynchronous pulsing variables, the effects of additive gases such as CF_4 and C_4F_8 on the etch profile control during the nanoscale Si trench etching have been investigated.

2. EXPERIMENTAL DETAILS

A 200 mm diameter inductively coupled plasma (ICP) etching system, shown schematically in Figure 1a, was used for etching of the silicon trench. A 13.56 MHz pulsed RF generator (SEREN, R10001) was connected to the ICP source antenna through a matching network. The pulse signal extracted from the source generator was fed to an RF amplifier (ENI, A1000) through a digital delay generator (DDG; SRS, DG645) and a signal generator (HP, 8657B) to generate a 12.56 MHz asynchronously pulsed bias power to the substrate. The pulse repetition frequency was maintained at 1 kHz, and the duty

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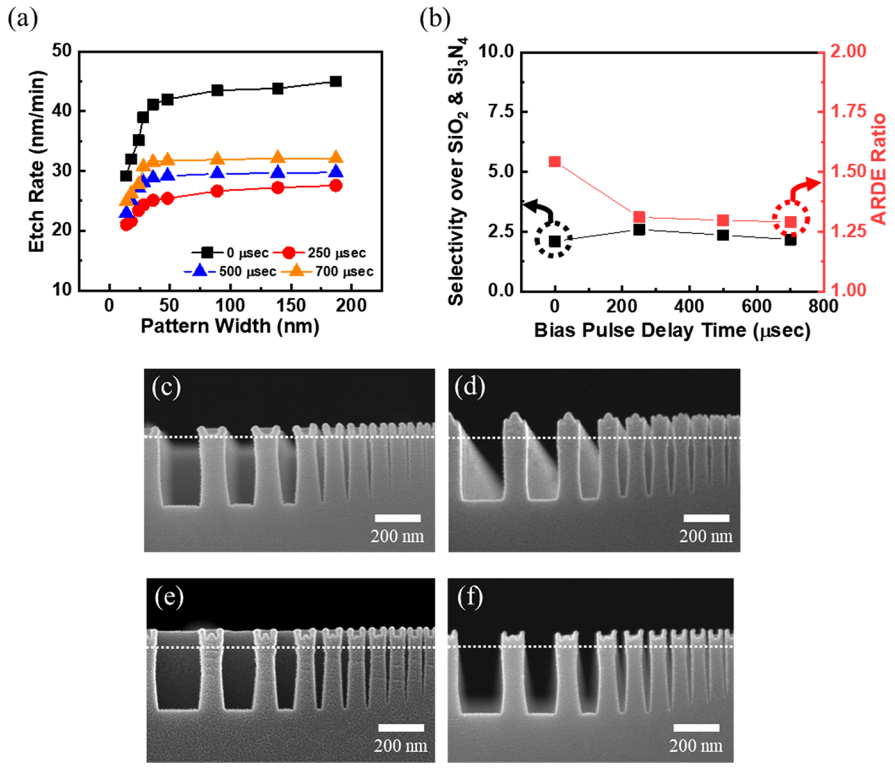

Figure 3. (a) Si etch rates as a function of pattern width for different bias duty delay times from 0 to 700 μs during the asynchronous pulsing. (b) Etch selectivity and ARDE ratio as a function of bias pulse delay time. Cross-sectional SEM images of Si trenches etched with the bias pulse delay times of (c) 0 μs, (d) 250 μs, (e) 500 μs, and (f) 700 μs. Both source pulse duty and bias pulse duty were 25%.

ratio of the ICP source was maintained at 25% (250 μs). The bias duty ratio and delay time were varied from 25 to 75% and from 0 to 700 μs, respectively (Figure 1b–g).

Silicon coupon samples having various opening widths from 185 to 14 nm were used to investigate the effects of different pulse parameters on the ARDE of the Si trench. A bilayer hardmask consisting of an SiO_2 (90 nm)/Si_3N_4 (90 nm) layer with a line and space pattern was used. For the etching of Si, gas mixtures of Cl_2, Ar, and additive gases (CF_4 or C_4F_8) were used, and the process pressure was maintained at 5 mTorr. The etch gases used in the experiment all had purities higher than 99.999%. The instant ICP source power was maintained at 400 W, and the instant bias power was applied from 75 to 150 W. The substrate temperature was kept at 20 °C during all experiments.

The instant RF voltage on the substrate for different asynchronously pulsed conditions was measured using a high voltage probe (P6015A, Tektronix) which was directly connected to a feed-through. During this measurement, ICP source power and bias power were maintained at 400 and 75 W, respectively. The time-average ion energy distribution (IED) on the substrate was measured using an RFEA (retarding field energy analyzer; Impedance, Semion) with four grids (G0 (substrate potential): entrance grid, G1 ion/electron repelling grid, G2 analyzer grid, G3 suppressing grid (set at −70 V), and C collector (set at −60 V)). The RFEA was located at the center of the substrate holder during the measurement.

The etching depths and profiles were measured using a field emission scanning electron microscope (FE-SEM; Hitach, S4700). To measure the degree of ARDE, the ARDE ratio was calculated by dividing the highest ER by the lowest ER for the patterns having opening widths from 185 to 14 nm. The etch selectivities between silicon and bilayered mask were calculated by dividing the etch depth of Si at 185 nm trench by the etch depth of bilayered mask. Also, to investigate species on the etched Si surface, XPS (X-ray photoelectron spectroscopy) measurements were conducted using blank Si and trench Si samples etched ∼400 nm in depth. Those samples were exposed at the same time with $Cl_2/CF_4/Ar$ (10/10/30 sccm) and $Cl_2/C_4F_8/Ar$ (10/10/30 sccm) conditions. In the case of trenched Si, samples were tilted ∼10° to measure species on the trench sidewall. In fact, the XPS information from the tilted samples contains information from both the top surfaces and the sidewalls. Highly dense patterned silicon samples were used to have more information from the sidewall of the trenches rather than top flat surface of the trenches.

3. RESULTS AND DISCUSSION

3.1. Effect of Bias Pulse Duty Ratio. To investigate the etching characteristics and the ARDE effect on the bias pulse duty ratio with asynchronously pulsed plasma, the bias duty ratio was changed from 25 to 75% while the instant ICP source power and bias power were maintained at 400 and 75 W, respectively. Cl_2 (5 sccm)/CF_4 (5 sccm)/Ar (40 sccm) gases were used. Figure 2a shows the ERs of the Si trench as a function of pattern width for different bias duty ratios of 25 (black dot), 50 (red dot), and 75% (blue dot) during the asynchronous pulsing (source pulse duty 25% and bias duty delay time of 250 μs). As shown in Figure 2a, ER was at its lowest at the smallest pattern width, and the increase in the pattern width generally increased the ER due to ARDE effect. Also, the ER was lowest at the condition of the bias duty ratio of 25% among all bias duty ratios by showing values from 26.1 nm/min at a 185 nm width pattern to 16.72 nm/min at a 14 nm width pattern due to the lowest etching time at the lowest bias duty ratio. In the case of a duty ratio higher than 50%, ERs of Si trenches were saturated from the pattern width of ≥48 nm.

Figure 2b shows the etch selectivity of Si over the bilayered mask (SiO_2/Si_3N_4) for the pattern width of 185 nm and the ARDE ratio between ER at 185 nm width/ER at 14 nm width as a function of the bias duty ratio (the ARDE effect can be

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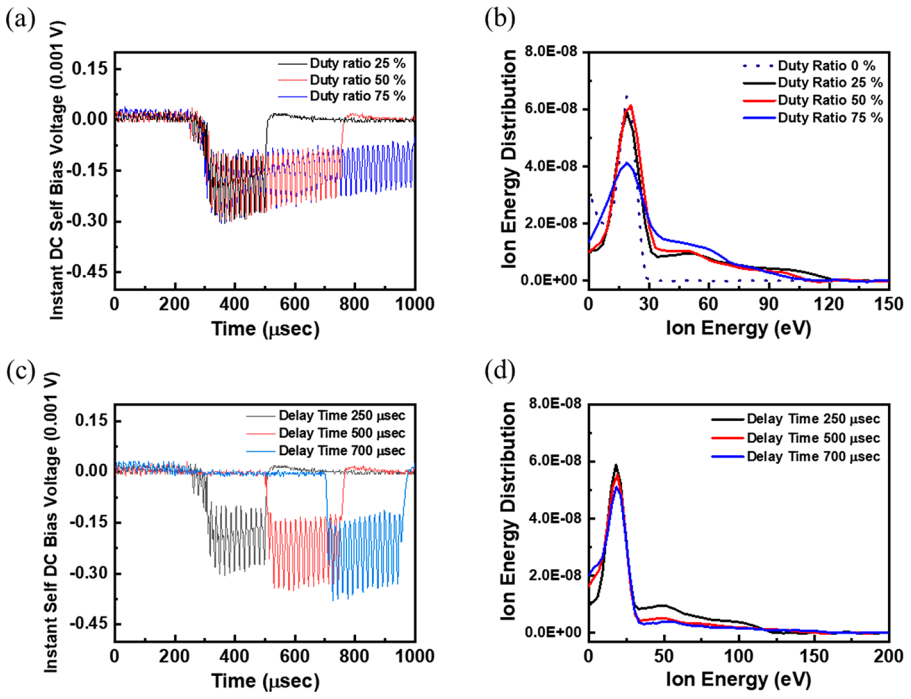

Figure 4. (a) Instant DC-self-bias voltage data as a function of time for various duty ratios of bias pulsing from 25 to 75%. (b) Time-averaged IED for various bias pulse duty ratios. (c) Instant DC self-bias voltage data as a function of time for bias pulse delay time from 250 to 700 μs in Figure 2. (d) Time-averaged IED observed for different bias pulse delay times.

more precisely described by showing etch depth vs time for different pattern widths, but for easier comparison, we used the ratio ER at 185 nm width/ER at 14 nm width after etching as the ARDE ratio). The selectivity was the highest (7.23) at the duty ratio 25% condition, and it was significantly decreased to 2.52 as the bias pulse duty ratio increased. This can be attributed to the increased sputtering with increasing bias pulse duty ratios by energetic ions. That is, as the bias duty ratio is increased during the asynchronous pulsing, the ion bombardment time is increased, which results in nonselective etching. However, the variation in bias duty ratio did not noticeably change the ARDE ratio, as it showed a similar ratio of 1.58−1.59 which was possibly due to the sufficient energetic ion flux at the bias duty ratio of 25% for the etching of all pattern widths.

Figure 2c−e shows the cross-sectional SEM images of silicon trenches with various pattern widths etched by different bias duty ratio conditions of 25, 50, and 75%, respectively. In the case of a duty ratio of 25%, tapered/bowed sidewall and trenching were observed, possibly due to a lack of sufficient ion bombardment of ions for the removal of polymer on the bottom of the trench during the bias power on time. However, for the duty ratio of 75%, the bottoms of the trenches were flat, possibly due to sufficient removal of the trench bottom polymer layer, even though the sidewalls were still bowed.

3.2. Effect of Bias Pulse Delay. The etch characteristics of Si trenches depending on the bias pulse delay time were investigated. The source power, duty ratio of source pulse, and gases were the same as shown in Figure 1, the instant bias power was set at 100 W, and the bias pulse duty ratio was kept at 25%. As the bias triggering time of the delay generator was varied, the bias pulse delay time was varied from 0 μs (synchronously pulsed plasma mode) to 700 μs. Figure 3a shows the Si trench etch rate as a function of pattern width for different bias duty delay times ranging from 0 to 700 μs during the asynchronous pulsing. ARDE was observed for all of the etch conditions; however, the bias delay time of 0 μs (synchronous pulsing condition) showed the highest ER compared to the bias delay time of ≥250 μs (asynchronous pulsing conditions), which was attributed to the synergy effect between the source power and the bias power. In the case of asynchronous pulsing (bias delay time ≥250 μs), the longer bias delay time showed a slightly higher ER compared to the shorter bias delay time.

Figure 3b shows the selectivity over the (SiO_2/Si_3N_4) mask for the pattern width of 185 nm and the ARDE ratio ER at 185 nm width/ER at 14 nm width as a function of the bias pulse duty time. The etch selectivity was the lowest (2.1) at the delay time of 0 μs (synchronous pulsing), whereas it was the highest (2.6) at the delay time of 250 μs. For asynchronous pulsing conditions, increasing the bias pulse delay time from 250 to 700 μs decreased the selectivity slightly from 2.6 to 2.2. The ARDE ratio was the highest (1.55) at the delay time of 0 μs (synchronous pulsing) while showing an improved ARDE ratio (∼1.3) for the delay time of ≥250 μs (asynchronous pulsing). Further, at the delay time of 500 and 700 μs, the saturation of ER was observed in patterns with a width of ≥48 nm. Therefore, there were differences in ARDE between synchronous pulsing and asynchronous pusling, but there were no significant differences for asynchronous pulsing with different pulse duty times.

Figure 3c−f shows the cross-sectional SEM of Si trenches with various pattern widths etched by bias pulse delay time 0, 250, 500, and 700 μs, respectively. In the case of synchronous pulsing (a delay time of 0 μs), severe mask loss was observed. On the contrary, under asynchronously pulsing conditions (delay time of ≥250 μs), SiO_2/Si_3N_4 mask layer was relatively preserved, which means that higher selectivity could be possible, but bowing was observed for almost all patterns. It is well-known that negative ions are formed for gases with high

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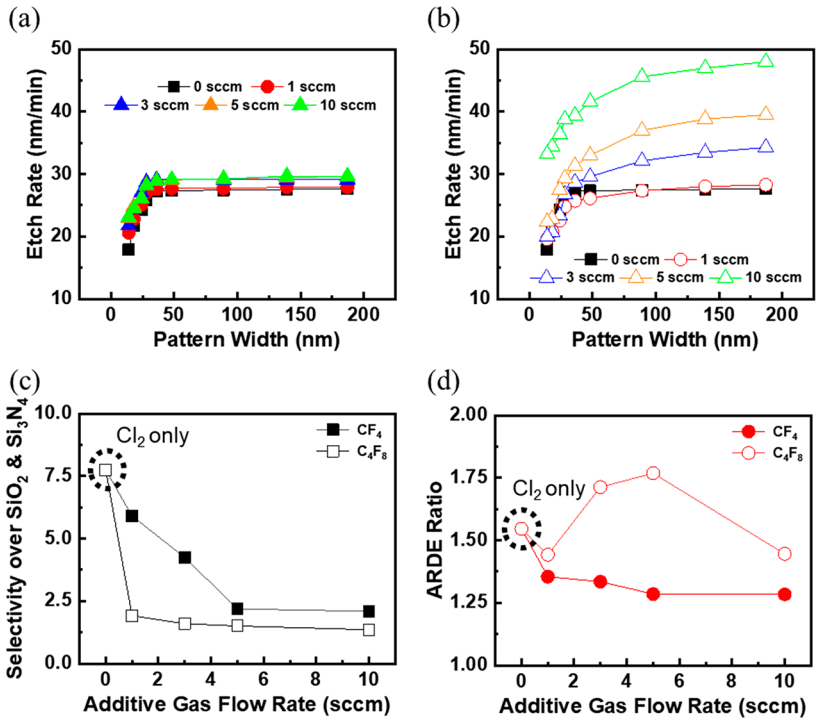

Figure 5. ERs of Si trenches as a function of pattern width for different additive gas flow rates of (a) CF_4 and (b) C_4F_8. (c) Si etch selectivity over the SiO_2/Si_3N_4 mask as a function of the flow rate of CF_4 (black filled square) or C_4F_8 (black empty square). (d) ARDE ratios observed as a function of CF_4 (red filled triangle) or C_4F_8 (red empty triangle) flow rate.

electronegativity during the source power off period and that these negative ions tend to remove the charging that is formed on the patterned samples.[20−22] However, as shown in Figure 3c−f, even though there were differences in pulse delay between the source power and bias power, there were no significant changes in etch profiles, particularly for asynchronously pulsing conditions, which was possibly due to the fact that there were no charge-related issues in our experiment for silicon etching.

3.3. Effect of Pulsing Parameters on Incident Ion Energy. In the above experiments, it was confirmed that the ER, selectivity, and degree of ARDE were varied by changing the bias pulse parameters during synchronous/asynchronous pulsing despite the same chemistry. To understand the effect of bias pulsing parameters on etch characteristics, instant bias voltages and ion energy distributions on the substrate were measured under various pulsing conditions. During the measurements, instant ICP source power and bias power were maintained at 400 and 75 W, respectively. And only Ar gas was used to prevent the contamination and corrosion of the RFEA sensor.

Figure 4a shows the instant DC-self-bias voltage data as a function of time for various duty ratios of bias pulsing from 25 to 75%. During the source power on period (0−249 μs), the DC bias voltage was nearly zero because there was only source RF power. But after bias power was applied to the substrate, negative DC self-bias voltages were developed. In addition, slightly lower DC-self-bias voltage was observed as the duty ratio was increased by showing −153 V for a duty ratio of 25%, −150 V for a duty ratio of 50%, and −144 V for a duty ratio of 75%. These results could be related to the power on−off transition and plasma stabilization. Figure 4b shows the time-averaged IED for various bias pulse duty ratios. The IED for the source pulsing only (duty ratio 0%) is also shown as a dotted line. The solid lines show the IEDs at the duty ratios of 25% (black), 50% (red), and 75% (blue). The time-averaged IED results in Figure 4b show the addition of two types of IEDs; a monoenergetic distribution centered at 18 eV resulting from ICP source power, and a broad distribution with higher energies resulting from the bias power. As the bias pulse duty ratio was increased, the distribution with the energy of greater than 100 eV was decreased whereas the IED in the range of 30−65 eV was increased, thus reflecting the decreased instant DC-self-bias voltage shown in Figure 4a. The higher ERs with lower etch selectivity observed in Figure 2a and Figure 2b, respectively, for the conditions with higher bias duty ratios are believed to be related to the higher ion dose in one source/bias pulse time period and increased physical sputtering after etching chemisorbed species on Si surface formed during the source pulsing (see Supporting Information Figure S-3a for the behavior of ion flux to the substrate as a function of bias duty ratio). In addition, the Si trenched with a flat trench bottom observed for the higher duty ratios in Figure 3e also appears to be related to the lower IED at the higher ion flux to the bottom of trench as a result of the increased duty ratios.

Figure 4c shows the instant DC self-bias voltage data as a function of time for the bias pulse delay times ranging from 250 to 700 μs in Figure 3. As shown in Figure 4c, as the bias pulse delay time was increased, the average DC self-bias voltage became larger (−153 V at 250 μs, −216 V at 500 μs, and −224 V at 700 μs). These results are believed to be related to the impedance changes of the plasma system after the ICP source pulse operation.[23,24] When the source power is off, the plasma density is gradually decreased due to the afterglow, so the system impedance is increased with time.[25] Therefore, the increased bias pulse delay time increases instantaneous DC self-bias voltage due to the increased plasma impedance for the asynchronously pulsed plasma. The time-averaged IED

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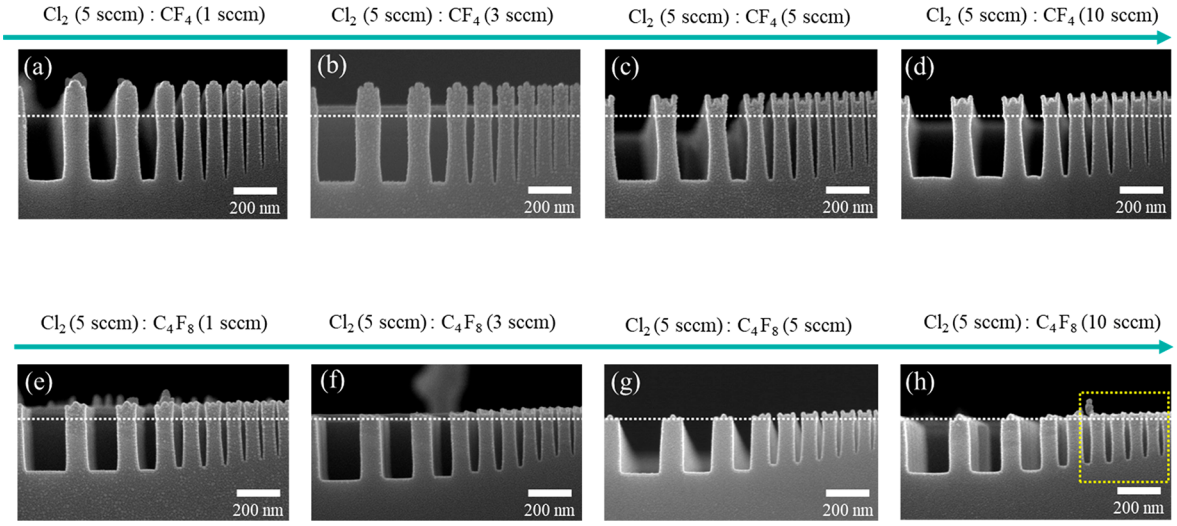

Figure 6. Cross-sectional SEM images of Si trenches having various pattern widths etched with different CF_4 (a–d) and C_4F_8 flow rates (e–h) for the process conditions shown in Figure 5.

observed for different bias pulse delay time in Figure 4d also showed both monoenergetic low energy IED from ICP source power and high energy IED from bias power having higher ion energy for a longer bias pulse delay time. From these results, it is believed that the higher etch rate, decreased etch selectivity, and improved ARDE at the longer bias pulse delay time shown in Figure 3 are all related to the higher ion energy to the substrate.

3.4. Effect of Additive Gas Flow on Etching Characteristics. The effect of additive gas (except for Ar) on Si trench etching characteristics during the asynchronous pulsed plasma etching was investigated by measuring ER, selectivity, ARDE ratio, and etch profile while changing the flow rates of additive gases such as CF_4 and C_4F_8. When only Cl_2/Ar gas mixtures were used for Si trench etching using asychronously pulsed plasmas, sidewall bowing of Si trenches caused by scattering of the ions was observed (as shown in Supporting Information Figure S-4). Therefore, fluorocarbon gases were added to protect the sidewall of the Si trench (O_2 gas was also considered as an additive gas for passivation, but severe trenching and ARDE were observed as shown in Supporting Information Figure S-5). The instant source power and duty ratio were kept at 400 W and 25%, respectively, while the instant bias power and its duty ratio were maintained at 150 W and 25%, respectively. The delay time of the bias pulse was kept at 250 μs, while the total flow rate of gases was maintained at 50 sccm. The flow rate of Cl_2 gas flow was kept at 5 sccm, and CF_4 or C_4F_8 was varied from 1 to 10 sccm. Ar gas was varied from 35 to 44 sccm to maintain an operating pressure of 5 mTorr.

Figure 5a and Figure 5b show the ERs of Si trenches as a function of pattern width for different additive gas flow rates of CF_4 and C_4F_8, respectively. As shown in Figure 5a, for CF_4 gas, the increase in the flow rate slightly increased the Si ER trench from 27.7 to 29.7 nm/min for the widest 185 nm pattern width and from 17.9 to 23.1 nm/min for the smallest 14 nm pattern width. In the case of C_4F_8 addition condition, as shown in Figure 5b, similar etch trends with CF_4 addition condition were observed but with higher ERs, that is, 48 nm/min for the widest pattern width and 33.2 nm/min for the smallest pattern width with 10 sccm of C_4F_8. The increase in Si ER with the additive gas of CF_4 or C_4F_8 is believed to be related to the dissociation of F species and the formation of volatile SiF_x byproducts with Si[26] (see Supporting Information Figure S-7a,b for blank Si, SiO_2, and Si_3N_4 samples). Even though more investigation is needed, the higher Si ER with the addition of C_4F_8 compared to the addition of CF_4 at the same additive gas flow rate appears to be related to the removal of oxygen or nitrogen from the SiO_2/Si_3N_4 mask layer depositing on the etched silicon surface.

Figure 5c shows the Si etch selectivity over the SiO_2/Si_3N_4 mask material as a function of the flow rate of CF_4 (black filled square) or C_4F_8 (black empty square). The etch selectivity was decreased for all additive gas conditions, and the selectivity was lower for C_4F_8 addition (from 1.9 to 1.4) than it was for CF_4 addition (from 5.9 to 2.1). Also, as the flow rate of additive gas was increased, the selectivity with the mask was decreased. Further, a sharp decrease in etch selectivity was observed for the C_4F_8 addition, which was possibly due to the formation of more polymeric species in the plasma than the CF_4 gas condition and which makes it easier to form volatile etch byproducts by reacting with the mask material composed of SiO_2 and Si_3N_4.[27] (See Supporting Information Figure S-8 for optical emission spectra of Ar + Cl_2, Ar + Cl_2 + CF_4, and Ar + Cl_2 + C_4F_8 conditions. By adding fluorocarbon additive gases, fluorocarbon species (250–350 nm)[28] were formed in the plasma, and more polymeric species were observed for the C_4F_8 addition condition.[29])

Figure 5d shows the ARDE ratios observed as a function of the CF_4 (red filled circle) or C_4F_8 (red empty circle) flow rate. In the case of CF_4 addition, the increase in CF_4 flow rate led to a significant improvement in the ARDE effect from 1.55 (Cl_2 only) to 1.35 (1 sccm) to 1.28 (10 sccm), which was possibly due to the inverse RIE-lag effect (polymerizing species such as CF_x (x = 1, 2) tend to stick on the sidewall during the Si trench etching for the narrow pattern width, and etching species such as Cl and F tend to move into the trench bottom and etch the Si. On the contrary, for the wide pattern width, in addition to etching species, the polymerizing CF_x species also tend to move to the bottom of the Si trench surface due to the smaller sidewall area and polymerize the bottom surface; therefore, the ER of Si tends to decrease for a wider pattern width in a different from normal ARDE). For the C_4F_8 addition conditions, ARDE ratio was initially increased with

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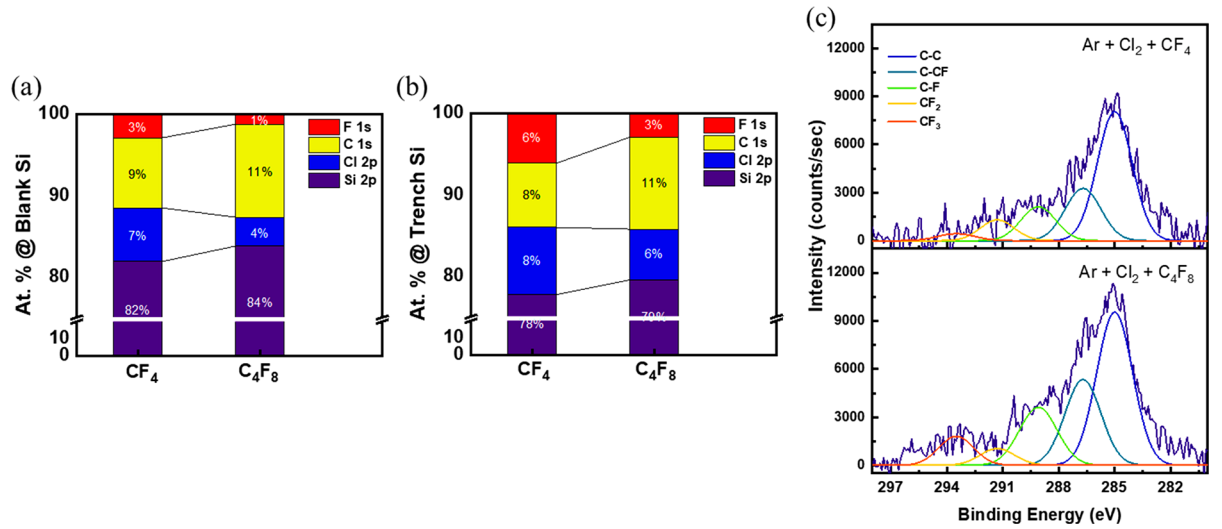

Figure 7. Atomic percentages of the species measured by XPS on the surface of (a) blank Si and (b) trench Si after etching without oxygen and (c) C 1s narrow scan data of Si trench sidewall etched with $Cl_2/CF_4/Ar$ and $Cl_2/C_4F_8/Ar$.

increasing C_4F_8 gas flow rate from 1.55 (Cl_2 only) to 1.71 (5 sccm CF_4), possibly due to the reaction of CF_x with oxygen/nitrogen on the Si trench bottom surface for a wide pattern width at low C_4F_8 flow rates, but for the C_4F_8 gas flow rate higher than 5 sccm, the ARDE ratio was decreased to 1.45 (10 sccm C_4F_8) due to the higher CF_x polymerizing species for the inverse RIE-lag effect. That is, in the case of a wide trench, polymerizing CF_x species can reach the bottom of the trench in addition to the sidewall of the trench; however, in the case of a narrow trench, polymerizing CF_x species are more likely to be attached on the sidewall of the trench during the transport to the bottom of the trench due to the collision on the sidewall with the high stickness of CF_x species, and less polymerizing species reach the bottom of the trench. Thefore, due to the lower polymerizing species on the bottom of the narrow width pattern, etching can be higher for the narrow pattern trench compared to the wide pattern trench, leading to an inverse-RIE effect.

Figure 6a–d and Figure 6e–h show cross-sectional SEM images of Si trenches having various pattern widths etched with different CF_4 (Figure 6a–d) and C_4F_8 flow rates (Figure 6e–h) for the process conditions presented in Figure 5. In the case of CF_4 addition, due to the higher etch selectivity over the mask layer, the masks were preserved relatively well compared to C_4F_8 addition (the decrease in etch selectivity at the high flow rates of CF_4 and C_4F_8 might also have affected the measured decrease in the ARDE ratio in Figure 5d). However, for CF_4 addition, the etched Si trench showed sidewalls that were bowed due to the insufficient sidewall passivation even with 10 sccm of CF_4, while for C_4F_8 addition, even though the etch selectivity was lower, highly anisotropic Si trench etch profiles were observed due to the formation of a thicker sidewall passivation layer compared to CF_4 addition (an anisotropic Si etch profile could be observed even with 0.5 sccm C_4F_8 addition, as shown in Supporting Information Figure S-8).

3.5. Surface Analysis of Si Trench by XPS. Blank Si and Si trench exposed to the same etch conditions in Figure 5, except for gas flow rate ($Cl_2/CF_4/Ar$ = 10/10/30 sccm and $Cl_2/C_4F_8/Ar$ = 10/10/30 sccm), were observed using XPS, and the species on the etched silicon surfaces were measured. For the Si trench samples, to obtain the species information on the sidewall of the trench, Si samples etched to a depth of 400 nm were tilted ~10°. Figure 7a and Figure 7b show the atomic percentages of the species on the surface of the blank Si and trench Si after the etching, respectively. Due to possible oxidation during the air exposure before the XPS measurement, the atom % of O 1s was excluded in the atomic percentages of the species. As shown in Figure 7a and Figure 7b, the condition of C_4F_8 showed higher carbon percent while showing lower fluorine and chlorine percentages compared to CF_4 addition for both blank Si surface and trench Si surface. The above results partially reflect the ion bombardment of the trench bottom while passivation occurs at the sidewall for the C_4F_8 addition condition by showing more polymeric species, even though it is not the exact same etching condition as used in Figures 2, 3, and 6. Figure 7c shows the high resolution XPS C 1s spectra that were measured for Si trench samples etched with CF_4 and C_4F_8 addition. The peaks observed in both conditions were assigned to the C–C (285 eV), C–O (286.7 eV), and C–F_x (x = 1, 2, and 3 at 289.7, 291.8, and 293.9 eV, respectively).[30,31] More CF_x bonding (55% of CF_x bonding for C_4F_8 compared to 47% of CF_x bonding for CF_4 condition) was observed for the Si trench etched with C_4F_8 addition compared to that etched with CF_4 addition. Therefore, the improvement of Si trench etch profiles with C_4F_8 addition compared to that with CF_4 addition was related to the thicker CF_x polymer formed on the sidewall of the etched Si trench surface.

4. CONCLUSION

In this study, the effects of bias pulsing parameters during asynchronous pulsing and fluorocarbon (CF_4 or C_4F_8) additive gas on Si trench etch characteristics were investigated. It was found that the bias pulse duty ratio for asynchronous pulsing affected the etch rates and etch selectivity over SiO_2/Si_3N_4 mask without changing the ARDE ratio due to the increased sputtering by the increased ion dose at the higher bias duty ratio. In the case of the bias pulsing delay time, the longer bias pulse delay time decreased the etch selectivity but slightly improved the etch rates and ARDE due to the increase of ion energy by increasing the plasma impedance of the system. The change in bias pulse duty ratios or bias pulse delay time did not

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ACS Appl. Nano Mater. 2023, 6, 10097–10105

improve the etch profiles and showed sidewall bowing, and an additive gas passivating the Si trench sidewall was required. By using fluorocarbon gas, especially by using C_4F_8 instead of CF_4 as an additive gas, a more anisotropic Si trench etch profile could be obtained due to the improved sidewall passivation by a fluorocarbon layer, even though it degraded etch selectivity and ARDE. Therefore, during the asynchronous pulsing, by controlling the bias pulsing parameters with additive gas, nanoscale Si trench etch characteristics which were difficult to control with conventional continuous wave plasmas could be controlled more easily. And this technique could be applicable to advanced etching techniques for high aspect ratio features having a wide variety of CDs such as nano-TSV (through silcon via), iso-STI (shallow trench isolation), etc. having various sizes of nanoscale silicon features.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsanm.3c00807.

Etch rates of blank Si, SiO_2, and Si_3N_4 for different pulse conditions and the selectivities over SiO_2 and Si_3N_4 (Figure S-1 and Figure S-2); ion flux to the substrate as a function of pulse condition (Figure S-3); cross-sectional SEM images of Si trenches etched by Cl_2 and Ar (Figure S-4); cross-sectional SEM images of Si trenches etched by Cl_2, O_2, and Ar (Figure S-5); repeatability test results of asynchronous pulsed plasma for the same etch conditions shown in Figure 6b (Figure S-6); etch rates of blank Si, SiO_2, and Si_3N_4 for different gas conditions and the selectivities over SiO_2 and the Si_3N_4 (Figure S-7); optical emission spectra of Ar/Cl_2, Ar + Cl_2 + CF_4, and Ar + Cl_2 + C_4F_8 conditions (Figure S-8); cross-sectional SEM images (Figure S-9a,b), ER (Figure S-9c), and ARDE ratios of Si trenches etched by different C_4F_8 flow rates (PDF)

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Notes

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