#### Etch Damage Reduction of Ultra Low-k Dielectric by Using Pulsed Plasmas

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To reduce interconnect resistance and capacitance (RC) time delay of semiconductor integrated circuit, the dielectric material with more porosity is used in recent interconnection for lower dielectric constant. However, it is difficult to use highly porous low-k dielectric materials at the narrow pitch because it is easily damaged during the plasma etching processes. In this study, as one of the plasma induced damage reduction methods in the etching of porous low-k dielectric using C<sub>4</sub>F<sub>8</sub>-based gases, RF pulsed plasma methods have been investigated by using a dual frequency capacitively coupled plasma etch system. RF pulsed plasmas generated higher carbon-rich radicals in the plasma and less charging effect on the dielectric material surface compared to continuous wave plasmas and, therefore, showed a reduced damaged layer compared to the conventional continuous wave plasma etching. Porous SiCOH dielectric with a patterned TiN hard mask was etched using the RF pulsed plasmas and the results showed more anisotropic etching profiles with less sidewall damages. Therefore, it is believed that the RF pulsed plasma etching process of ultra low-k dielectric materials can improve the RC delay related with plasma damage for the next interconnect technology.

### Introduction

In the development of advanced semiconductor integrated circuits, resistance and capacitance (RC) time delays in copper interconnection became more critical than complementary metal oxide semiconductor (CMOS) gate delay because the smaller pitch of metal-to-metal makes the resistance and capacitance much higher. <sup>[1]</sup> In order to reduce interconnect RC time delay, highly porous dielectric material, that is, porous SiCOH, is used in recent interconnection to decrease the dielectric constant further. <sup>[2]</sup> However, the porous SiCOH is very easily damaged during plasma etching processes by plasma induced damages (PIDs). That is, during plasma etching process, plasma ions, reactive radicals, and UV/VUV photons from the plasma break Si-CH<sub>3</sub> bonds in SiCOH and make the material hydrophilic from hydrophobic.<sup>[3]</sup> As a result, the damaged porous SiCOH easily bonds with moisture and degrades RC time delay by making dielectric constant increased. Recently, many potential solutions to reduce PIDs during the integration with

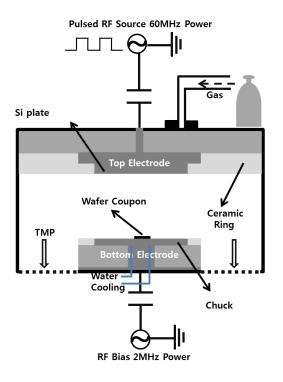
porous SiCOH have been widely investigated using various methods such as pore stuffing<sup>[4-5]</sup>, cryogenic etching<sup>[6-7]</sup>, direct copper etching, etc.<sup>[8]</sup> However, they require additional processes, very low temperature, or a totally different integration scheme. Thus, BEOL(Back End of Line) integration with porous SiCOH still has challenges and it needs more researches to reduce PIDs.

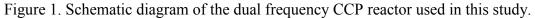
In this study, RF pulsed plasma etching has been investigated to reduce the PID of porous SiCOH dielectric material. Compared to conventional plasma etching, RF pulsed plasma etching can vary etching characteristics such as selectivity, etch profile, PID, uniformity, UV/VUV radiation, and polymerization property by adjusting the pulse frequency and pulse duty cycle.<sup>[9-14]</sup> Among them, this study will specifically focus on the properties of RF pulsed plasma etching for less UV/VUV radiation, lower energy ion species, and higher polarization property to reduce plasma induced damage of an ultra low-k dielectric material. In copper/low-k interconnection, the weakest area to PID is the sidewall because the sidewall damaged layer remaining after the etching tends to increase the capacitance.<sup>[3]</sup> Thus, as a possible solution for the sidewall protection from the PID, an RF pulsed-plasma etching process which may have the properties of less UV/VUV radiation, lower energy ion species, and higher polymerization to the sidewall has been investigated. To prove this hypothesis, a dual-frequency capacitive coupled plasma system (DF-CCP) with a pulsed RF source (60 MHz) and a continuous wave RF bias (2 MHz) was used and the etching properties such as profile, the amount of PID, etc. by using pulsed plasma and conventional (CW) plasma were compared.

### Experimental

#### Equipment **Equipment**

In this study, a dual frequency CCP system as shown in Figure 1 was used in the experiment. The top and bottom electrodes were covered by a silicon plate surrounded by a ceramic ring for the insulation. The distance between two electrodes for RF discharge was 80mm. The top electrode was perforated for gas flow to the chamber and a 60 MHz pulsed RF power source (Pearl CF-3000) was connected to control the plasma characteristics. A 2 MHz RF bias power (ENI GMW-50) was connected to the bottom electrode for ion bombardment onto the substrate and was cooled by water to maintain the substrate at room temperature. The chamber was evacuated by using a turbo molecular pump (3200 l/s) backed by a dry pump.





# Etch samples

A thick SiO<sub>2</sub> and thin SiCN layer were deposited first on Si wafers for good adhesion between the porous SiCOH and the silicon wafer, and a porous SiCOH was deposited. On the SiCOH, a SiON/TiN/SiON multilayer hard mask pattern was formed for good etch selectivity. And the porous SiCOH was etched by using a DF-CCP system with a  $C_4F_8/Ar/O_2/N_2$  gas mixture. The samples etched using both continuous wave plasmas and pulsed plasmas having 1 kHz frequency and 50% duty ratio were compared. The schematic diagrams of the sample for etching and RF pulsing waveforms are shown in Figure 2.

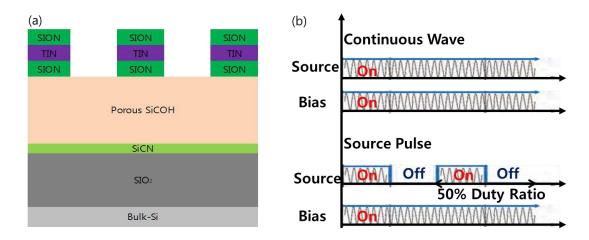


Figure 2. Schematic diagrams of (a) a porous SiCOH pattern structure and (b) continuous wave form and pulsed-wave form used in the experiment.

# Characterization

The etch characteristics such as profile, etch depth, and etch rate of the porous SiCOH were estimated by Field Emission Scanning Electron Microscopy (FE-SEM, Hitachi S-4700). The plasma damage was characterized with FE-SEM by measuring sidewall thickness loss before and after dipping the etched samples in a diluted HF solution (0.5%, 60s). Figure 3 showed the schematic diagram of the etched profile before and after the dipping process for the estimation of the sidewall damage after the etching.

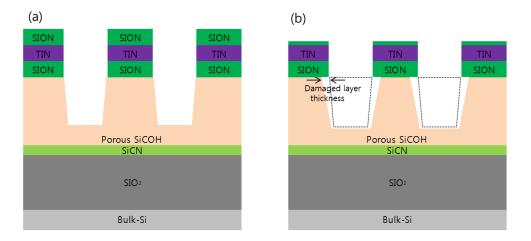


Figure 3. Schematic diagrams of etched profiles (a) before and (b) after a diluted HF dipping process.

# **Results and Discussion**

# Profile Setup

Before investigating the effect of RF pulsing, the etching by using conventional continuous wave (CW) plasmas was conducted for a proper etching condition. Figure 4 (a) – (c) show the SEM images of SiCOH profiles etched with various CW RF power conditions. In order to find a proper RF power, different combinations of source and bias power were conducted and the most anisotropic profile was obtained for the condition of Figure 4 (c), which was the condition of source 100W / bias - 600V.

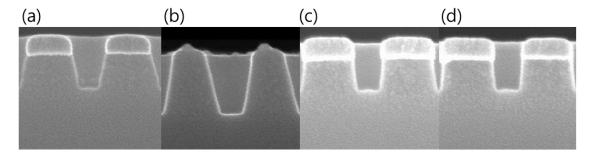


Figure 4. SEM images of etched profiles after the etching by (a) continuous wave / 200W source power / - 600V bias voltage, (b) continuous wave / 200W source power / - 1200V bias voltage, (c) continuous wave / 100W source power / - 600V bias voltage, (d) source pulse /100W source power / - 600V bias voltage.

Excessive source power (200W, Figure 4 (a)) made the profile less anisotropic and excessive bias voltage (-1200V, Figure 4 (b)) made the hard mask more eroded. This may be related to high energy ion species at higher powers and heavy ion bombardment for higher bias voltages. Using the plasma conditions in Figure 4 (c) by pulsing the source power at 50% and at 1kHz, the etched profile of SiCOH as shown in Figure 4 (d) was obtained. In general, compared to CW conditions, the etch profiles for the pulse conditions were more anisotropic. Detailed etch rates and sidewall slopes which indicates the criteria of anisotropic profile are showed in Figure 5.

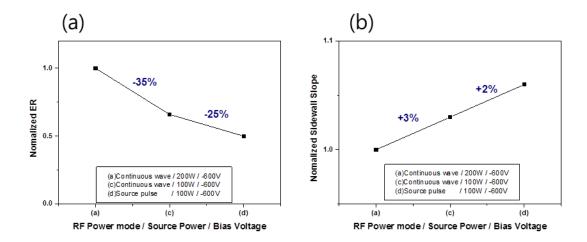


Figure 5. (a) Calculated etch rates and (b) measured sidewall slope angles for the etching of porous SiCOH etched patterns with various CW and pulse conditions.

In Figure 5, the data from Figure 4 (b) having a self-bias voltage of -1200V was removed because all mask layer was eroded. Figure 5 (a) shows the etch rates of porous SiCOH obtained from Figure 4 (a), (c), and (d). The etch rate for the condition of continuous wave / 200W source power / - 600V bias voltage was the highest possibly due to the high energy ion species and, after the source power was decreased by 100W, it dropped by 35%. On the contrary, when the pulse mode (50% at 1kHz) was turned on for the source power of 100W, the etch rate was just decreased by 25% from Figure 4 (c) condition. Figure 5 (b) shows the sidewall angle of the porous SiCOH patterns and, as shown in Figure 5 (b), the slope became more anisotropic as the source power was decreased and as the pulse mode was turned on. The most anisotropic etch profile was obtained for the etching condition with the source pulsing.

#### Damage Characterization and Comparison

In the previous section on profile setup, the optimum etching condition of CW plasma was the condition for Figure 4 (c) with the source power of 100W and the bias voltage of - 600V. In this section, the source pulse mode was turned on based on the optimum CW condition and plasma damage after the etching thick porous SiCOH was compared between two conditions.

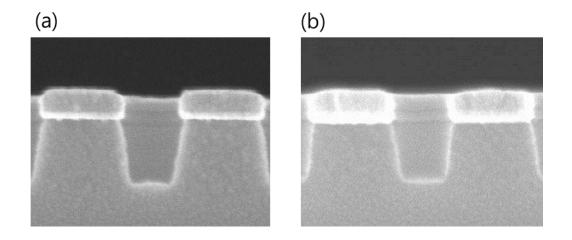


Figure 6. SEM images of SICOH etch profiles after dipping the etched sample in a diluted HF for 60s. (a) Profile for the CW condition (source power 100W / bias voltage - 600V) and (b) profile for the source pulse condition while keeping other conditions the same as (a).

Figure 6 showed the etch profiles after dipping the etched sample into diluted HF for 60s. As HF is used normally as a SiO<sub>2</sub> etchant, the plasma damaged layer on the porous SiCOH could be also etched away because the SiCOH surface is changed to Si-O-Si structure from Si-O-CH structure during the plasma etching process. <sup>[15]</sup> Both profiles showed the loss of a sidewall damaged layer, and the sidewall slope was degraded less anisotropic. However, Figure 6 (b) showed more anisotropic profiles and lower sidewall thickness loss than Figure 6 (a). Detailed damaged thickness loss ratio and slope change are shown in Figure 7.

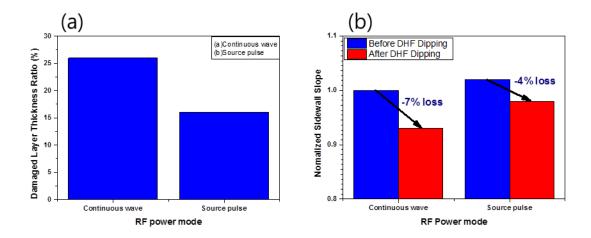


Figure 7. (a) Damaged layer thickness ratio per total CD and (b) sidewall slope change after dipping in a diluted HF solution.

In Figure 7 (a), the damaged layer thickness ratio per CD of the SiCOH for the pulse condition showed lower damage compared to that for the CW condition. Similarly, the sidewall slope change in Figure 7 (b) was less by 4% for the source pulse condition. These results indicate that the etching by using the RF source pulse mode damages porous SiCOH less than the etching by using the CW mode. This is because the pulsed plasma has characteristics of less UV/VUV radiation, lower energy ion species, and higher polymerization <sup>[12-14]</sup>, all yielding lower damage compared to CW plasmas.<sup>[3]</sup> Also, the more anisotropic SiCOH etch profile obtained by the source pulse condition could result in not only less capacitance change but also less leakage current for the interconnection.

#### Conclusions

RF pulsed-plasma etching for porous SiCOH showed more anisotropic profile and less plasma damage characteristics compared to CW plasma etching due to less UV/VUV radiation and lower energy ionic species to the substrate. It also showed lower damaged layer thickness and less sidewall slope change after dipping in a diluted HF solution. Although CW plasma etching at an optimized condition of source power 100W / bias voltage - 600V showed a good etch profile, RF pulsed plasma etching showed a better etch profile and less damage. A disadvantage of using pulsed plasma compared to CW plasma seems to be the etch rate drop. However, it does not look significant because new IC nodes are also being scaled down. It is believed that RF pulsed-plasma etching can be applied as a low damage etching method in advanced IC generations which need more aggressive capacitance target.

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