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Simple Fabrication of Pillar Silicon Nanostructures by a Contact Block Copolymer Technique

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In this study, silicon nanopillar structures were fabricated by a contact block copolymer (BCP) technique, which is a potential technique for the fabrication of self-aligned silicon nanoscale structures. For the contact BCP technique, a nanometer-scale BCP hole pattern was formed on the silicon surface and the silicon, masked with BCP, was exposed to a nitrogen ion beam for surface nitriding. Using the nitride surface as the etch mask, after the removal of the BCP silicon nanopillar structures could be successfully fabricated using a low-energy chlorine-based ion beam. By eliminating the additional steps of hard mask deposition and etching, this technique provided a simplified method of forming a silicon nanostructure. Especially, due to the extremely low thickness of the nitride mask layer, precise transfer of the mask dimension to the silicon was possible. The use of a low-energy ion beam could not only minimize the damage to the nanopillar silicon surface but could also increase the etch selectivity.

Keywords: Pillar-Type Silicon Nanostructure, Block Copolymer, Surface Nitriding, Inverted Ion Beam Etching.

1. INTRODUCTION

Silicon nanostructures have been used in a variety of applications such as in sensors, field effect transistors, solar cells, etc.[1–3] The shapes of the nano-structured materials are very important to control the electrical and optical properties to achieve the desired device performance.[4–7] Especially, the silicon nanopillar structure can be applied in decreasing the surface reflectance significantly and can be used as the low cost nanoimprint master for various applications. Recently, for the fabrication of nanostructures, various lithographic methods such as UV-lithography, *E*-beam lithography, nanoimprinting lithography (NIL), and blocked copolymer (BCP) have been studied. Among these, the photolithography process requires a multi-step deposition/etching technology to overcome resolution limitations. For this reason, the process is becoming increasingly complex and process costs are also going up. With *E*-beam lithography it is easy to pattern a small size, but it is difficult to apply the method to a large area or for mass production due to the low throughput. NIL technology has a fast production speed, but the imprint mask production for it is a very difficult problem. For these reasons, using a BCP to fabrication silicon nanostructures has been widely investigated—owing to the advantages of low production costs and easy mass production.

The most widely used BCP material is polystyrene (PS)-*b*-polymethyl methacrylate (PMMA). Nanoscale PS mask features are formed on the substrates after direct self-assembly (DSA). In order to form a pillar-type silicon nanostructure using BCP, a thin hemispherical PS array formed by the DSA is used as the etch mask. However, due to the problems in dry etch selectivity between the silicon and the PS, rather than using the PS array as the etching mask, after the deposition of some material that is capable of selective etching with silicon the latter material

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is used as the etching mask.[8–11] In general, multiple layers are deposited onto the silicon substrate prior to forming the BCP. And after that, repetitive etching is done while changing the etching gas to have sufficient etch selectivity between the materials deposited on the silicon.[12–14]

In this experiment, a new process was investigated to reduce the repetitive steps for forming 40-nm-wide silicon nanopillars using BCP. On the PS nanosize hole patterns formed on the silicon substrate by DSA, a nitride layer was formed directly on the silicon surface by surface nitriding using nitrogen ions. Using the nitride surface as the mask, silicon was etched by a chlorine-based ion beam, and a silicon nanostructure was formed.

2. EXPERIMENTAL DETAILS

2.1. The Fabrication of the PS Mask Using BCP

The template used as the nitrification mask was a BCP consisting of PS and PMMA. In order to form 40-nm-diameter PS array pattern, 140 kg/mol polystyrene and 65 kg/mol PMMA were dissolved in toluene and the mixed solution was spin-coated on the bare [100] silicon wafer. A thin silicon oxide layer was formed on the silicon surface for the neutralization of the silicon surface. After that, a thermal annealing was performed at 230 °C for 40 hours to form a self-assembled hole structure of PS-*b*-PMMA. The PMMA part of the BCP can be selectively removed by either a wet or dry development method. The wet development is conducted with the procedure of deep UV exposure and PMMA solvent rinsing. With this method it is easy to obtain a high selectivity between the PS and the PMMA but the process time is too long and a degradation problem occurs, such as line edge roughness (LER) due to the porosity of the PS during the direct reaction of the solution. In this experiment, to maintain a complete nanoscale hole array structure of the PS mask after the development, a dry development with Ar/O_2 reactive ion etching (RIE) was used. Dry development was conducted using a 13.56 MHz inductively-coupled plasma (ICP) under the conditions of 3.5 mTorr of operating pressure (the gas ratio of $Ar:O_2$ is 4:1), 200 W of ICP power, 10 W of 13.56 MHz bias power, and 75 sec of process time. As a result, a 40 nm PS hole array mask pattern was formed for the pattern transfer.[15–17]

2.2. Nitride Formation and Etching Processes

A low energy ion beam system was used for nitriding and silicon etching. The reactive ion beam source used in the experiment consisted of an ICP ion gun with three grids, as shown in Figure 1. The reactive ions are formed in the ICP ion source by applying 200 W of 13.56 MHz rf power. The reactive ions were extracted using three grids having a hole diameter of 2 mm. A potential ranging from +10 to +70 V was applied to the 1st grid located close to the ICP source (acceleration grid). A potential of −150 V was applied to the 2nd grid (extraction grid) and the 3rd grid

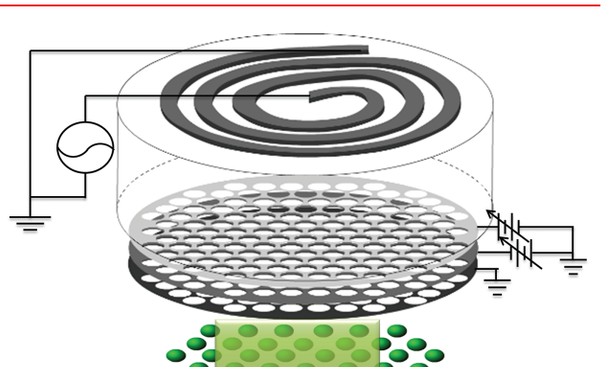

Figure 1. Schematic diagram of the low energy ion gun system with three grids for the energy control of ions used in this study.

was grounded. The temperature of the substrate was maintained at −19 °C by using a chiller. 100 SCCM of N_2 gas was supplied to the chamber for nitriding. A Cl_2/Ne mixture gas with 90 SCCM was used as the silicon etching gas.

2.3. Analysis

Field emission scanning electron microscopy (FE-SEM, Hitachi S-4700) was used for the analysis of the self-assembled BCP and the silicon pattern profile. X-ray photon spectroscopy (XPS; ESCA2000, VG Microtech Inc.) was used to analyze the nitride surface. The etched height was measured with a stylus profilometer (Tencor Alpha-step 500). The ion energy of the ions extracted from the ICP ion source was analyzed using a shop-made ion energy analyzer, into which was installed a current meter (Keithley 2400) and a voltage meter (Hewlett Packard 34401A).

3. RESULTS AND DISCUSSION

In general, it is difficult to form a deep [100] silicon nanostructure using a PS hole pattern mask formed by the self-assembly of BCP with dry etching, due to the etch selectivity problem between the CH-based polymer and silicon. Therefore, silicon nanostructures are generally formed by evaporating a metal such as Cr on the PS holes followed by the lift-off of the Cr metal, or by using an alternate hard mask which is formed by depositing a thin SiO_2 or Si_3N_4 before the BCP processing and etching using the PS hole pattern mask. In this study, a silicon nitride layer was formed directly on the silicon surface masked with the PS hole pattern mask, by silicon surface nitriding using nitrogen ions. And using the nitride surface as the mask, the silicon nanostructure was formed by etching the silicon using a chlorine-based ion beam. The schematic drawing of the procedure for forming the silicon nanostructure by the contact BCP method is shown in Figure 2.

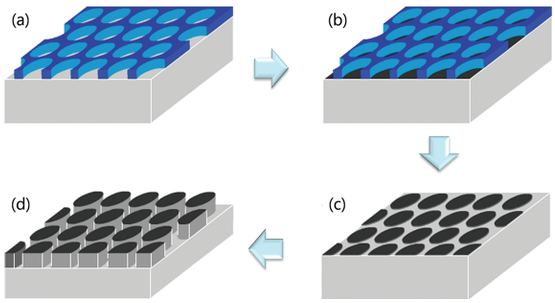

Figure 2. Formation of a pillar-type silicon nanostructures by the contact BCP technique: (a) 40 nm diameter hole pattern of the PS mask on [100] bare Si by the BCP self-assembly, (b) silicon surface nitriding using nitrogen ion beam, (c) stripping PS hole mask sequentially with toluene and acetone, and (d) Si nanopillar structure formed by chlorine-based low energy ion etching.

3.1. Nitrification of the Silicon Surface Masked with PS Hole Array

First, before the formation of silicon nitride with nitrogen ions, the energy distribution of the nitrogen ions bombarding the silicon surface during the nitrification was measured using an ion energy analyzer located near the substrate (about 15 cm away from the ion source) as a function of the 1st grid voltage of the ion source. The results are shown in Figure 3. 100 SCCM of N_2 and 200 W of 13.56 MHz rf power was used for plasma generation in the ICP source of the ion beam. For the nitrogen ion energy measurement, the 1st grid voltage was varied from +10 to +50 V while the 2nd grid voltage of the ion gun was maintained at −150 V and the third grid was grounded. The nitrogen ion energy distribution generally had a Gaussian shape, and showed peak intensity in the range of +17∼+46 eV for +10∼+50 V of 1st grid voltage. Therefore, the energy of the nitrogen ions bombarding the silicon substrate was similar to the 1st grid voltage.

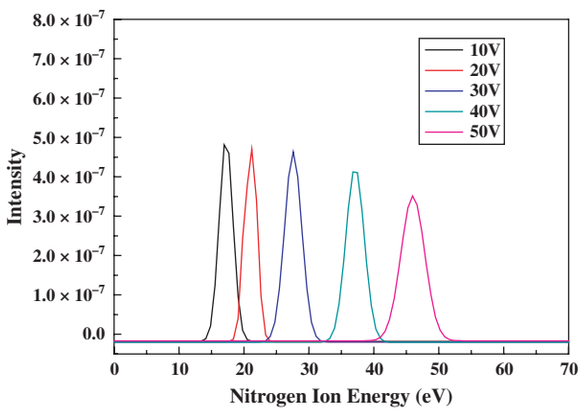

Figure 3. Nitrogen ion energy distribution measured as a function of the 1st grid voltage. (Ion beam source source: 13.56 MHz and 200 W, N_2 100 SCCM, 1st grid: +10∼+50 V, 2nd grid: −150 V).

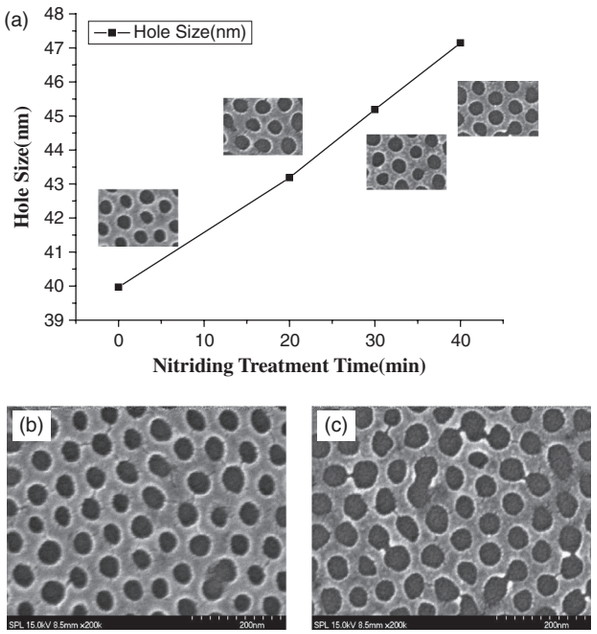

Figure 4. (a) PS hole size change as a function of nitriding time. (b) PS hole reference obtained after BCP self-assembly. (c) Bridging of PS holes observed after nitriding time of 40 min (1st/2nd grid: +35 V/−150 V, and N_2 100 SCCM).

The 40-nm PS hole pattern formed on the silicon surface was exposed to the nitrogen ions, and the effect of the nitrogen ion exposure time on the degradation of the PS hole mask was investigated. For the 1st grid voltage, +35 V was used while other process conditions were maintained the same as those in Figure 3. The silicon substrate masked with the PS hole pattern was maintained at −19 °C. Figure 4(a) shows the change of the PS mask hole size measured as a function of nitriding time. The change of the PS mask hole size was measured using SEM, and SEM micrographs were taken during the

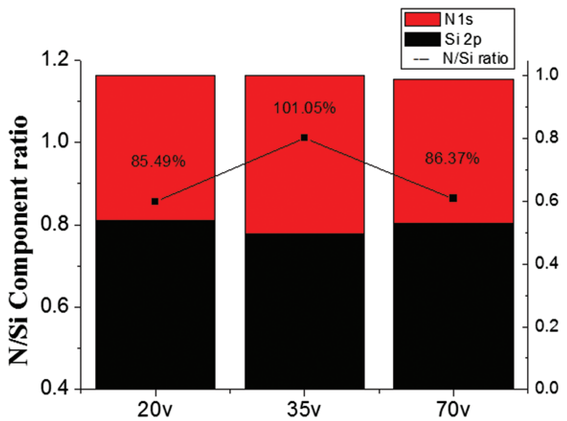

Figure 5. Composition ratio of N/Si measured by XPS as a function of nitrogen ion energy (1st grid voltage). (Nitriding condition: N_2 100 SCCM, 2nd grid potential −150 V, and process time: 40 min).

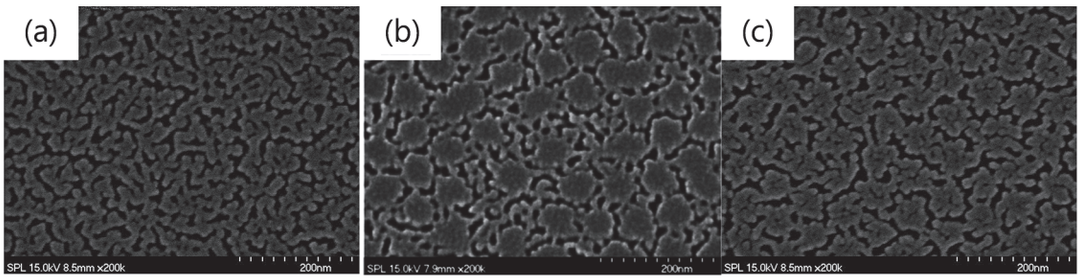

Figure 6. SEM micrographs of the silicon nitride masks after the exposure to Cl_2 plasma for the silicon nitride formed with the conditions of Figure 5. (Nitriding condition : 1st grid potential (a) 20 V (b) 35 V (c) 70 V, Silicon etching condition: Cl_2 90 SCCM, 1st/2nd grid: +30 V/−150 V, and the etching time: 40 min).

nitriding. As shown in Figure 4(a), increased of process time increased the PS hole size by about 0.18 nm/min. No degradation of the PS hole mask pattern shape was observed at up to 30 min of process time—the PS mask shape was similar to the PS mask before the nitridation as shown in Figure (b). But Figure 4(c) shows the PS mask after 40 min of exposure and it exhibits the bridging of PS holes, indicating the initiation of PS mask degradation. Therefore, at the +35 V of 1st grid voltage, less than 40 min of nitridation was required even though the degree of nitridation of the silicon surface could be increased with the increase of process time.

While maintaining the nitridation time for 30 min, the energy of the nitrogen ions was varied from +20 to +70 V to investigate the resultant degrees of nitridation of the silicon surface. Other process conditions were the same as those in Figure 4. Figure 5 shows the silicon surface composition ratio of N/Si, measured for different nitrogen ion energies during the nitridation. The nitridation was carried out on blank silicon wafers to measure the surface composition with XPS. As shown in Figure 5, the increase of nitrogen ion energy from +20 to +35 eV increased the degree of nitridation. However, when the nitrogen ion energy was as high as +70 eV, the degree of nitridation was decreased. The increase of nitrogen ion energy from +20 to +35 eV increases the nitrogen ion penetration depth and therefore a thicker nitride appeared to be formed. However, when the nitrogen ion energy was further increased to +75 V, possibly due to the increase of sputtering of surface silicon, a thinner nitride appeared to be formed at the higher nitrogen ion energy.

3.2. Cl-Based Low-Energy Ion Etching of Silicon

Using the silicon wafers with the PS hole mask nitrified under the conditions of Figure 5, after the removal of the PS hole mask the nitride surface was exposed to a chlorine-based ion beam for 40 min to test the effectiveness of the mask for silicon nanostructure etching. The SEM micrographs of the nitride silicon surface after the chlorine-based ion etching are shown in Figure 6. For silicon etching, chlorine plasma was generated in the ion beam source by supplying 90 SCCM of Cl_2 and by applying 200 W of 13.56 MHz rf power to the ICP source—and to the grids +30 V/−150 V of 1st/2nd grid voltages were applied while the third grid was grounded. The silicon substrate temperature was maintained at 19 °C and the etch time was 40 min. As shown in Figures 6(a and c), for the nitride layer respectively formed with the low 1st grid voltages of +20 V and +70 V, the nitride mask appeared to be etched together with the silicon, possibly due to the thin nitride thickness formed on the silicon at the low nitrogen ion energy as shown in Figure 5. However, for the nitride formed with the 1st grid voltage of +35 V, as shown in Figure 6(b), the nitride surface appeared to act as a mask during the silicon etching by showing more or less circular shapes (that is, the PS hole pattern shape) even though the mask boundary is not clear yet.

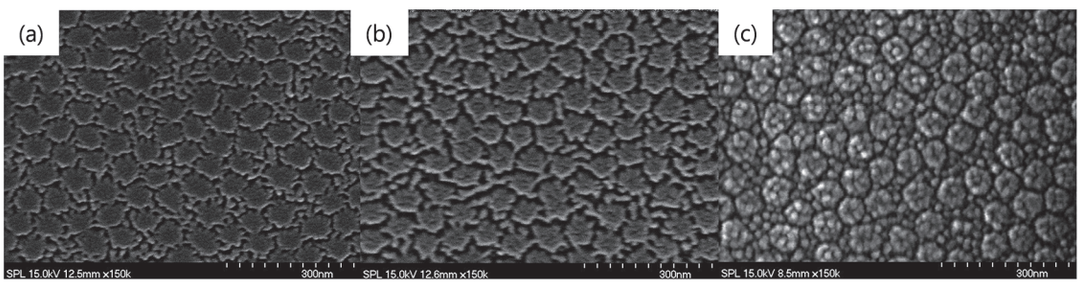

Figure 7. SEM micrographs of the silicon nitride mask formed after etching with different chlorine ion energies, (a) with the 1st grid voltage of 30 V, (b) 40 V, and (c) 50 V. (Nitriding condition: N_2 100 SCCM, 1st/2nd grid: +35 V/−150 V, and process time: 40 min. Silicon etching condition: Cl_2 90 SCCM, 2nd grid: −150 V, and the etching time: 30 min.)

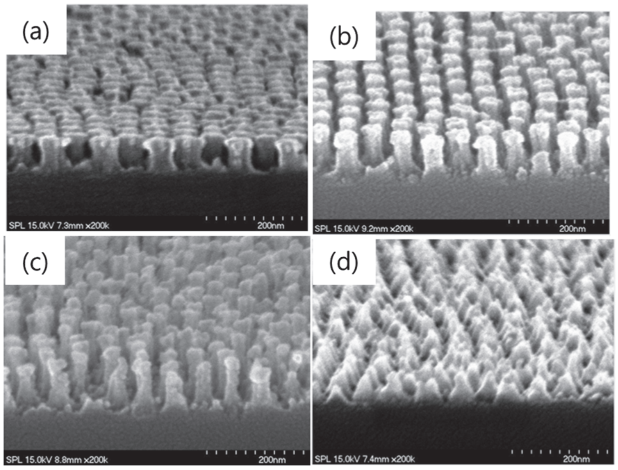

Figure 8. SEM micrographs of silicon nanostructures for different ratios of Ne and Cl during the silicon etching. (a) only Cl_2 etching, (b) Cl_2:Ne = 3:1, (c) Cl_2: Ne = 1:1, and (d) Cl:Ne = 1:2. (silicon etching condition: etching time: 40 min, 1st/2nd grid potentials: +30/−150 V, and mixing gas flow rate: 90 SCCM).

While using the nitride surface formed with +35 V of 1st grid voltage as shown in Figure 6(b), the 1st grid voltage for the silicon etching using Cl_2 ions was varied from +30 V to +50 V (2nd grid voltage: −150 V and the third grid: grounded) and the SEM micrographs observed after the silicon etching are shown in Figures 7(a–c) for +30 V, +40 V, and +50 V, respectively. The Cl_2 plasma was generated with 90 SCCM Cl_2 and by applying 200 W of 13.56 MHz rf power to the ICP source, and the etching time was 30 min. As shown in Figure 7, when the silicon was etched with chlorine ions formed with the 1st grid voltage of +50 V, due to the decreased etch selectivity of the nitride mask with silicon at the high chlorine ion energy the nitride mask was damaged and etched away with silicon as shown in Figure 7(c). However, when silicon was etched with the chlorine ions formed with 1st grid voltage equal to and less than +40 V, as shown in Figures 7(a and b), the nitride mask was not severely damaged and the lower 1st grid voltage showed the least nitride mask damage.

In fact, to obtain PS hole patterns by the self-assembly of BCP on the silicon surface, a thin silicon oxide layer is required on the silicon surface for neutralization before the BCP spin coating. The silicon oxide layer on the exposed silicon surface will be changed to silicon nitride during the nitrification but the silicon oxide layer on the PS mask area remains after the removal of PS mask and it prevents the silicon etching during the etching with the chlorine ions. The rough edges shown in Figures 7(a and b) appear to also be related to the thin silicon oxide layer on the silicon surface. For more selective etching of silicon with the thin silicon oxide, Ne gas was mixed with the Cl_2 gas and the effect of various gas ratios of Ne:Cl_2 on the etched silicon nanostructure shapes was observed. Figure 8 shows the SEM micrographs of the silicon nanostructures formed with (a) Cl_2 only, (b) Cl_2:Ne = 3:1, (c) Cl_2: Ne = 1:1, and (c) Cl_2:Ne = 1:2. Ion source settings were 200 W of 13.56 MHz rf power and +30 V/−150 V of 1st/2nd grid voltage, and the gas flow was maintained at 90 SCCM. When Ne was mixed with Cl_2, the higher silicon etch rate (the etch rate of silicon using Cl_2: Ne = 3:1 was about 30% faster than that using only Cl_2 gas.) and there was a reduced masking effect of silicon oxide. Therefore, more anisotropic silicon nanostructures were observed for Cl_2:Ne = 3:1 compared to the silicon nanostructure obtained with Cl_2 only, as shown in Figures 8(a and b). However, when the Ne ratio was Cl_2:Ne = 1:1, the silicon nanostructure was again degraded and, when the Cl_2:Ne ratio was 1:2, a cone-shaped silicon nanostructure was observed due to the less selective mask selectivity at the high Ne ratio in the gas mixture, as shown in Figures 8(c and d), respectively. (When Ar was mixed instead of Ne, possibly due to the higher sputtering effect of Ar, more degraded silicon nanostructure was observed). For the optimized etch gas ratio of Cl_2:Ne = 3:1, the silicon was etched longer for 45 min. while maintaining the other conditions the same, as in Figure 8, and

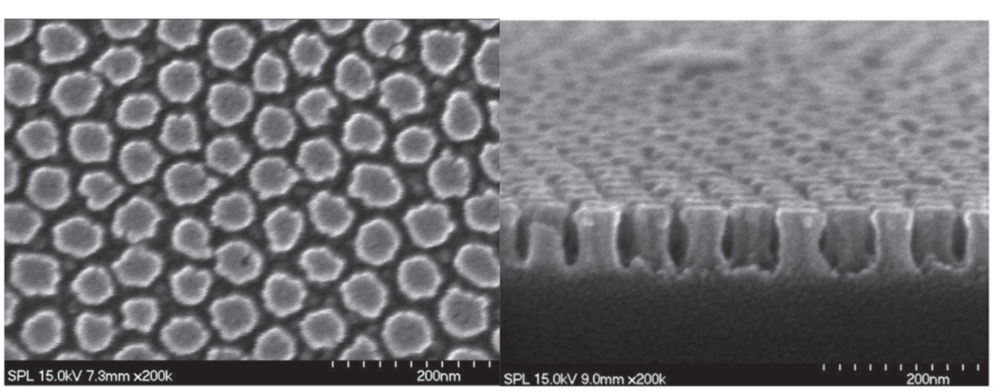

Figure 9. SEM micrograph of an optimized pillar-type silicon nanostructure formed by the contact BCP method. (Nitriding condition: N_2 100 SCCM, 1st/2nd grid: +35 V/−150 V, and process time: 40 min. Silicon etching condition: Cl_2/Ne = 3:1 and 90 SCCM, 2nd grid: −150 V, and the etching time: 45 min).

the SEM micrographs of the silicon nanostructure formed after the etching are shown in Figure 9. As shown in Figure 9, due to the greater selectivity of the nitride mask over the silicon layer, more anisotropic pillar-type silicon nanostructures having heights greater than 100 nm were formed.

4. CONCLUSIONS

A pillar-type silicon nanostructure of 40-nm-scale was fabricated by a contact BCP method which consists of silicon surface nitriding for etch mask formation and Cl_2/Ne ion beam etching for selective silicon etching. The silicon surface nitriding condition and the Cl_2/Ne ion beam etching condition were optimized at low ion energy conditions and the use of low-energy ion beams during the silicon nitrification and silicon etching minimized the damage to the silicon nitride mask. Therefore, etching of pillar-type silicon nanostructures could be made more selective. Even though more investigation is required for more optimization of the process, it is believed that this simple silicon nanoscale pillar production method could be applied for the fabrication of silicon nanostructures while decreasing the device fabrication production cost.

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