Electrical characteristics of buried-Pt Schottky contacts on thin InP/InAlAs heterostructures

Seung Heon Shin, Jong-In Song, and Jae-Hyung Jang[a)]
School of Information and Communications, Center for Wireless Sensor Networks, and WCU Department of Nanobio Materials and Electronics, Gwangju Institute of Science and Technology (GIST), Gwangju 500-712, South Korea

Sang-Duk Park, Jeong-Woon Bae, and Geun-Young Yeom
Department of Advanced Materials Science & Engineering, Sungkyunkwan University, Suwon, South Korea, 440-746

Tae-Woo Kim
Microsystems Technology Laboratory, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139

(Received 26 March 2011; accepted 17 June 2011; published 11 August 2011)

Schottky diodes were fabricated on the InP/InAlAs heterostructures where the thickness of the InP ranges from 0 to 7 nm. A Ne-based atomic layer etching technique was utilized for precise control of the thickness of the InP layer. After removing the part of the InP layer, Pt/Ti/Pt/Au multilayer metallization was evaporated to form a Schottky contact. Thermal annealing was then carried out to drive Pt into the device layer. The electrical characteristics of the Schottky diodes were analyzed to determine the effect of a thin InP layer on the performance of the Schottky diodes. Transmission electron microscopy (TEM) was also utilized to investigate the diffusion of the metal into the semiconductor heterostructures. The experimental results show that the 7-nm-thick Pt can pass through the 4-nm-thick InP layer and reach the InAlAs layer. A Schottky junction was effectively formed within InAlAs layer when the thickness of the InP layer was equal or less than 4 nm for the 7-nm-thick Pt bottom layer. © *2011 American Vacuum Society.* [DOI: 10.1116/1.3610171]

I. INTRODUCTION

The fabrication of ultra-high-speed InP high electron mobility transistors (HEMTs) requires gate recess etching to remove the highly doped cap layer and to allow direct access for gate metallization onto the Schottky barrier layer. Wet chemical etching methods based on various acids such as succinic acid and citric acid were widely utilized to selectively remove the InGaAs cap layer on the top of the InP or InAlAs layer.[1–5] When the selective removal of InGaAs against InAlAs is not readily available, a 2–4-nm-thick AlAs etch stop layer is inserted between the InGaAs cap layer and the InAlAs Schottky layer to achieve better etch selectivity.[6] After InP etch stop layer was introduced to avoid the potential problem of a lattice mismatch between the AlAs layer and other materials in the device heterostructures,[7] it is now commonly used in the HEMT heterostructures.[1,2,8–12] The thin InP layer serves as a surface passivation layer as well as an etch stop layer. By covering the InAlAs surface with InP, transconductance dispersion and kink phenomena could be suppressed.[8] A gate metallization material consisting of Ti/Pt/Au was deposited on top of the InP[1] or InAlAs after removing the thin InP etch stop layer using a dry etching process.[2] When the gate metallization material was evaporated directly onto the InP layer, the Schottky barrier height of the metal/InP junction ($\Phi_B = \sim 0.3$ eV) could not sufficiently achieve a low leakage gate diode. To overcome this drawback, Ar-based reactive-ion-etching (RIE) was utilized to remove the thin InP layer selectively, thus achieving excellent device performance.[2] Ne-based atomic layer etching was also investigated to improve the etch selectivity of InP against InAlAs and to reduce any possible electrical and physical damage during the dry recess etching process.[9,13] If the InAlAs layer is exposed to air after the removal of the InP or AlAs etch stop layer through a wet chemistry or dry etching technique, this raises the possibility of oxidation, which may degrade the performance of the device.

In this article, we investigate a means of fabricating a Schottky contact with an improved barrier height on top of InP/InAlAs heterostructures without removing the thin InP layer. Platinum is known for its ability to penetrate into InP easily.[10–12,14] By employing a post-annealing process, the Pt deposited onto the InP layer can penetrate the InP and reach the InAlAs layer to form a Schottky contact. Cross-sectional transmission electron microscopy (TEM) micrographs show that the Schottky contact was formed within the InAlAs layer. The measured electrical characteristics of the buried-Pt Schottky contact show that the Schottky barrier height was improved to the point that it was similar to that of the buried-Pt on the InAlAs layer.

II. EXPERIMENT

The original Schottky diode heterostructures consisted of a 7-nm-thick InP, 300-nm-thick $In_{0.52}Al_{0.48}As$ barrier (5×10^{16} cm^{-3}), and a 500-nm-thick InAlAs buffer (2×10^{18} cm^{-3}) on top of an n^+-InP substrate. Backside Ohmic

a)Electronic mail: jjang@gist.ac.kr

TABLE I. RMS surface roughness measured after etching the InP layer down to various thicknesses through selective HCl-based wet-etching, Ar-based plasma-etching, and atomic layer etching (ALET).

Etching methods	The thickness of the removed InP layer(nm)	Surface	Surface roughness (Å)
HCl-based wet-etching	7	InAlAs	7.8
Ar-based plasma-etching	7	InAlAs	3.0
	3	4-nm-thick InP	2.1
	4	3-nm-thick InP	2.6
Atomic layer etching	7	InAlAs	1.4

contact was formed by using e-beam evaporation of Ni/Ge/Au (10/45/250 nm), followed by a thermal annealing process at 275 °C for 45 s under N_2 ambient. To determine the penetration dynamics of Pt through an InP layer, InP layers with three different thicknesses, 3, 4, and 7 nm, were utilized in this study. The different InP layer thicknesses were realized through the use of Ne-based atomic layer etching technology (ALET). More detailed information about the particular process used here is available in the literature.[9,13] By employing ALET to remove the InP partially, a very smooth surface morphology was obtained and the surface stoichiometry was preserved. Atomic force microscopy (AFM) was used to measure the rms (root mean square) roughness of the etched sample. The Schottky metallization material consisting of Pt/Ti/Pt/Au (7/20/20/250 nm) was evaporated on top of the InP layer with three different thicknesses. The thickness of the Pt bottom layer was intentionally set to be very close to the original thickness of the InP layer. Thermal annealing processes at various temperatures ranging from 275 to 350 °C were subsequently carried out to drive the Pt into the remaining InP layer. The annealing time was set to be 30 s because the longer annealing at temperatures higher than 325 °C degrades the electrical performance of the Ni/Ge/Au ohmic contacts.

To investigate the movement of the bottom Pt layer onto the semiconductor layer, scanning transmission electron microscopy (STEM) was utilized. The electrical characteristics of the Schottky diodes were measured with a semiconductor parameter analyzer (Agilent, 4155A).

III. RESULTS AND DISCUSSION

The ALET process used in this study had an etch rate of 1.47 Å/cycle for the InP layer and showed better selectivity compared to that observed when using conventional Ar-based plasma.[9,13] With this ALET technology, which uses a much lower level of plasma energy than conventional Ar-based plasma, we could control the thickness of the remaining InP layer to be 3 and 4 nm.

Table I compares the rms roughness of the surface measured by AFM after etching the thin InP layer. The exposed $In_{0.52}Al_{0.48}As$ surface after the etching 7-nm-thin InP etch stop layer using three different etching methods exhibited different degree of surface roughness. The measured rms surface roughness values were 7.8, 3.0, and 1.4 Å for the heterostructures etched by using HCl-based wet-etching, Ar-based plasma-etching, and the ALET process, respectively. The highest rms surface roughness observed from the sample etched with HCl-based wet chemistry is due to the presence of interstitial layer at the interface of the InP and InAlAs layer.[9,15] The smallest rms surface roughness obtained from the sample etched with ALET process is attributed to a combinational etching mechanism of a chlorine-based chemical reaction with the InP layer and the desorption of InP chloride by physical Ne sputtering at a low energy level.[9,13] When the InP layer was partially removed, the surface rms roughness levels of the samples with the 3- and 4-nm-thick InP layer were 2.6 and 2.1 Å, respectively. The surface roughness appeared to increase with an increase of the etching time when the thin InP layer was partially removed, but it was reduced to its minimum value when the InAlAs layer was exposed due to the high etching selectivity of InP against InAlAs.

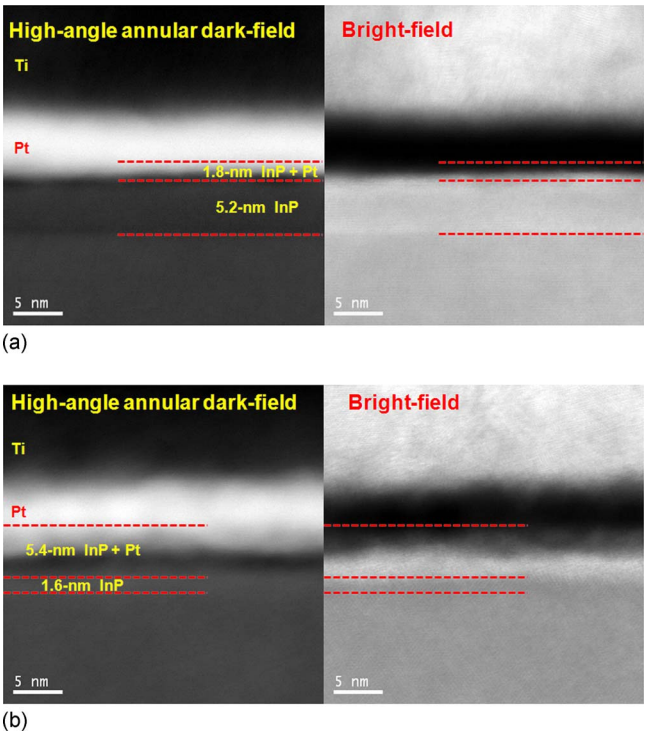

FIG. 1. (Color online) (a) Bright-field (left) and high-angle annular dark-field (right) STEM images of the Schottky contact fabricated on a 7-nm-thick InP layer. (b) Bright-field (left) and high-angle annular dark-field (right) STEM images of the Schottky contact fabricated by utilizing buried-Pt technology on 7-nm-thick InP layer annealed at 325 °C.

To investigate the movement of the Pt into the Schottky diode heterostructures during the thermal annealing process, a STEM study was carried out. Figures 1(a) and 1(b) depict bright-field (BF) and high-angle annular dark-field (HAADF) STEM images of a Schottky contact on the 7-nm-thick InP layer. The diffusion depth can be determined directly by measuring the distance between the metal-semiconductor interface and the InP layer of the STEM contour plot. The STEM images of the nonannealed Schottky contact on the 7-nm-thick InP layer in Fig. 1(a) show that the Pt atoms penetrate into the InP layer by 1.8 nm during the

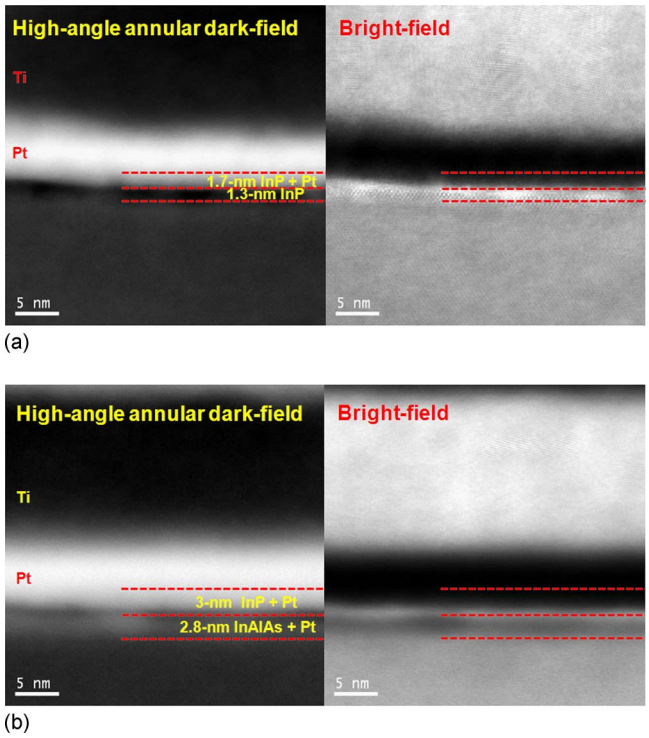

FIG. 2. (Color online) (a) Bright-field (left) and high-angle annular dark-field (right) STEM images of the Schottky contact fabricated on 3-nm-thick InP layer. (b) Bright-field (left) and high-angle annular dark-field (right) STEM images of the Schottky contact fabricated by utilizing buried-Pt technology on 3-nm-thick InP layer annealed at 325 °C.

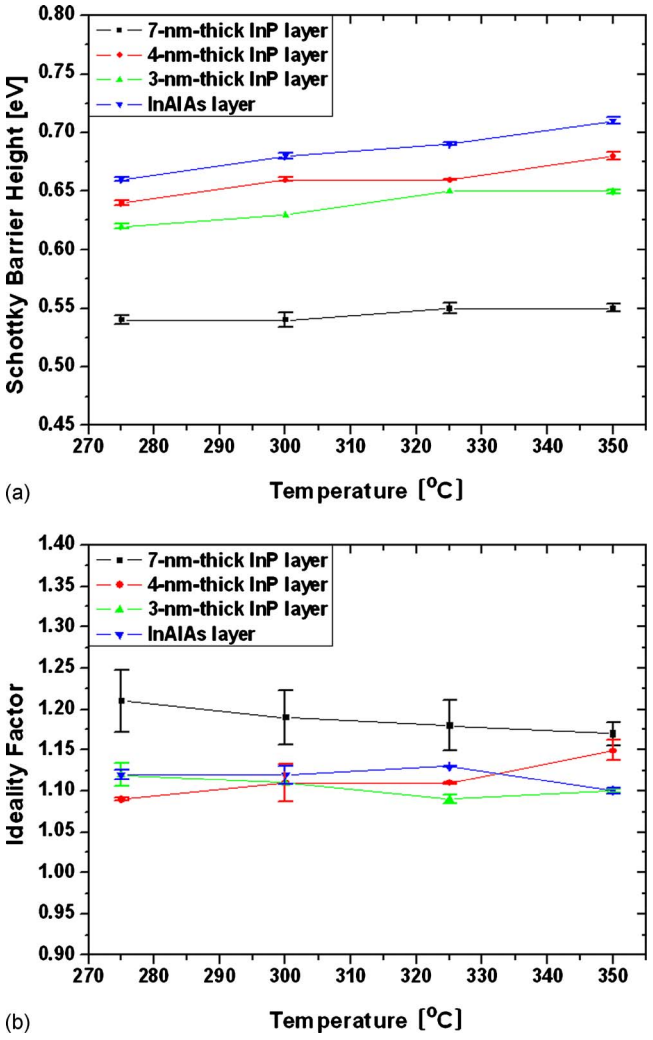

FIG. 3. (Color online) (a) Schottky barrier heights and (b) ideality factors with respect to the annealing temperatures for various Schottky diodes fabricated on InP/InAlAs heterostructures having different InP layer thicknesses. The top and bottom of the error bars correspond to $m \pm \sigma$, where m and σ are the mean and standard deviation of the measured quantities, respectively.

evaporation of the Schottky contact metallization material. After postannealing at 325 °C for 30 s, the Pt diffused 3.6 nm further into the InP layer, as shown in Fig. 1(b). The resulting InP layer thickness was 1.6 nm.

Figures 2(a) and 2(b) show the cross-sectional STEM images of the Schottky contact on a 3-nm-thick InP layer before and after annealing. The STEM image of the nonannealed Schottky contact in Fig. 2(a) shows that the Pt atoms diffused into the InP layer by 1.7 nm during the evaporation of the Schottky contact metallization material, which is essentially the same diffusion depth observed with the nonannealed Schottky contact on the 7-nm-thick InP layer shown in Fig. 1(a). After thermal annealing at 325 °C for 30 s, the bottom of the Pt layer completely passed through the 3-nm-thick InP layer and established contact with the InAlAs layer, as shown in Fig. 2(b). The Pt atoms passed 2.8 nm further through the 1.3-nm-thick InP layer and penetrated into the InAlAs layer as a result of the thermal annealing process. Considering that the diffusion depths of the Pt during the postannealing process were 3.6 and 4.1 nm for the 7- and 3-nm-thick InP layer, respectively, the diffusion of Pt through the InAlAs layer was much easier than that through the InP layer.

Figure 3 shows the Schottky barrier heights and ideality factors of Schottky diodes fabricated on heterostructures with InP layers of four different thicknesses. These parameters were extracted using the standard current-voltage (I-V) method.[16] The Schottky barrier heights of the samples annealed at 325 °C for 30 s were 0.69, 0.65, 0.66, and 0.55 eV for the devices with 0, 3-, 4-, and 7-nm-thick InP layers. The highest Schottky barrier height was obtained from the diodes fabricated directly on top of the InAlAs layer that was prepared by removing InP layer completely by using ALET process. As clearly shown in Fig. 2, the bottom of the Pt layer completely passed through the 3-nm-thick InP layer and reached the InAlAs layer to form a Schottky contact. Pt atoms reacting with As in the InAlAs layer produce amorphous layer of $PtAs_2$ which increase the Schottky barrier height[17,18] as in the Pt/GaAs system through thermal annealing process.[19] By forming the Schottky contact with the InAlAs layer, the Schottky barrier heights of the samples with the 3- and 4-nm-thick InP layer were much higher than that of the sample with the 7-nm-thick InP layer. Although the Schottky contact was formed within the InAlAs layer for the devices with 3- and 4-nm-thick InP layer layers, the Schottky metallization material still made contact with the InP layer at the

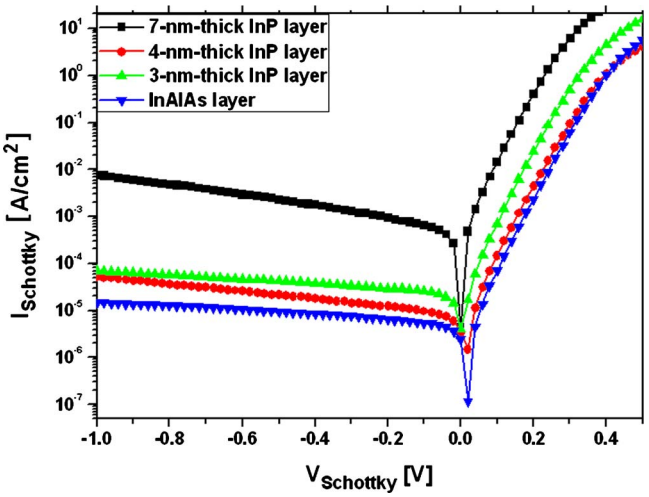

FIG. 4. (Color online) *I-V* characteristic of the Schottky diodes fabricated on InP/InAlAs heterostructures having different InP layer thicknesses through a thermal annealing process at 350 °C.

edge of the Schottky contacts. The surface of the etched InP layer is also rougher than the InAlAs surface. The rougher surface has the higher surface defect density leading to the higher leakage current[20,21] and the lower Schottky barrier height.[22,23] Thereby, Schottky barrier heights of the contacts on 3- and 4-nm-thick InP layers were slightly lower than those of the contacts created directly on top of the InAlAs layer. Interestingly, the contacts formed on the 4-nm-thick InP layer exhibited a higher Schottky barrier height than those formed on the 3-nm-thick InP layer. This can also be ascribed to etching-related surface roughness at the interface and possible damage on the surface caused during etching. The surface roughness of the etched surface was greater in the 3-nm-thick InP layer than it was in the 4-nm-thick InP layer. The surface roughness increased with an increase of the etching time, despite the fact that it is much lower than the surface roughness of the samples etched with other etching technology.[9,13]

For all of the samples investigated in this study, the Schottky barrier height increased with a higher annealing temperature. Pt reacted with the InP layer as well as the InAlAs layer to form Schottky contacts with improved Schottky barrier heights. The ideality factors of the diodes show that all of the contacts were fairly stable, as shown in Fig. 3(b).

Figure 4 shows *I-V* characteristics of Schottky diodes with different InP thicknesses after a thermal annealing process at 350 °C. The revere leakage current slopes of the Schottky diodes on the 3-nm-thick InP layer and the InAlAs layer look similar. And the Schottky diodes on the 4-nm and 7-nm-thick InP layers exhibit the similar reverse leakage current slopes. However, the leakage current level of the devices with the 3-nm-thick InP layer is higher than that of the devices with the 4-nm-thick InP layer, which can be ascribed to the higher surface roughness observed in the 3-nm-thick InP layer after etching.

IV. CONCLUSION

Buried-Pt Schottky contacts were fabricated on top of InP/InAlAs heterostructures with different InP thicknesses. Although the Schottky metallization material was deposited on top of 3- and 4-nm-thick InP layers, the performance of the Schottky diodes was much better than those fabricated on a thick InP layer because the 7-nm-thick Pt penetrated through the thin InP layer and formed a Schottky contact effectively on the InAlAs layer. When this technique is applied in the HEMT fabrication process, an InP etch stop layer with a thickness of equal or less than 4 nm may not need to be removed. By removing the need of dry gate recess etching process, a more robust HEMT fabrication process can be achieved.

ACKNOWLEDGMENTS

This work was supported by KRF Grant No. D00714, by the Center For Distributed Sensor Network (CDSN) at GIST, and by the World Class University (WCU) program through the KRF funded by the MEST (Grant No. R31-2008-000-10026-0). The authors would like to thank Y. K. Kim at UNIST and NCNT at POSTECH in Korea for the help with STEM analysis.

[1]Takatomo Enoki, Hiroshi Ito, Kenji Ikuta, Yohtaro Umeda, and Yasunobu Ishii, Microwave Opt. Technol. Lett. **11**, 135 (1996).
[2]T. Suemitsu, H. Yokoyama, Y. Umeda, T. Enoki, and Y. Ishii, IEEE Trans. Electron Devices **46**, 1074 (1999).
[3]D. Moran, E. Boyd, H. McLelland, K. Elgaid Y. Chen, D. S. Macintyre, S. Thoms, C. R. Stanley, and I. G. Thayne, Microelectron. Eng. **67–68**, 769 (2003).
[4]David A. J. Moran, Helen McLelland, Khaled Elgaid, Griogair Whyte, Colin R. Stanley, and Iain Thayne, IEEE Trans. Electron Devices **53**, 2920 (2006).
[5]J. H. Jang, S. Kim, and I. Adesida, Solid-State Electron. **50**, 852 (2006).
[6]Aaditya Mahajan, Mohamed Arafa, Patrick Fay C. Caneau, and I. Adesida, IEEE Trans. Electron Devices **45**, 2422 (1998).
[7]David R. Greenberg, Jesús A. del Alamo, and Rajaram Bhat, IEEE Electron Device Lett. **13**, 137 (1992).
[8]G. Meneghesso, D. Buttari, E. Perin, C. Canali, and E. Zanoni, Tech. Dig. - Int. Electron Devices Meet. **1998**, 227.
[9]T.-W. Kim, J.-I. Song, J.-H. Jang, D.-H. Kim, S. D. Park, J. W. Bae, and G. Y. Yeom, Appl. Phys. Lett. **91**, 012110 (2007).
[10]Keisuke Shinohara, Wonill Ha, and Mark J. W. Rodwell, IEEE International Conference on Indium Phosphide and Related Materials, 2007, p. 18.
[11]Chien-I Kou, Heng-Tung Hsu, Edward Yi Chang, China-Yuan Chang, Yasuyuki Miyamoto, Suman Datta, Marko Radosavljevic, Guo-Wei Huang, and Ching-Ting Lee, IEEE Electron Device Lett. **29**, 290 (2008).
[12]Seung Heon Shin, Tae-Woo Kim, Jong-In Song, and Jae-Hyung Jang, Solid-State Electron. **62**, 106 (2011).
[13]S. D. Park, C. K. Oh, W. S. Lim, H. C. Lee, J. W. Bae, G. Y. Yeom, T. W. Kim, J. I. Song, and J. H. Jang, Appl. Phys. Lett. **91**, 013110 (2007).
[14]Y. Ashizawa, C. Nozaki, T. Noda, and A. Sasaki, IEEE International Conference on Indium Phosphide and Related Materials, 1995, p. 861.
[15]M. Takakusaki, H. Momoi, K. Kakuta, and H. Nakata, Proceedings of the GaAsMANTECH Conference (unpublished), 2003, p. 8.13.
[16]Ralph E. Williams, *Gallium Arsenide Processing Techniques* (Artech House, Inc., London, 1984), p. 267.
[17]Seiyon Kim, Heedon Hwang, and Ilesanmi Adesida, Appl. Phys. Lett. **87**, 232102 (2005).

[18]N. Harada, S. Kuroda, T. Katakami, K. Hikosaka, T. Mimura, and M. Abe, IEEE International Conference on Indium Phosphide and Related Materials, 1991, p. 377.
[19]Dae-Hong Ko and Robert Sinclair, J. Appl. Phys. **72**, 2036 (1992).
[20]M. L. Green, T. W. Sorsch, G. L. Timp, D. A. Muller, B. E. Weir, P. J. Silverman, S. V. Moccio, and Y. O. Kim, Microelectron. Eng. **48**, 25 (1999).
[21]Se Hoon Oh, Kyung Woong Park, Jeong Hee Park, Boum Seock Kim, and Duck Kyun Choi, J. Vac. Sci. Technol. B **18**, 1923 (2000).
[22]M. Wittmer and J. L. Freeouf, Europhys. Lett. **26**, 135 (1994).
[23]Kung-Yen Lee and Michael A. Capano, J. Electron. Mater. **36**, 272 (2007).