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Effects of Etch-Induced Damage and Contamination on the Physical and Electrical Properties of Cobalt Silicides

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Damage and residue remaining on the silicon wafer after oxide overetching using C_4F_8/H_2 plasmas and the effects of various post treatments after the overetching on the formation of contact silicides were investigated. The Co silicides formed on the variously etched surfaces were unstable, therefore, the sheet resistances were high and dependent on the etching conditions. However, stable Co silicides could be formed on the etched silicon surfaces regardless of etch conditions after O_2 plasma cleaning followed by thermal annealing at 600°C and the sheet resistance and the thickness of the silicides were close to those of the silicides formed on a clean control silicon surface. The formation of stable Co silicides was more dependent on the characteristics of the residue than on the damage remaining on the silicon surface. The effects of the remanent residue and damage on the formation of stable silicides following Ti silicidation were similar to those following Co silicidation.

KEYWORDS: helicon plasma etching, damage, residue, contact silicides, oxide etching

1. Introduction

High-density plasma etchings are promising for the manufacture of submicron contact holes with a large aspect ratio in semiconductor devices and require high C/F (carbon/fluorine) ratio gases or hydrogen-containing gases to improve the etch selectivities.[1)] However, the use of these gases often generates a thick residue layer and physical or electrical damage on the silicon during the oxide overetch period.[2,3)] As the depth of the contact junction becomes shallower according to the scaling rule, minimization of the etch-induced damage and residue is a prerequisite for the next generation semiconductor devices. However, the minimization of etch-induced damage and residue during the oxide overetching is not always available depending on the process conditions, therefore, post-etch processes for removing the damage and residue formed during the oxide overetching should be used. Practically, a clean, etched silicon surface may only be obtained by optimization of both the specific etch processes and the subsequent post-etch treatment processes such as cleaning and annealing. However, some damage and residue could remain even after the post-etch processes depending on the characteristics of the damage and residue.[4,5)]

Generally, contact silicides are formed on etched and cleaned silicon surfaces by the deposition of metal followed by a silicidation process. Contact silicides may have to be formed on etched silicon surfaces having residual damage or residue if these were not completely removed during the post-etch processes, however, few studies on the effects of residual damage or residue on the formation of stable contact silicides have been reported.[5–7)] In this study, the effects of residual damage and residue after oxide overetching and post-etch cleaning on the formation of stable contact silicides have been investigated. Co silicide was studied as the contact silicide in this study, and some of the results were compared with the results obtained using the Ti silicide, to study the effects of different silicide materials.

2. Experimental

To study the effects of damage and residue on contact silicidation, 1-μm-thick phosposilicate glass (PSG) deposited on silicon wafers was etched using 100%C_4F_8 and 70%C_4F_8/30%H_2 helicon plasmas for a 50% overetch time after the endpoint. A source power of 1.5 kW was applied to the antenna while the operating pressure was kept at 1.5 mTorr and the total flow rate at 30 sccm. Separate rf bias power was varied to achieve -80 V or -120 V of dc self-bias voltage on the substrate. In addition, to generate damage on the etched silicon surface without a fluorocarbon residue, seperate etchings were performed using 100%HBr and 50%Ar/50%H_2 plasmas at a dc self-bias voltage of -150 V. The 50%-overetched silicon wafers were cleaned using different post-etch cleaning processes to remove etch-induced residue,and annealed to remove etch-induced damage. The silicon wafers were cleaned using a piranha cleaning solution (H_2SO_4 : $H_2O = 4 : 1$, 90°C) for 10 min. O_2 plasma cleaning was also performed using a microwave plasma asher (ASTEX Co.) at 200 W, 500 mTorr, and substrate temperature of 120°C for 40 min. To further remove damage and remaining residue, the overetched silicon wafers were annealed at 600°C for 30 min in N_2 after O_2 plasma cleaning. The characteristics of the residues remaining on the variously etched, cleaned, and annealed silicon surfaces were investigated using X-ray photoelectron spectroscopy (XPS), and the thickness of the remaining residue was measured using an ellipsometer. The degree of damage remaining on the silicon wafers was estimated by measuring the carrier lifetimes.

On the etched, cleaned, and annealed silicon wafers, Ti silicide and Co silicide were formed to study the effects of the remaining residue or damage on the formation of stable silicides. To fabricate silicides, 500 Å of Co and Ti were evaporated using an e-beam evaporator on etched, cleaned, and annealed silicon wafers after dipping in a diluted HF solution for 30 s. Rapid thermal annealing at 800°C for 1 min under 500 mTorr in an Ar atmosphere was used to form contact silicides. The sheet resistances of Ti and Co silicides were measured using a four-point probe after the wet etching of residual Co and Ti using HNO_3/H_2O and $HF/H_2SO_4/H_2O$, respectively. In the case of the Co silicides, the physical properties were investigated in greater detail using cross-sectional transmission electron microscopy (TEM) and X-ray diffraction (XRD). Clean, nonetched silicon wafers (control) were

always included in the analyses as reference.

3. Results and Discussion

Table I shows the etching characteristics for various oxide etchings, the damage and residue remaining on the silicon surface as measured using XPS, and the carrier lifetime measurements after 50% overetching, for the case of 1-μm-thick PSG. The use of hydrogen in C_4F_8 (70%C_4F_8/30%H_2 instead of 100% C_4F_8) generally resulted in a decrease in PSG etch rates, however, an increase in the PSG etch selectivity over silicon due to the increased effective C/F ratio of the plasma.[8] Increase of dc self-bias voltage from -80 V to -120 V generally increased PSG etch rate without reducing the etch selectivity, possibly due to the enhanced ion bombardment. The composition of the residue measured using XPS on the silicon surface after the overetchings showed higher C/F ratio for 70%C_4F_8/30%H_2 compared to 100% C_4F_8 and for the higher dc self-bias condition (-120 V). The measurement of carrier lifetimes indicating the extent of damage remaining on the silicon surface after overetching, revealed a shorter carrier lifetimes; therefore, there was more damage for the case of 70%C_4F_8/30%H_2 compared to that for 100%C_4F_8, possibly due to the hydrogen and the higher dc self-bias condition, due to the increased ion bombardment energy.[9,10] In the case of silicon etchings with 100%HBr and 50%Ar/50%H_2, which were investigated to study the effects of only damage on the subsequent formation of silicides, independent of the effect of the residue described above, the measured carrier lifetimes were 0.8–10 μs and 15–45 μs, respectively. Therefore, these etched silicon surfaces were more severely damaged than those etched under the etch conditions described in Table I.

Table II shows the carbon bonding states of the residue for different etching conditions measured by narrow scan XPS. As the bias voltage is increased or hydrogen is added to the plasma, C–F_x ($x = 1, 2, 3$) bonding states decreased and C–C(/H) bonding states increased. In paticular, strong C–Si bonding, which is known to be critical for the formation of a stable silicide,[6] was observed on the etched silicon surface and also increased with dc-self bias voltage and the addition of hydrogen in the plasma.

The thickness of the residue remaining on the silicon for the etch conditions listed in Table I was measured as a function of the post-etch treatment using an ellipsometer and is shown in Fig. 1. As shown in the figure, the use of hydrogen and the use of lower bias voltage for the etching led to increased the thickness of the residue. Figure 1 also shows the effect of different cleanings and annealing treatments after the various overetching processes on the thickness of the remaining residue. O_2 plasma cleaning was more effective than Piranha cleaning in reducing the thickness of residue, and annealing at 600°C after O_2 plasma cleaning further reduced the thickness of residue, to close to that of control sample. The refractive index of the residue after the annealing process at 600°C was close to 1.5, the same value as that of native oxide.

On the above variously etched, cleaned and annealed silicon wafers, Co silicides were formed, and their physical and electrical properties were investigated. Figure 2 shows the XRD data obtained for the Co silicides formed on silicon surfaces overetched using (b) 100%C_4F_8 (-80 V), (c) 70%C_4F_8/30%H_2 (-80 V), (d) 70%C_4F_8/30%H_2 (-120 V), and on silicon surfaces post-etch-treated using (e) O_2 plasma cleaning and (f) O_2 plasma cleaning followed by annealing at 600°C, after overetching with 70%C_4F_8/30%H_2 (-120 V). XRD data of Co silicide (a) formed on a clean nonetched silicon surface (control) is included in the figure. In the case of silicides formed on the control wafer and on silicon wafers overetched using 100%C_4F_8 (-80 V), XRD peaks corresponding to stable $CoSi_2$ such as (111), (220), and (331), were observed, but no peaks from unstable CoSi or Co_2Si were detected. However, in the case of silicides formed on silicon wafers etched using 70%C_4F_8/30%H_2, small peaks from Co_2Si and CoSi and the peaks from Co_2Si and CoSi were observed for the low dc-bias volt increased for the higher dc-bias voltage condition of -120 V. The peaks from Co_2Si and CoSi for 70%C_4F_8/30%H_2 (-120 V) were reduced after O_2 plasma cleaning and they disapeared completely after O_2 plasma cleaning followed by annealing at 600°C, similar to the controls.

Cross-sectional TEM was used to observe the morphology of the silicides formed for 70%C_4F_8/30%H_2 (-80 V). Figure 3 shows the cross-sectional TEM micrographs of silicides formed on silicon wafers (a) nonetched (control), (b) etched using 70%C_4F_8/30%H_2 (-80 V), (c) cleaned using O_2

Table I. Etch characteristics, surface composition of the residue, and carrier lifetime as a function of various PSG etching conditions.

Etching chemistry (bias voltage)	PSG etch rate (Å/min)	Selectivity to Si	Composition Si : C : F : O	Carrier lifetime (μs)
100%C_4F_8 (-80 V)	6700	10.5	17 : 36 : 36 : 11	300–330
100%C_4F_8 (-120 V)	9100	13	30 : 37 : 19 : 14	135–165
70%C_4F_8/30%H_2 (-80 V)	4500	20.5	14 : 42 : 32 : 12	195–220
70%C_4F_8/30%H_2 (-120 V)	6500	25	22 : 45 : 20 : 13	75–110
Control (non-etched silicon)			69 : 18 : 0 : 13	380–410

Table II. Carbon bonding states of the remaining residue for different PSG etching conditions as measured by narrow scan XPS.

Etching chemistry	C–F_1	C–F_2	C–F_3	C–C(/H)	C–CF_x	C–Si
100%C_4F_8 (-80 V)	26.5	15.7	6.4	14.4	31.8	5.2
100%C_4F_8 (-120 V)	17.4	6.6	4.0	19.7	38.4	13.9
70%C_4F_8/30%H_2 (-80 V)	23.0	13.0	4.0	17.0	36.0	7.0
70%C_4F_8/30%H_2 (-120 V)	14.0	4.0	2.0	22.5	41.0	16.5

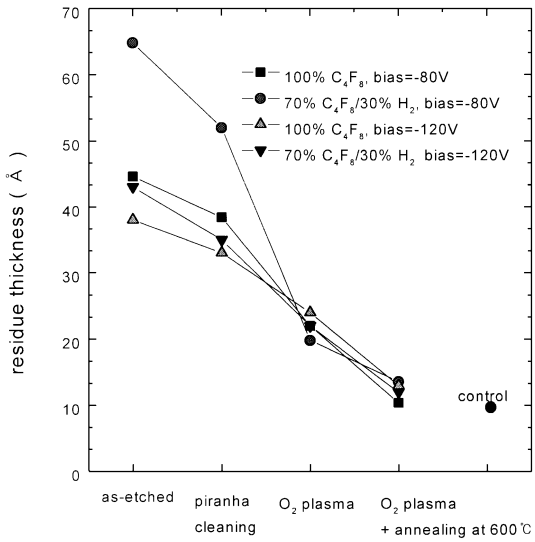


Fig. 1. Thickness of the residue remaining on variously etched, cleaned, and annealed silicon surfaces measured using an ellipsometer.

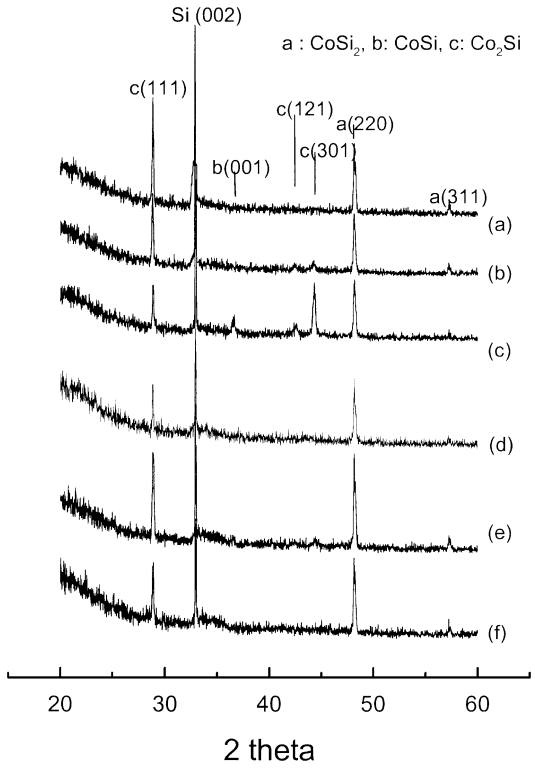


Fig. 2. XRD patterns of the cobalt silicides fabricated on silicon surfaces (a) control, (b) etched using (b) 100%C_4F_8 (−80 V), (c) 70%C_4F_8/30%H_2 (−80 V), and (d) 70%C_4F_8/30%H_2 (−120 V), and (e) O_2 plasma-cleaned after (d),and (f) annealed at 600°C after (e).

plasma after (b), and (d) annealed at 600°C after (c). For all of the samples, a layer of Co was observed on the top of the sample due to the incomplete Co silicidation process used in the experiment. In addition, no noticeable differences in the roughness of the silicide interface were observed. However, the thickness of the silicide was different depending on the sample. The control sample showed a silicide thickness of 140–170 nm, the etched sample showed a thickness 130–150 nm, and both the O_2 plasma-cleaned sample and the sample annealed at 600°C showed a thickness 140–180 nm. Therefore, thinner Co silicide films were formed on the silicon wafers etched using 70%C_4F_8/30%H_2 compared to those

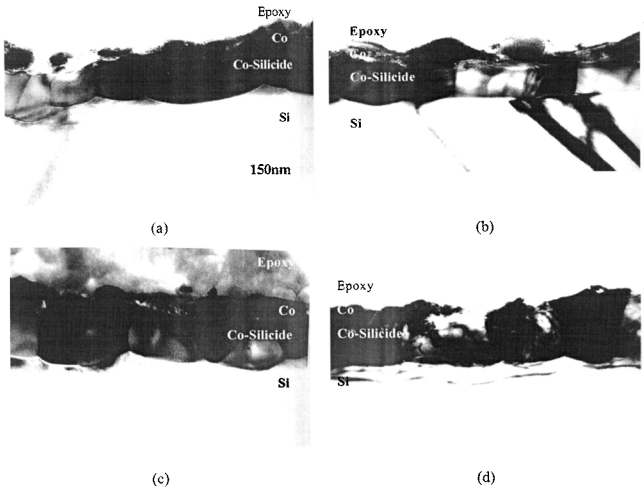
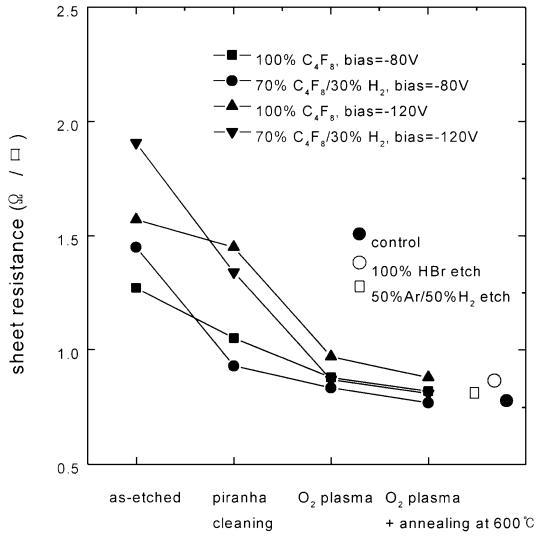


Fig. 3. Cross-sectional TEM image of the silicon surface (a) control, (b) etched at −80 V of bias voltage using 70%C_4F_8/30%H_2, (c) cleaned by O_2 plasma after (b), and (d) annealed at 600°C after (c).

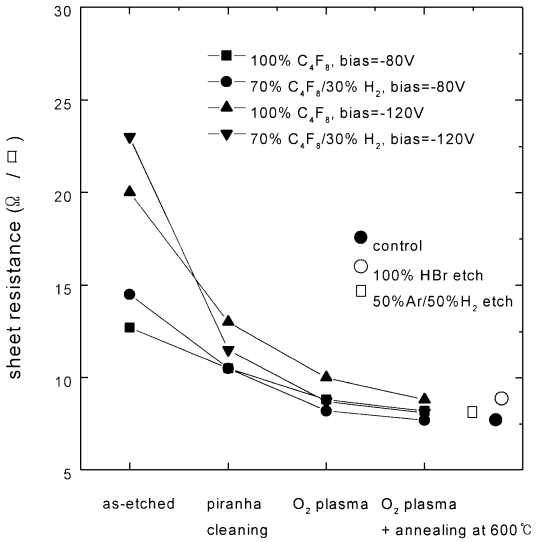
formed on the control, and the thickness of the silicide was rerestored after O_2 plasma cleaning. The thicknesses of the Co silicides formed on the silicon surfaces overetched using 70%C_4F_8/30%H_2 (−120 V) and cleaned using O_2 plasma cleaning and thereafter by annealed at 600°C were also estimated by cross-sectional TEM (data not shown). The thickness of the Co silicides formed on overetched silicon wafers measured 115–130 nm, and those formed on the overetched silicon wafers after O_2 plasma cleaning followed by annealed at 600°C measured 135–180 nm.

Figure 4(a) shows the sheet resistances of the Co silicides fabricated on etched, cleaned, and annealed silicon surfaces. As a reference, the sheet resistance of the Co silicide formed on a clean control wafer was included. The sheet resistances of the Co silicides formed on the as-etched silicon surfaces were the highest and were reduced to the control value (0.8 Ω/square) as cleaning and annealing proceeded.[11] The decrease in sheet resistances following the cleaning and annealing under the same etch conditions was similar to the decrease in residue thickness shown in Fig. 1. On the other hand, the sheet resistances determined for four different etching conditions had different values for only as-etched and piranha-cleaned wafers. In regard to the as-etched wafers, higher sheet resistances were obtained for Co silicides formed on silicon wafers etched at a higher bias voltage and with hydrogen-containing plasma (70%C_4F_8/30%H_2). One the other hand, the increase in sheet resistance could be related to the damage remaining on the etched silicon wafers. Therefore, the sheet resistances of Co silicides formed on the severely damaged silicon surfaces having no residue were also measured. The silicon wafers having only damage were prepared by etching with 100%HBr and 50%Ar/50%H_2 plasmas. The sheet resistances of these Co silicides (0.8–0.9 Ω/square) were only slightly higher than the control value, therefore, the damage itself was not responsible for the increase in the sheet resistance of Co silicide formed on etched silicon. The little or no influence of etch-induced damage on the sheet resistance may be related to the consumption of the damaged silicon layer during the silicidation process.

The relationship between the sheet resistance value and the thickness of the residue appears to be significantly related to the chemistry of the residue. As mentioned in Tables I and



(a)



(b)

Fig. 4. Sheet resistances of the (a) Co silicides and (b) Ti silicides fabricated on variously etched, cleaned, and annealed silicon surfaces.

II, the composition of the residue is varied for different gas chemistries and dc-bias voltage conditions. The C/F ratio and C–Si bondings are the greatest for the 70%C_4F_8/30%H_2 (−120 V) condition, simliar to that of the sheet resistance shown in Fig. 4(a). A previous study[5] has shown that fluorine-rich residue (C/F ratio is 0.73) blocks more effectively the formation of stable silicides compared to a residue containing more carbon (C/F ratio is 1). In the current experiment, the silicides formed on the more carbon-rich residues (C/F ratio is more than 2) showed higher sheet resistances compared to those formed on less carbon-rich residue (C/F ratio: 1.0–1.3). The difference between the previous work and the current experiment appears to be related to the C–Si bonding and the different C/F ratio studied. In the previous work, magnetized inductively coupled plasmas (MICP) were used to etch the PSG, therefore, the remaining residues showed C/F ratios lower than 1 (0.73–1), no C-Si bonding was observed. However, for the current experiment, helicon-wave plasmas were used to etch the PSG, and the C/F ratios of the residues were higher than 1 (1.0–2.2) and many C–Si bondings were also observed.

To compare the effect of the metal employed on the formation of stable silicides, Ti silicide was also formed on the above etched, cleaned, and annealed silicon wafers, and the results are shown in Fig. 4(b). The sheet resistances were higher for silicides formed on silicon wafers etched with hydrogen-containing plasmas and at higher bias voltage. In addition, the sheet resistances decreased as the etched wafers were cleaned and annealed. When annealing at 600°C after O_2 plasma cleaning was performed, the sheet resistance was close to that of the control. These results were similar to those for Co silicides, therefore, in the case of Co and Ti silicides, rather than damage or thickness, the characteristics of the residue were more closely related to the formation of stable silicides.

4. Conclusions

In this study, 1-μm-thick PSG-deposited silicon wafers were 50% overetched to expose the silicon surface with C_4F_8/H_2 helicon plasmas, under different dc self-bias voltages, and the characteristics of the residue and the degree of damage formed on the exposed silicon wafers were investigated. In particular, the effects of the residue characteristics and the damage remaining on the etched, cleaned, and annealed silicon wafers on the formation of a stable silicide were investigated. The thickness of the residue increased with the amount of a hydrogen added to the C_4F_8 plasma and with decreasing dc self-bias voltage, and the degree of damage increased with the amount of a hydrogen added to the plasma and increasing dc self-bias voltage.

The thickness of the residue decreased with Piranha cleaning, and further decreased to the control value after O_2 plasma cleaning followed by annealing at 600°C. The Co silicides formed on the variously etched, cleaned, and annealed silicon wafers exhibited different degrees of unstable Co silicidation, showing the formation of CoSi and Co_2Si compounds instead of stable $CoSi_2$, thinner Co silicides, and higher sheet resistances, when the residue remained on the silicon surfaces. The sheet resistance of silicides are dependent on the absolute thickness and C/F ratio of the residue. These characteristics of the residue are dependent on the etching conditions and cleaning conditions. The damage remaining on the etched silicon surface appears to not significantly affect the formation of stable silicides. When Ti silicides were formed on the etched, cleaned, and annealed silicon wafers, similar results to those for Co silicides were obtained.

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