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Etch-induced damage in single crystal Si trench etching by planar inductively coupled Cl_2/N_2 and Cl_2/HBr plasmas

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Abstract

In this study, 0.3–0.5 μm deep and 0.3 μm wide silicon trenches were etched using Cl_2/10%-N_2 and Cl_2/50%-HBr inductively coupled plasmas, the physical and electrical defects remaining on the etched silicon trench surfaces and the effects of various annealing and oxidation on the removal of the defects were studied. High resolution transmission electron microscopy and capacitance–voltage techniques were used to investigate the physical and electrical defects, respectively. Physical defects were found on the silicon trench surfaces etched in both Cl_2/10%-N_2 and Cl_2/50%-HBr. The most dense defects were found near the trench bottom edge, lesser dense defects were found at the trench bottom, and the least dense defects were found at the trench sidewall. The silicon etched in Cl_2/50%-HBr showed more physical defects compared to that etched in Cl_2/10%-N_2. Thermal oxidation of 20 nm at temperatures up to 1100°C alone appears not to remove the defects formed on the etched silicon trenches for both of the etch conditions. To remove the defects, an annealing at temperatures higher than 1000°C in N_2 for 30 min appears to be required.

Keywords: Shallow trench isolation; ICP; Etching; Damage

1. Introduction

Shallow trench isolation (STI) is a promising key technology for the deep submicron device isolation of silicon integrated circuits which replaces conventional local oxidation of silicon (LOCOS) type of isolations [1–5].

Currently, chlorine and bromine-based plasmas are widely studied in trench etch processes from the experience of the anisotropic etching of highly doped gate polysilicon [6,7]. However, the most studies are concentrated on controlling etch profiles and the selectivity while maintaining the etch uniformity, and the effects of these gas combination on the remaining defects during the shallow trench etch processes are not well investigated.

The purpose of this work is to identify the defects on the submicron silicon trenches etched using Cl_2/N_2 and Cl_2/HBr plasmas, and also to study the effects of the following oxidation or annealing processes on the removal of the defects. By distinguishing the effects of gas combinations on the defects and the degree of removal of them by the following processes, better control of the shallow trench isolation processes could be obtained.

2. Experiment

The inductively coupled plasma equipment used in the experiment can be found elsewhere [8]. Silicon wafers were patterned with 100 Å pad oxide / 2,000 Å nitride having 0.3–0.8 μm linewidths and 0.3–0.5 μm deep trenches were etched as a function of gas combination at − 100 V of bias voltage, 400 W of 13.56 MHz inductively coupled power, and 10 mTorr of operational pressure.

The defects formed on the etched silicon trenches were observed using high resolution transmission electron microscopy (HRTEM; JEOL JEM 2000 EX). The annealing processes were performed in N_2 from 600 to 1100°C for 30 min and the oxidation processes in O_2 from 900 to 1100°C for the time to form 200 Å-thick SiO_2 on the silicon trench were also implemented. Remaining physical defects on the sidewalls, bottoms, and corners of the annealed/oxidized silicon trenches were also observed using HRTEM.

To measure the electrical properties of the etched and annealed silicon surfaces, Au Schottky diodes were made on the blank etched and annealed silicon surfaces and their capacitance–voltage (*C–V*) characteristics were evaluated.

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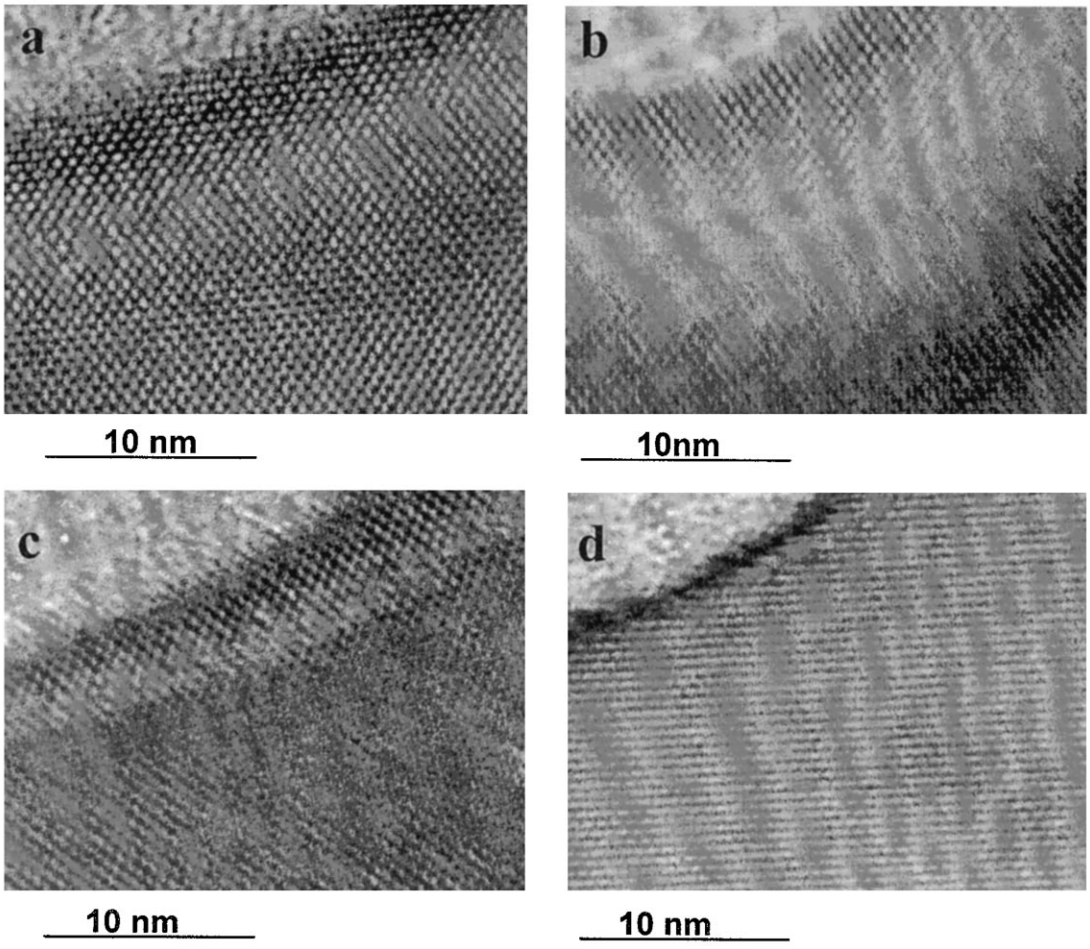

Fig. 1. High resolution TEM micrographs of the bottom edge region of 0.3 μm width silicon trenches (a) etched at 400 W, − 100 V, 10 mTorr and in Cl_2/10%-N_2, (b) Cl_2/50%-HBr, (c) oxidized after the etchings in Cl_2/10%-N_2 and (d) Cl_2/50%-HBr.

3. Results and discussion

Energetic ion bombardment during etch processes can generate physical and electrical damage on the plasma exposed surfaces. Especially for the silicon trench etch process, where there is no etch stop layer, therefore, the etched silicon trench surfaces are liable to suffer plasma damages during the etch processes. Fig. 1a,b shows HRTEM micrographs of the 500 nm-deep silicon trenches etched in Cl_2/10%-N_2 (etch rate: 280 nm/min) and in Cl_2/50%-HBr (etch rate: 300 nm/min) while other etch parameters are fixed at 400 W, 10 mTorr, and − 100 V. Only the bottom edge parts of the trenches are shown because when physical defects in the trenches were inspected, the largest number of defects were found near the trench bottom edge, and the smallest number at the trench sidewall. As shown in Fig. 1a,b, the silicon trench etched in Cl_2/10%-N_2 showed smaller number of physical defects compared to the trench etched at Cl_2/50%-HBr. The thickness of severe defects was 3–8 nm for the silicon trench etched at Cl_2/50%-HBr and that for Cl_2/10%-N_2 was 1.5–5 nm.

After the silicon trenches are etched, the trenches are generally oxidized to remove the possible defects formed on the trench surface during the etching and also to make trench corners round. Therefore, the shallow trench samples etched in the experiment were oxidized, and the effects of the oxidation on the removal of the defects formed during the etching were investigated. As seen in Fig. 1c,d, defects close to the surface were found for all of the etched trenches. The thickness of the defects were in the range from 2 to 4 nm, however, the thickness of defects remaining on the silicon trench etched in Cl_2/10%-N_2 appears to be thicker than those etched in Cl_2/50%-HBr. The thermal oxidation of 20 nm is supposed to remove about 10 nm of the silicon trench surface. Therefore, any defects located within the 10 nm depth from the silicon surface should be removed by the oxidation process, and the defects shown in the micrographs may be related to the oxidation process. However, because the thicknesses of defects found on the oxidized trench surfaces are different between the silicon trenches etched in different gas combinations, they could be also related to the defects formed during the etch processes. The thermal oxidation of 20 nm was also carried out at 1100°C (not shown), and the similar defects were found within 2 nm in

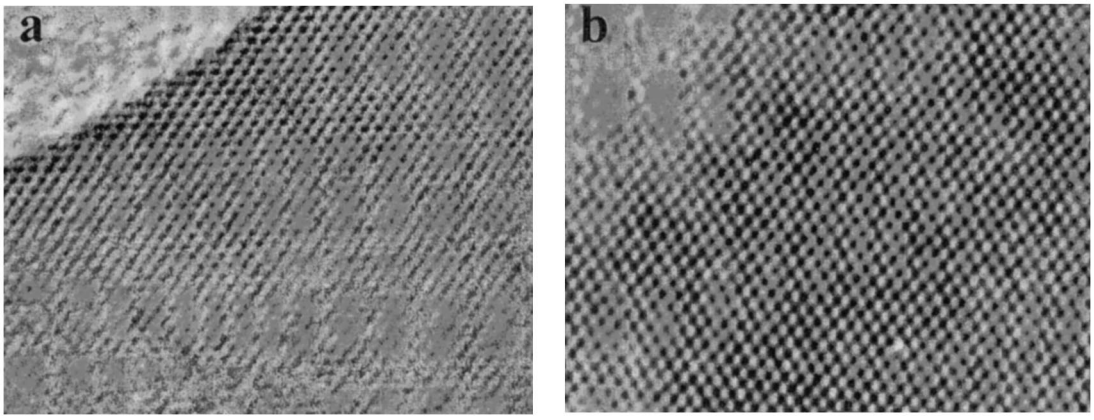

Fig. 2. High resolution TEM micrographs of the silicon trench bottom edges annealed in a furnace at 1000°C for 30 min in a nitrogen environment after the etchings in (a) Cl_2/10%-N_2 and (b) Cl_2/50%-HBr.

depth at the trench bottom and within 4 nm in depth at the trench bottom edge. Therefore, the thermal oxidation process growing 20 nm in thickness may not be able to remove the physical defects formed during the etching for both of the etch conditions used in the experiment.

To remove the defects formed during the etching, annealing processes can be followed before or after the trench surface oxidation. The annealings at 1000°C are shown in Fig. 2a for Cl_2/10%-N_2 and Fig. 2b for Cl_2/50%-HBr. The trench surface annealed at 1000°C after the silicon trench etching appeared to be dependent upon the gas combination used in the experiment. As shown in Fig. 2a,b, in case of the trench etched in Cl_2/10%-N_2, almost all of the defects were removed except for one or two atomic layers, where surface atoms appeared to be distorted. However, a clean and defectless trench surface was observed for the annealed trench surface etched at Cl_2/50%-HBr as shown in Fig. 2b. However, after the annealing up to 900°C, all of the trenches still showed some defects near the surface and more defects were found for the Cl_2/10%-N_2 case (not shown). The more reduction of damage through annealing processes compared to oxidation processes appears to be related to the shorter process time required for the oxidation of 20 nm at 900 and 1100°C.

The effects of the combination of the annealing process and the oxidation process on the removal of the defects formed during the etch processes were also investigated using HRTEM (not shown). When the trenches etched both in Cl_2/10%-N_2 and in Cl_2/50%-HBr were 20 nm-oxidized at 900°C in O_2 after the annealing at 900°C in N_2 for 30 min, a number of defects still remained near the trench surfaces, however, when the trenches were oxidized with the same condition after the annealing at 1000°C for 30 min, all of the defects appeared to be removed.

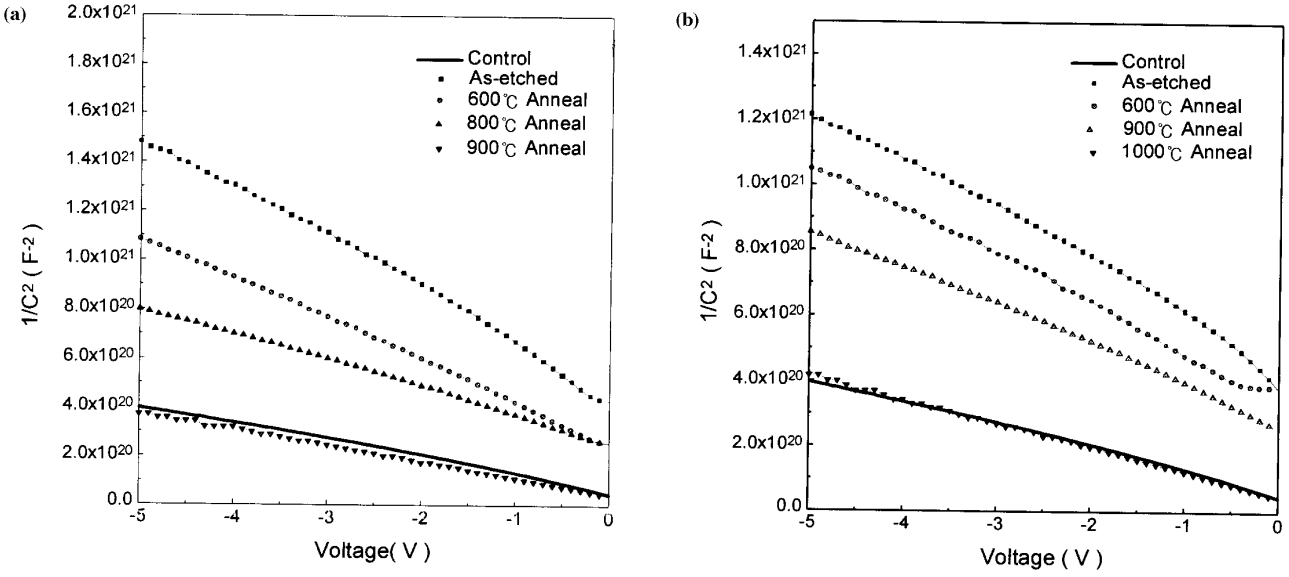

Fig. 3. The $1/C^2$–V characteristics of Schottky diodes fabricated on the silicon etched in (a) Cl_2/10%-N_2 and (b) Cl_2/50%-HBr and annealed at different temperatures.

To compare the physical defects observed above with electrical defects remaining on the etched and annealed silicon trenches, the *C–V* relations of the Schottky diodes fabricated on the blank silicon wafers, etched and annealed with the same conditions described above were measured and the results are shown in Fig. 3. The slope of $1/C^2$ vs. V of a Schottky diode is supposed to be proportional to the inverse of the doping concentration, therefore, proportional to the number of electrical defects [9,10]. Fig. 3a shows that the electrical defects on the silicon etched in Cl_2/10%-N_2 is reduced as the annealing temperature is increased and is close to the control sample (non-etched silicon) when the annealing temperature is increased to 900°C. Fig. 3b also shows that the electrical defects on the silicon etched in Cl_2/50%-HBr is removed when the annealing temperature is reached at 1000°C.

Therefore, the results on the electrical defects obtained using *C–V* appear to agree with the results of the physical defects observed using transmission electron microscopy except for some of the cases annealed at high temperatures. This exception might be from the different samples used in the experiment for the measurement of physical defects and electrical defects, that is, blank silicon samples instead of silicon trench samples were used to investigate electrical damage. However, from the measurements of electrical and physical defects, it could be concluded that the defects generated on the silicon trench surface during the silicon trench etching in our experimental conditions require an annealing process at least 1000°C in N_2 for 30 min to remove them completely.

4. Conclusions

Physical defects within the range of 10 nm in depth from the surface were found on the silicon trenches etched in Cl_2/10%-N_2 and more dense physical defects in Cl_2/50%-HBr when the silicon trenches were etched using inductively coupled plasmas in Cl_2/10%-N_2 and Cl_2/50%-HBr while other etch conditions such as the inductive power, bias voltage, operational pressure, and the etch depth were kept the same at 400 W, − 100 V, 10 mTorr, and 0.5 μm, respectively. All of the etched silicon trenches showed the most dense defects near the trench bottom edge area and the least dense defects at the trench sidewall area. A 20 nm thick thermal oxidation of the etched silicon trench at the temperature up to 1100°C alone appears not to remove the defects formed on the etched silicon trenches for both of the etch gas conditions even though the oxidation removed the 10 nm thick damaged silicon surface. However, the annealing at 1000°C for 30 min in N_2 appears to remove all of the defects for the silicon trenches etched in Cl_2/50%-HBr and most of the defects for the Cl_2/10%-N_2 etched silicon trenches.

Electrical defects measured by *C–V* of Schottky diodes showed the results similar to those of the physical defects obtained using transmission electron microscopy.

From the measurements of physical and electrical defects, an annealing process at least 1000°C in N_2 for 30 min appears to require the removal of the defects remaining on the silicon surface during the silicon trench etching.

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References

[1] B. Davari, C. Koburger, T. Furukawa, et al., IEDM Tech. Dig. 88 (1988).
[2] A. Chatterjee, J. Esquivel, S. Nag, et al., 1996 Symp. VLSI Technol. Dig. Tech. Pap., 156 (1996).
[3] J.Y. Cheng, T.F. Lei, T.S. Chao, Jpn. J. Appl. Phys. 36 (1996) 1319.
[4] H. Crazzolara, N. Gellrich, J. Electrochem. Soc. 137 (1990) 708.
[5] J. Maa, H. Gossenberger, L. Hammer, J. Vac. Sci. Technol. B 8 (1990) 581.
[6] M. Sato, Y. Arita, J. Electrochem. Soc. 134 (1987) 2856.
[7] S. Samukawa, M. Sasakai, Y. Suzuki, J. Vac. Sci. Technol. B 8 (1990) 1192.
[8] J.H. Lee, G.Y. Yeom, J.W. Lee, J.Y. Lee, J. Vac. Sci. Technol. A 15 (3) (1997) 573.
[9] O.S. Nakagawa, S. Ashok, J.F. Kruger, J. Appl. Phys. 69 (4) (1991) 2057.
[10] J.M. Heddleson, M.W. Horn, S.J. Fonash, J. Electrochem. Soc. 137 (1990) 1960.