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Influence of Ultra-Thin Ge_3N_4 Passivation Layer on Structural, Interfacial, and Electrical Properties of HfO_2/Ge Metal-Oxide–Semiconductor Devices

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We report the effects of the nitride passivation layer on the structural, electrical, and interfacial properties of Ge metal-oxide–semiconductor (MOS) devices with a hafnium oxide (HfO_2) gate dielectric layer deposited on *p*-type ⟨100⟩ Ge substrates. X-ray photoelectron spectroscopy analysis confirmed the chemical states and formation of HfO_2/Ge_3N_4 on Ge. The interfacial quality and thickness of the layers grown on Ge were confirmed by high-resolution transmission electron microscopy. In addition, the effects of post-deposition annealing (PDA) on the HfO_2/Ge_3N_4/Ge and HfO_2/Ge samples at 400 °C in an ($FG + O_2$) ambient atmosphere for 30 min were studied. After PDA, the HfO_2/Ge_3N_4/Ge MOS device showed a higher dielectric constant (k) of ∼21.48 and accumulation capacitance of 1.2 nF, smaller equivalent oxide thickness (EOT) of 1.2 nm, and lower interface trap density (D_{it}) of 4.9×10^{11} cm^{-2} eV^{-1} and oxide charges (Q_{eff}) of 7.8×10^{12} cm^{-2} than the non-annealed sample. The *I–V* analysis showed that the gate leakage current density of the HfO_2/Ge_3N_4/Ge sample (0.3–1 nA cm^{-2} at $V_g = 1$ V) was half of that of the HfO_2/Ge sample. Moreover, the barrier heights of the samples were extracted from the Fowler–Nordheim plots. These results indicated that nitride passivation is crucial to improving the structural, interfacial, and electrical properties of Ge-based MOS devices.

Keywords: Ge_3N_4/HfO_2 Gate Stacks, XPS, PDA, Interfacial Properties, F–N Mechanism, Ge MOS Devices.

1. INTRODUCTION

To keep the momentum with belittling size and enhancing the speed of metal-oxide–semiconductor field-effect transistors (MOSFETs), Ge-based MOSFETs have fascinated much more attention. This is due to the exceptionally high carrier mobility, which not only improves the drive current of transistors but also forms a perfect channel for high-speed integrated circuits [1, 2]. However, Ge oxide is not suitable as a gate dielectric because of its volatile and water-soluble nature. In addition, Ge native oxide (GeO_2) exhibits poor physical and electrical characteristics [3, 4]. Moreover, direct deposition of high-k dielectric on Ge, gets degraded by unstable GeO_x that affects the performance of high-speed MOSFET devices [4]. Thus, minimizing the water-soluble GeO_x layer on the Ge surface is the major task during the deposition of high-k dielectric materials [5]. Many researchers have addressed

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these thermal and chemical stability issues by transforming GeO_x to Ge oxynitride through various surface passivation treatments [6, 7]. Different types of surface passivation techniques such as nitridation (Ge_xN_y, AlN, TaON, and GeO_xN_y), sulfur passivation, and silicon nitridation (SiN) have been employed to obtain a stable interface in oxide/Ge stacks [8–10]. Among these techniques, Ge nitridation (Ge_3N_4) in an ambient NH_3 atmosphere is mostly performed before the deposition of high-k dielectric materials on Ge substrates [4–9]. N_2 atoms penetrate the GeO_2 layer and form Ge_xN_y, passivating the Ge surface. This nitride layer on the Ge surface enhances the interface stability and protects the interface during thermal and wet treatments.

Among the various mono high-k dielectric materials, HfO_2 possesses excellent thermal stability on the Ge surface, and it is extensively studied as a gate dielectric material in the CMOS technology [11]. This is due to its high dielectric constant (~25), large band gap energy (~5.8 eV), and promising properties for Ge MOS devices with physical thickness scaled down to a few nanometers [12]. Atomic layer deposition (ALD) is a prominent method for HfO_2 deposition because the following advantages: high accuracy and high uniformity of film thickness [13]. Post-deposition annealing is imperative to accomplishing high-performance MOS devices [14]. To improve the interface quality without adversely affecting the other properties, such as EOT and D_{it}, it is vital to choose an appropriate annealing temperature and annealing ambience. A Cr–Au electrode is used as the top-gate electrode, wherein Cr is used as a linkage layer for Au. Reportedly, Au electrodes are chemically stable and easy to fabricate, and have a high work function [15].

Here, we report the structural, interfacial, and electrical properties of the HfO_2 gate dielectric deposited on Ge_3N_4/Ge and compare them with those of HfO_2/Ge. In this study, X-ray photoelectron spectroscopy (XPS) was used to analyze the chemical structure and chemical compositions of the samples. The microstructural and interfacial quality of the deposited films on Ge was studied using high-resolution transmission electron microscopy (HRTEM). Further, we investigated the effect of post-deposition annealing in an ($FG + O_2$) atmosphere on the structural, electrical, and interfacial properties of the HfO_2/Ge_3N_4/Ge and HfO_2/Ge samples. The HfO_2/Ge_3N_4/Ge sample showed improved structural, interfacial, and electrical properties as compared with the HfO_2/Ge sample.

2. EXPERIMENTAL DETAILS

Two-inch p-type Ge ⟨100⟩ substrates with resistivity 0.01–0.1 Ω cm were used in this study. HfO_2 was used as the gate dielectric layer. Before deposition of the gate dielectric, the Ge wafers were cleaned with acetone, ethanol, and trichloroethylene for 1 min each, and then rinsed with deionized (DI) water several times. Subsequently, the wafers were immersed into dilute HF (1:50 volume ratio) for 10 s, rinsed with DI water five times each for 10 s, and finally, dried with N_2 gas. After cleaning, the substrates were loaded into a rapid thermal processing (RTP) chamber for the *in situ* growth of interfacial germanium nitride (Ge_3N_4) layer. The nitridation was carried out at 475 °C for 90 s in an NH_3 ambient. The formation of an ~0.67-nm-thick Ge_3N_4 layer was confirmed by microstructure and chemical composition analyses. Here after, devices subjected to RTP are referred to as passivated devices, and the other devices (not subjected to RTP) are referred to as non-passivated devices. Next, the passivated and non-passivated Ge samples were loaded into the atomic layer deposition (ALD) chamber to deposit a 6-nm-thick HfO_2 gate dielectric. Post-deposition annealing was carried on the passivated and non-passivated Ge devices at 400 °C in an ($FG + O_2$) atmosphere for 30 min each. A Cr–Au top electrode was deposited using a four-target electron-beam evaporation method, followed by Liftoff lithography. A back-contact Al electrode with thickness 50 nm was done after removing the native oxide by wiping with 5:1 buffered HF using the thermal evaporation process.

XPS was performed to confirm the chemical composition and structure of the samples. The microstructure and surface interface quality was studied using the HRTEM images. The capacitance–voltage (C–V) and conductance–voltage (G–V) characteristics at 1 MHz as well as current–voltage (I–V) characteristics were measured at room temperature using a Keithley 4200-SCS precision LCR meter. The oxide capacitance, equivalent oxide thickness (EOT), flatband voltage (V_{FB}), interface trap density (D_{it}), oxide charge (Q_{eff}), and barrier height (Φ_B) values were extracted from the C–V, G–V, and I–V curves.

3. RESULTS AND DISCUSSION

3.1. XPS Studies

The composition and chemical states of the HfO_2/Ge_3N_4/Ge sample were analyzed by XPS. The spectra in Figure 1(a) confirm the deposition of the nitride layer over the Ge surface. The peaks at 29.28 eV and 31.54 eV are assigned to bulk Ge and Ge_3N_4, respectively [9, 10]. After annealing, more nitrogen oxide was incorporated into the Ge surface, resulting in the Ge_3N_4 peak shift towards lower binding energy levels [16]. The Ge 3d doublet separation energy was determined to be $\Delta E = 2.28$ eV. From this result, we confirmed the formation of the nitride layer on the Ge surface during RTP in an NH_3 ambient. HfO_2 peaks were observed at 16.3 eV (Hf 4$f_{7/2}$) and 18.07 eV (Hf 4$f_{5/2}$), as shown in Figure 1(b). The spin-orbit splitting energy was found to be 1.68 eV, confirming the complete oxidation of hafnium oxide [17]. Figure 1(c) shows the N 1s peaks convoluted at 397.75 eV and 380 eV, which correspond to the as-deposited and annealed nitride layer on the Ge substrate

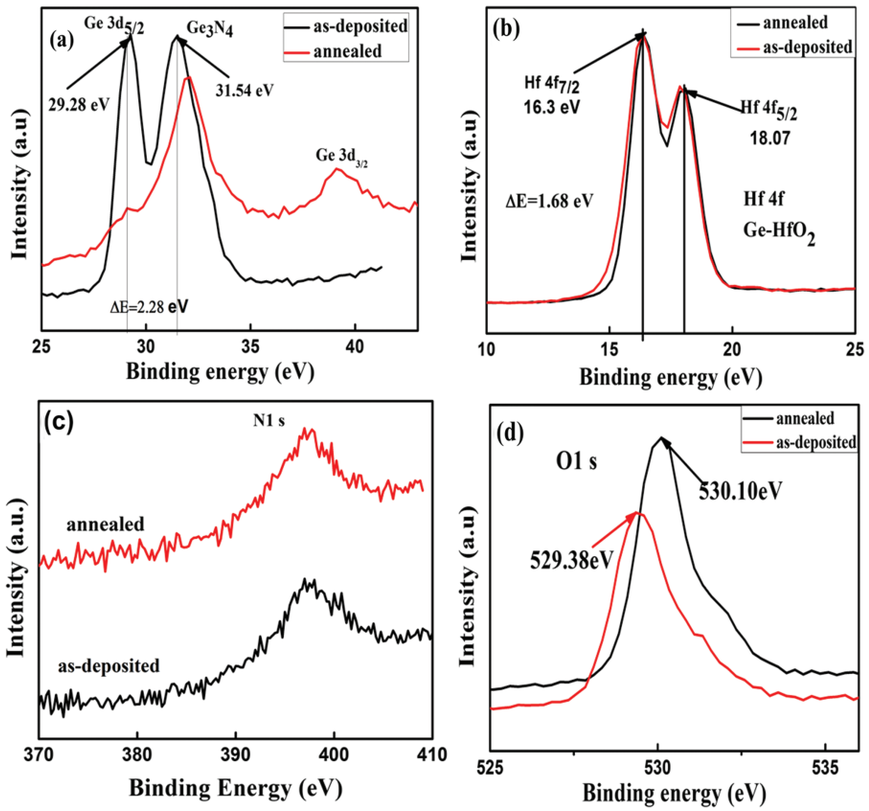

Figure 1. Core-level binding energy spectra of (a) Ge, (b) HfO_2, (c) N_2, (d) O_2.

after RTP. A small shift 0.3 eV in the annealed nitride layer, the possible reason for introducing N atoms is to prevent the formation of GeO_2 during oxygen diffusion at the interface [18]. This implies that the nitride layer is incorporated into the Ge substrate. Figure 1(d) shows the O 1*s* spectra of the as-deposited and annealed samples; the peaks assigned to the O–Hf bond in the ALD-deposited HfO_2 films were convoluted at 530 eV [19].

3.2. HRTEM Studies

Figure 2 shows the cross-sectional HRTEM images of the passivated and non-passivated HfO_2/Ge MOS devices after the PDA treatment. The figure clearly shows an ~0.67-nm Ge_3N_4 interfacial layer (IL) and the sharp and smooth interface between the HfO_2 gate dielectric and Ge substrate in the HfO_2/Ge_3N_4/Ge sample after the NH_3 pre-treatment, as indicated by the XPS results. No IL layer was formed between HfO_2 and Ge after PDA at 400 °C. This implies that the Ge_3N_4 layer might have effectively prevented the diffusion of Ge atoms to from the unstable low-*k* IL during PDA, improving the quality of the HfO_2/Ge interface. In addition, the HRTEM image of the non-passivated sample as shown in Figure 2(b) shows an

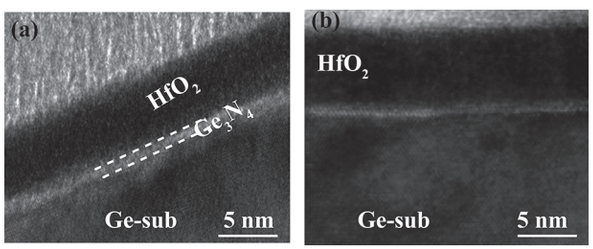

Figure 2. Cross-sectional HR-TEM images of annealed (a) passivated and (b) non-passivated HfO_2/Ge MOS devices.

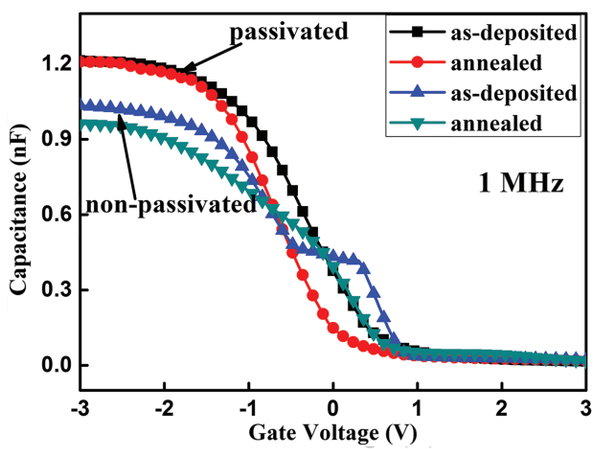

Figure 3. *C–V* characteristics of passivated and non-passivated HfO_2/Ge MOS devices.

Table I. Comparison of IL properties of passivated Au/Cr/HfO_2/Ge_3N_4/Ge and non-passivated Au/Cr/HfO_2/Ge MOS capacitors.

IL-properties	Passivated		Non-passivated	
Sample	As-deposited	Annealed	As-deposited	Annealed
K-value	20.69	21.48	15	16
EOT (nm)	1.5	1.2	1.9	1.5
D_{it} (cm^{-2} eV^{-1})	1.9×10^{12}	4.9×10^{11}	7.67×10^{12}	1.9×10^{12}
Q_{eff} (cm^{-2})	7×10^{12}	7.8×10^{12}	9.05×10^{12}	7.1×10^{12}
Φ_B (eV)	0.61	0.64	0.53	0.57

~1 nm non-uniform IL formed between the HfO_2 gate dielectric and Ge substrate in the HfO_2/Ge sample after the PDA treatment; the presence of the IL could be attributed to the direct deposition of gate dielectric (HfO_2) on Ge. The grown layer attributes to be Hf-GeO_x because the chemical reaction between HfO_2 and Ge substrate temperature at 400 °C [20, 21]. The diffusion of Ge atoms into HfO_2 led to the formation of Hf-GeO_x; the formation of the undesirable low-k IL between HfO_2 and the Ge substrate could degrade the electrical parameters of the MOS devices.

3.3. Electrical Property Measurements

To understanding the effect of the nitride passivation layer and PDA in an ($FG + O_2$) ambient at 400 °C, we fabricated Au/Cr/HfO_2/Ge_3N_4/Ge and Au/Cr/HfO_2/Ge MOS capacitors. Figure 3 shows the C–V characteristics of the passivated and non-passivated HfO_2/Ge MOS devices. The passivated HfO_2/Ge samples showed significantly higher accumulation capacitance (1.2 nF), smaller EOT (1.2 nm), and clear accumulation, depletion and inversion regions as compared with the non-passivated samples. These results for the passivated HfO_2/Ge_3N_4/Ge samples could be attributed to the presence of a smooth and stable nitride IL between HfO_2 and Ge. This resulted, suppressed the formation of defective low-k IL between HfO_2 and Ge, and effectively blocked the HfO_2 in-diffusion of oxygen and out-diffusion of Ge substrate [20, 21]. Moreover, the non-passivated HfO_2/Ge devices showed small accumulation capacitance (1 nF) and large EOT (1.5 nm); in addition, there were many bumps and stretches in the depletion and inversion regions. This could be attributed to the large interface trap densities between HfO_2 and Ge in the non-passivated samples, which was a possible reason for the formation of an unstable low-k IL between HfO_2 and Ge. It causes due to the out-diffusion of Ge atoms into in diffusion of the HfO_2 layer appears a defective Hf-GeO_x IL between HfO_2/Ge of the non-passivated devices [22, 23]. Moreover, the slope of the curve for the passivated sample was very clear and long, and there were no bumps and stretches in the depletion and inversion region, indicating a small D_{it} and strong interface between HfO_2 and Ge in the passivated MOS devices. A negative shift in the V_{FB} value was observed in the C–V curves of the passivated and non-passivated devices. The negative shift implied positive ionic charges (Q_{eff}) at the HfO_2/Ge interfaces in the passivated and non-passivated devices [24, 25]. The oxide charge (Q_{eff}) values of the passivated and non-passivated HfO_2/Ge devices were calculated using the following equation [26].

$$Q_{eff} = \frac{\Delta V_{FB} C_{ox}}{Q A_G} \quad (1)$$

Where Q is the charge of electron, A_G is the area of the gate, C_{ox} is the oxide capacitance, and ΔV_{FB} is the flat band voltage. The Q_{eff} values for the as-deposited and annealed passivated devices were determined to be 7×10^{12} cm^{-2} and 7.8×10^{12} cm^{-2} and those for the non-passivated devices were found to be 9.05×10^{12} cm^{-2} and 7.1×10^{12} cm^{-2}, respectively. The as-deposited and annealed passivated devices showed high-dielectric constant values as compared with the non-passivated devices (Table I). After PDA treatment, the passivated device exhibited an improved dielectric constant (k), indicating that the Ge_3N_4 IL layer enabled a good interfacial contact between HfO_2 and the Ge substrate, in agreement with the HRTEM results.

Figure 4 shows the G–V characteristics of the passivated and non-passivated HfO_2/Ge devices at a high frequency

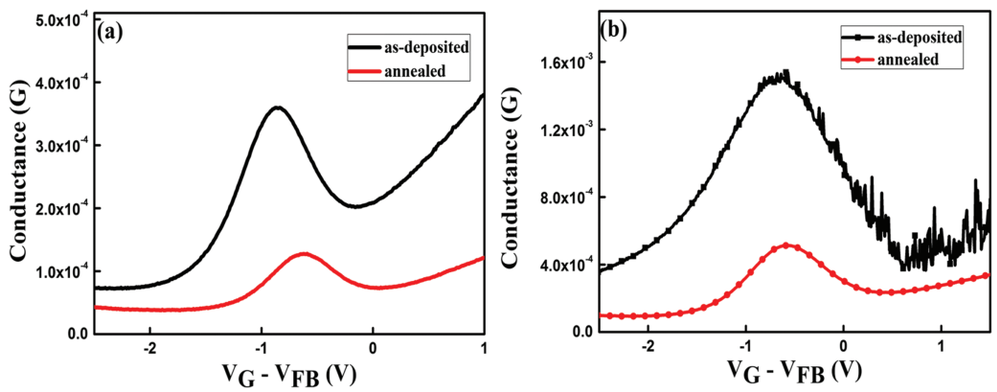

Figure 4. G–V characteristics (a) passivated (b) non-passivated HfO_2/Ge MOS devices.

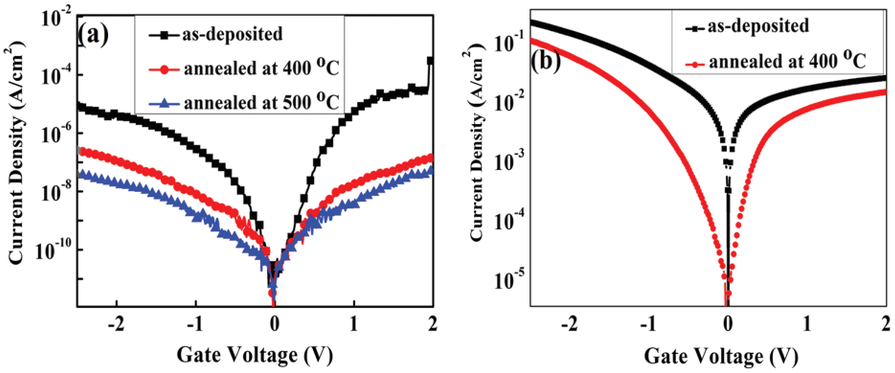

Figure 5. *I–V* characteristics of (a) passivated and (b) non-passivated HfO_2/Ge MOS devices.

of 1 MHz. The D_{it} values were determined by the high-frequency conductance method [27, 28], according to following equation.

$$D_{it} = \frac{2.5(G_p/\omega)\max}{qA_G} \tag{2}$$

Where q is the elemental charge and A_G is the gate electrode area and

$$\left(\frac{G_p}{\omega}\right) = \frac{\omega G_p C_{ox}^2}{C^2 m + \omega^2 (C_{ox} - C_m)^2} \tag{3}$$

Where G_p and C_m are the peak losses corresponding to the G–V and C–V curves, and ω is the angular frequency; the D_{it} values of the passivated devices were found to be $\sim 1.9 \times 10^{12}$ cm^{-2} eV^{-1} and $\sim 4.9 \times 10^{11}$ cm^{-2} eV^{-1} before and after annealing, respectively, and those of the non-passivated devices were determined to be $\sim 7.6 \times 10^{12}$ cm^{-2} eV^{-1} and $\sim 1.9 \times 10^{12}$ cm^{-2} eV^{-1} before and after annealing, respectively. As expected, the D_{it} values of the passivated devices were smaller as compared with those of the non-passivated samples, implying that the nitride passivation layer caused a significant improvement in the interface quality and decrease in the HfO_2/Ge interface trap densities in the MOS devices.

Figure 5 shows the *I–V* characteristics of the passivated and non-passivated HfO_2/Ge MOS devices. The gate leakage current densities (GLCDs) of the as-deposited passivated devices were determined to be in the range 0.5–1 μA cm^{-2} at $V_g = -1$ V and 0.05–0.08 mA cm^{-2} at $V_g = 1$ V, and the values for the annealed devices were found to be in the range 0.5–1 nA cm^{-2} at $V_g = -1$ V and 0.3–1 nA cm^{-2} at $V_g = 1$ V. On the other hand, for the as-deposited non-passivated devices, the GLCDs were in the range 10–15 mA cm^{-2} at $V_g = -0.5$ V and 1–5 mA cm^{-2} at $V_g = 1$ V; however, after annealing, the value decreased to 0.5–1 mA cm^{-2} at $V_g = -1$ V and 0.3–0.5 mA cm^{-2} at $V_g = 1$ V. Further, the passivated device annealed at 500 °C exhibited a GLCD lower than that of the sample annealed at 400 °C. As expected, the passivated devices showed leakage currents two orders of magnitude lower as compared with the non-passivated devices. This indicated that the rapid decrease in the leakage current density in both the as-deposited and annealed devices might be due to the presence of the intentionally grown nitride passivation layer between HfO_2 and the Ge substrate. Therefore, the nitride passivation layer on the Ge surface improved the quality of the interface between HfO_2 and Ge and reduced the gate leakage current. The Fowler–Nordheim

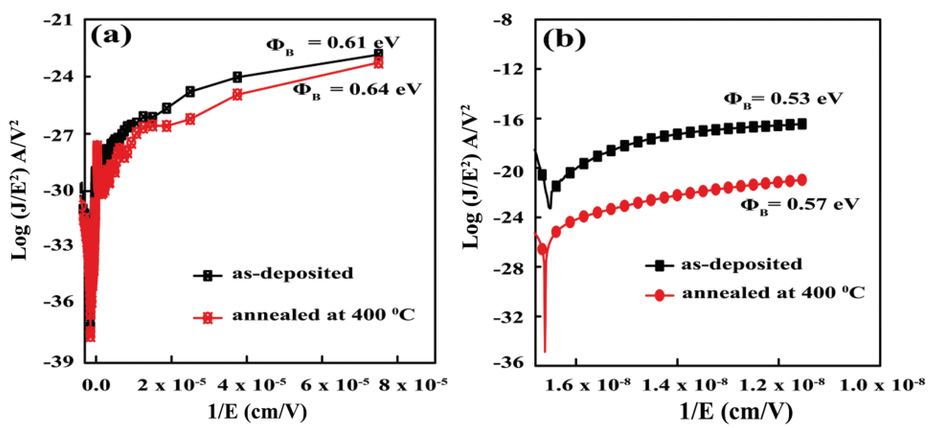

Figure 6. F–N plots or $\log(J/E^2)$ versus $1/E$ curves of (a) passivated and (b) non-passivated HfO_2/Ge MOS devices.

(F–N) plots obtained by plotting $\log(J/E^2)$ versus $1/E$ are shown in Figure 6. From these curves, we extracted the value of Φ_B between the gate dielectric (HfO_2) and substrate material (Ge) of the sample using the following equation [29, 30]

$$J_{FN} = AE^2 \exp(-B/E) \tag{4}$$

Where

$$A = \frac{q^3 m_c}{(8\pi h/2\pi)} \tag{5}$$

And

$$B = \frac{4(2m)^2 \emptyset B^{3/2}}{(3qh/2\pi)} \tag{6}$$

Where m_e is the HfO_2 effective mass of electron in the free space, which is equal to 0.1 [31] and Φ_B is the potential barrier height between the oxide and semiconductor material. The barrier heights were calculated from the slope of the liner region of the $\log(J/E^2)$ versus $1/E$ plots. The calculated barrier heights of the as-deposited and annealed passivated devices were found to be 0.61 eV and 0.64 eV, respectively. The obtained values were similar than those reported by Agrawal et al. [31] Moreover, the Φ_B values for the non-passivated samples were 0.53 eV and 0.57 eV before and after annealing, respectively; these values were higher than those reported by the same authors. After the PDA treatment at 400 °C, the Φ_B values of the passivated and non-passivated samples increased to 0.64 eV and 0.57 eV, implying a reduction in D_{it} and improvement in the HfO_2/Ge interface quality.

4. CONCLUSIONS

In summary, we have investigated the structural, interfacial, and electrical properties of ALD-deposited 6-nm HfO_2 films deposited on Ge with and without NH_3 plasma pre-treatments. The XPS analysis confirmed the formation of the HfO_2 and Ge_3N_4 layers on Ge. From the HRTEM images clearly shows, the micro-structural and interfacial thickness of HfO_2 and Ge_3N_4 layers over the Ge. The nitrided HfO_2/Ge_3N_4/Ge devices exhibited enhanced structural, interfacial, and electrical characteristics compared with the non-passivated HfO_2/Ge samples, as shown in Table I. After PDA in an $(FG+O_2)$ ambient at 400 °C, the passivated samples showed improved D_{it}, Q_{eff}, and dielectric constant values. Moreover, from the I–V measurements, the GLCD of the passivated device was determined to be in the range 0.3–1 nA cm^{-2} at $V_g = 1$ V, which was two times lower than that of the non-passivated sample. This study shows that nitride passivation and PDA in an $(FG+O_2)$ ambient are the major techniques to improving the structural, electrical, and interfacial properties of Ge-based MOS devices.

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