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Effects of post deposition annealing atmosphere on interfacial and electrical properties of HfO_2/Ge_3N_4 gate stacks

Kumar Mallem[a,1], Jagadeesh Chandra S.V.[b,*], Minkyu Ju[a,1], Subhajit Dutta[a], Swagata Phanchanan[a], Simpy Sanyal[a], Duy Phong Pham[a], Shahzada Qamar Hussain[a], Youngkuk Kim[a], Jinjoo Park[a], Young-Hyun Cho[a], Eun-Chel Cho[a,*], Junsin Yi[a,*]

[a] College of Information and Communication Engineering, Sungkyunkwan University, Suwon 16419, Republic of Korea
[b] Department of Electronics and Communication Engineering, Lakireddy Bali Reddy College of Engineering, Mylavaram 521 230, Andhra Pradesh, India

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ABSTRACT

Effects of post deposition annealing (PDA) atmosphere, including oxygen (O_2) gas and forming gas (FG), on interfacial and electrical properties of a HfO_2 gate dielectric on nitrided Ge are analyzed. Experiments to study the dielectric morphology, interface quality, and chemical composition of HfO_2/Ge_3N_4/Ge devices were carried out using X-ray diffraction, high-resolution transmission electron microscopy (HRTEM) imaging, and X-ray photoelectron spectroscopy (XPS) measurements, respectively. The XPS study confirmed that O_2 PDA effectively improves the HfO_2 film stoichiometry, and the stability of the interface between HfO_2/Ge_3N_4/Ge stacks is enhanced. Further, HRTEM images showed that the interface between HfO_2/Ge_3N_4/Ge stacks for O_2-annealed devices was smooth, uniform, and flat. The experimental results for devices annealed in O_2 at 500 °C exhibited improved interfacial and electrical characteristics, such as a high dielectric constant of ~19.50; high capacitance, 1.24 nF, low equivalent oxide thickness, 1.74 nm; interface trap density, $2.18 \times 10^{11}\,cm^{-2}\,eV^{-1}$; oxide charges, $2.50 \times 10^{12}\,cm^{-2}$; and gate leakage currents in the order nA of 0.5×10^{-9} A/cm^2 as compared with FG annealing devices. The Fowler−Nordheim tunneling current conduction mechanism was also verified. Therefore, these results are evidence that the O_2 PDA process improves the interfacial and electrical properties of HfO_2/Ge_3N_4/Ge metal-oxide-semiconductor (MOS) devices as compared with FG annealing, which is important for future Ge-based complementary MOS device performance and reliability.

1. Introduction

To maintain pace with the downscaling and speed enhancement of metal-oxide-semiconductor field-effect-transistors (MOSFETs), Ge-based MOSFETs are being developed. These devices are of interest owing to the high electron–hole mobility, small energy band gap, and low dopant activation energy of Ge as compared with Si [1–3]. However, naturally grown GeO_2 is not stable like a SiO_2 layer on Si [1]. GeO_2 degrades the physical and electrical properties of the devices owing to its thermal instability at 450 °C, the easy formation of volatile GeO at low temperatures (e.g., 400 °C), and its water-soluble nature [4–6]. Moreover, direct deposition of high dielectric material on Ge surfaces results in poor interface quality, high interface trap densities (D_{it}), and high gate leakage currents [6]. To overcome this problem, a number of techniques have been proposed to passivate the germanium oxide to germanium oxynitride (Ge_3N_4, GeO_xN_y) before depositing a high-k dielectric on the Ge surface [7–10]. The nitridation of Ge surfaces by rapid thermal annealing (RTA) with an NH_3 atmosphere has helped the interface between high-k dielectric films and the Ge substrate achieve superior quality [11]. However, HfO_2 is an extensively studied dielectric material used in modern CMOS technology owing to its high value of k (25), wide bandgap, and good thermal stability over Ge for thicknesses of a few nanometers [12,13]. For better device fabrication, uniform deposition of HfO_2 is desired that can be prominently done by atomic layer deposition (ALD) technique, as compared with others, that results in a good interface quality [14].

Apart from the deposition techniques, post deposition annealing (PDA) in an appropriate atmosphere and temperature also plays an important role in improving the interface quality between the gate dielectric and the substrate material. This results in the reduction of D_{it},

* Corresponding authors at: 2066, Seobu-ro, Jangan-gu, Suwon-si, Gyeong gi-Do 16419, South Korea.
E-mail addresses: kumareceb7@skku.edu (K. Mallem), svjchandra@gmail.com (S.V. Jagadeesh Chandra), mkju@skku.edu (M. Ju), echo0211@skku.edu (E.-C. Cho), Junsin@skku.edu (J. Yi).
[1] Indicates equal contribution to this work.

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equivalent oxide thickness (EOT), and gate leakage current. Many researchers have reported the effects of PDA atmosphere on HfO_2/Ge_3N_4 gate stacks on Ge for various temperatures. Oshima et al. reported the effects of PDA atmosphere, including forming gas (FG), inert gas, and high vacuum annealing at 375 °C on plasma-nitrided Ge substrates with an HfO_2 gate dielectric [15]. Deng et al. observed low ($2 \times 10^{11}\ eV^{-1}$ and $4 \times 0^{11}\ eV^{-1}$) D_{it} and ($8.3 \times 10^{\wedge 11}\ cm^{-2}$ and $4.53 \times 10^{\wedge 12}\ cm^{-2}$) oxide charges ($Q_{eff}$) after PDA of HfO_2/Ge in oxygen (O_2) and FG at 350 °C. [16]. Chen et al. reported lower EOT and D_{it} and improved interfacial properties after PDA with O_2 gas at 550 °C for HfO_2 and Al_2O_3 on nitrided Ge [17]. Chandra et al. also reported that after O_2 PDA at 500 °C, HfO_2/Ge devices showed lower values of leakage currents and the interface between HfO_2 and Ge improved, as compared with FG-annealed devices [18].

In this paper, we report the effects of PDA in O_2 and FG on the interfacial and electrical properties of HfO_2/Ge_3N_4/Ge devices and compare their properties. High-resolution transmission electron microscopy (HR-TEM) images showed that the interface between the HfO_2/Ge_3N_4/Ge stacks for the O_2 PDA atmosphere was uniform and smooth. The annealing temperature increases in both devices, improving their electrical characteristics, such as D_{it}, Q_{eff}, and gate leakage currents, irrespective of the use of an O_2 or FG atmosphere. The O_2-annealed devices were found to improve faster as compared with the FG-annealed devices.

2. Experimental details

P-type <100> gallium-doped Ge substrates with a resistivity ranging from 0.01–0.1 Ω cm were used in this study. Each Ge wafer was cleaned with acetone, ethanol, and trichloroethylene for 1 min to remove any organic contamination. Substrates were then subjected to a 2% HF dip for 20 s, rinsed with DI water several times, and finally dried with N_2 gas. After cleaning, the Ge wafers were loaded into the rapid thermal annealing chamber to passivate the Ge surface with germanium nitride (Ge_3N_4). The nitridation was carried out at 575 °C in an NH_3 atmosphere for 85 s. Then, an 8 nm thick HfO_2 layer was deposited on the nitride passivated Ge samples using ALD at a substrate temperature of 200 °C for 80 cycles (NCD LUCIDA D100). Tetrakis (ethylmethylamino)-hafnium (TEMAH) and H_2O were used as the Hf precursor and oxidant source for HfO_2 deposition, respectively. Each ALD cycle consisted of a 0.2 s TEMAH pulse, 10 s N_2 purge, 0.2 s H_2O pulse, and 10 s N_2 purge. A flow rate of 50 sccm of pure (99.999%) N_2 gas was used as the purging and carrier gas. The HfO_2 growth rate and ALD chamber pressure were maintained constant during the deposition at about ~1 Å thickness per cycle and ~1.0 Torr, respectively. The PDA was carried out at 400, 450, and 500 °C in ambient O_2 gas and FG separately, each for 30 min. The thickness of the Ge_3N_4 layer was confirmed from the HR-TEM images and ellipsometry measurements. Chromium–gold metal was used as the gate electrode and was deposited on top of the HfO_2/Ge_3N_4/Ge by a 4-target E-beam thermal evaporator system followed by a liftoff-lithography process. The Al electrode was used as a back contact electrode deposited by a thermal evaporator system with a thickness of 50 nm.

The crystallinity of the gate dielectric HfO_2 was characterized by a Bruker D8 (Bruker XAS) advanced X-ray diffractometer. The X-ray diffraction (XRD) patterns were collected using Cu Kα monochromatic radiation source (λ = 1.54 Å) with an X-ray incident angle of 0.5°, 2θ scanning range from 20°–80°, step size of 0.1° per 1 s, and an operating voltage of 40 kV. The quality of the interface and thickness of the HfO_2/Ge_3N_4 layers over an Ge substrate were confirmed from the HR-TEM images that were captured using the JEM 2010F (JEOL) model in the resolution range from 5 to 50 nm at an operating voltage of 200 kV. Further, the sample was prepared by Ar ion milling. The chemical composition of the HfO_2/Ge_3N_4/Ge structure was confirmed using a PHI 5000 VersaProbe II (ULVAC PHI, Japan) XPS system, equipped with standard Al Kα monochromatic X-ray energy source

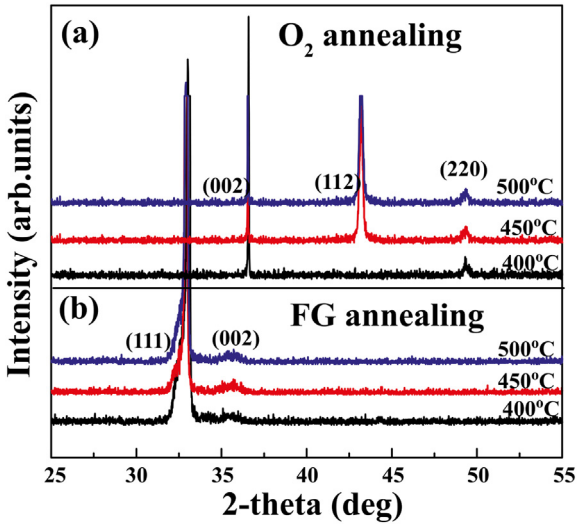

Fig. 1. XRD patterns of ALD-HfO_2 films annealed at 400, 450, and 500 °C in (a) O_2 and (b) FG, respectively.

($h\nu$=1486.6 eV) with an operating power of 48.93 W. The XPS data were collected at 45° angles with an Ar sputtering energy of 2.0 kV and sputter time of 2 min. The collected XPS binding energy spectra calibrated with the Ge $3d_{5/2}$ peak at 29.40 eV and spectral deconvolution was processed using the Gaussian–Lorentzian (G–L) function after smart-type background subtraction. For the peak fitting procedure, a list of references and published papers were referred to avoid arbitrary decisions. Capacitance–voltage (C–V) and conductance–voltage (G–V) curves of the HfO_2/Ge_3N_4/Ge devices were measured at a high frequency of 1 MHz using a Keithley VEGA 4200 LCR meter. The current–voltage (I–V) characteristics were also measured using the same meter.

3. Results and discussion

3.1. XRD results

To analyze the crystallinity and phase transition of HfO_2, PDA was carried out in O_2 gas and FG at 400, 450, and 500 °C for 30 min each. The samples obtained were characterized using XRD as shown in Fig. 1. As can be seen from the XRD results, the crystallinity increased with PDA temperature, and the phase transition rate also showed improvement for both O_2– and FG-annealed samples. As shown in Fig. 1(a), the O_2-annealed samples showed strong diffraction peaks at ~36° and ~43.21° attributed to the (002) and (211) planes, belonging to the monolithic and cubic phases of HfO_2, respectively [19,20]. In contrast, the FG-annealed sample in Fig. 1(b) showed only one diffraction peak centered at ~32° corresponding to the (111) plane, which represents the monolithic phase of HfO_2 [19,20]. The O_2-annealed samples showed monolithic, cubic, and a combination of weak cubic and tetragonal peaks, which suggest improved electrical properties of the gate dielectric, such as a higher k and lower D_{it} and leakage currents. Therefore, these results suggest that annealing in an O_2 atmosphere effectively improved the crystallinity of the HfO_2, as combinations of different diffraction peaks were observed, compared with FG annealing. This considerably improves the device performance.

3.2. HR-TEM

The interface quality of $HfO_2/Ge3N_4$ gate stacks on Ge was verified using cross-sectional HR-TEM images after PDA at 400 °C in both O_2 and FG atmospheres, as shown in Fig. 2. The HR-TEM images clearly show the formation of an 8 nm thick HfO_2 layer and a 0.8 nm thick

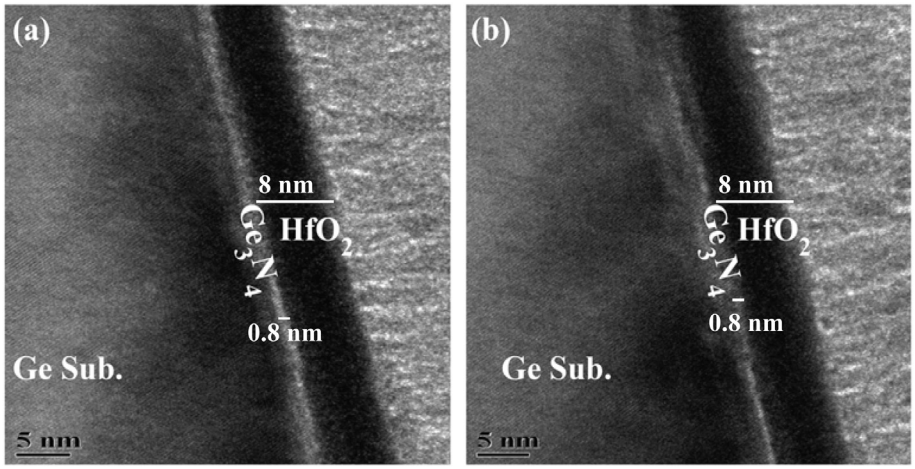

Fig. 2. Cross-sectional HR-TEM images of the $HfO_2/Ge_3N_4/Ge$ stacks annealed at 400 °C in (a) O_2 and (b) FG, respectively.

Ge_3N_4 (HfO_2/Ge_3N_4) bilayer structure on the Ge surface, the same layers as those suggested by the XPS results. The images clearly show that there is only a sharp and uniform thin interfacial layer (IL) of Ge_3N_4 between the HfO_2 layer and the Ge substrate and there is no other IL in the $HfO_2/Ge_3N_4/Ge$ stacks. In Fig. 2(a), the O_2-annealed devices show a smooth and uniform interface between the gate dielectric and the substrate material, as compared with the FG-annealed devices shown in Fig. 2(b). The formation of a thin Ge_3N_4 layer between HfO_2 and the Ge substrate enhances the interface stability between HfO_2 and Ge and improves the structural and electrical properties of the HfO_2/Ge MOS devices.

3.3. XPS

The XPS analysis was performed to confirm the chemical composition of the HfO_2/Ge_3N_4 layers formed on the Ge substrate. Fig. 3 demonstrates a comparison of XPS core level binding energy spectra of Ge 3d, Hf 4f, O 1 s, and N 1 s for $HfO_2/Ge_3N_4/Ge$ stacks after PDA at 400, 450, and 500 °C in O_2 and FG atmospheres, respectively. The Ge 3d spectra for O_2-annealed devices are shown in Fig. 3(a). The bulk Ge peak was observed at 29.40, 29.50, and 29.52 eV, while the corresponding nitride peak could be seen at 32.26, 31.98, and 31.94 eV after PDA at 400, 450, and 500 °C in O_2, respectively [15,21,22]. The sub peak splitting energies of the Ge 3d peak were found to be 2.86, 2.48, and 2.42 eV, which confirms the different oxidation states of the Ge [23,24]. As the PDA temperature increased, a peak shift toward lower binding energies was observed. This implies the densification of nitrogen atoms and their incorporation into the oxide layer that converts the oxide layer to an oxynitride layer [21,22,25]. Fig. 3(b) shows the Ge 3d spectra for the FG-annealed devices. The peaks observed at

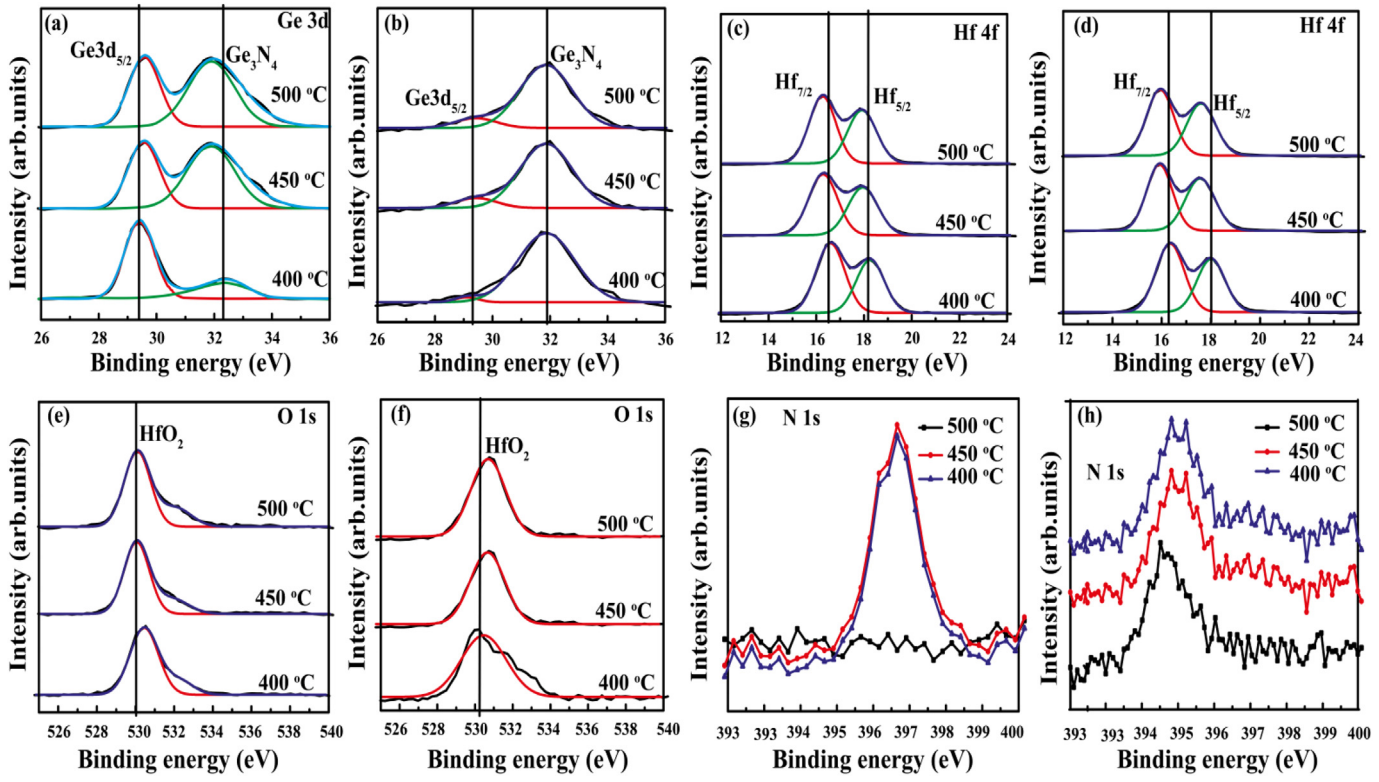

Fig. 3. XPS core level binding energy spectra of: Ge3d (a) after PDA in O_2 and (b) FG atmosphere, Hf4f (c) in O_2 and (d) FG, O 1 s (e) in O_2 and (f) FG, and N 1 s (g) in O_2 and (h) FG at 400, 450, and 500 °C.

29.29, 29.52, and 29.54 eV represent bulk Ge, and the peaks at 31.92, 31.94, and 31.97 eV represent the formation of Ge_3N_4 after PDA at 400, 450, and 500 °C in FG, respectively. The sub peak splitting energies of the Ge 3d peak were found to be 2.63, 2.44, and 2.42 eV, which can be attributed to the oxidation states of the Ge [23,24]. Fig. 3(c) & (d) show the Hf 4f spectra for O_2– and FG-annealed samples. Peaks were observed at 16.36 and 18.12 eV, which correspond to $Hf_{7/2}$ and $Hf_{5/2}$, respectively. The spin orbit separation energy was 1.75 eV, which indicates the full oxidation of hafnium oxide [26]. For O_2 atmospheres, PDA at 450 and 500 °C resulted in a slight peak shift in the Hf 4f spectrum toward higher binding energies, which implies improvement in the stoichiometry and full oxidation behavior of the HfO_2 films [27]. These results provide evidence that the passivated nitride layer effectively blocks the formation of a defective Ge–O layer during the ALD-HfO_2 deposition and PDA process, in agreement with the HR-TEM images. The O 1 s spectra for O_2– and FG-annealed samples are shown in Fig. 3(e) & (f), respectively. The peak centered at 530 eV belongs to the ALD-HfO_2 film as a result of the O_2 plasma used during the reaction [15,16]. Fig. 3(g) & (h) show N 1 s spectra for the O_2– and FG-annealed samples. The peaks originating at 398 eV for O_2 and 394 eV for FG annealing confirm that nitrogen atoms were incorporated into the substrate material (Fig. 3(a) & (b)), which is in agreement with previous reports [15,16].

3.4. Electrical properties

To understand the effects of the PDA atmosphere on the interfacial and electrical properties of the multilayered gate dielectrics, the HfO_2/Ge_3N_4 on Ge stacks were analyzed in terms of their C–V, G–V, and I–V characteristics measured at a high frequency of 1 MHz at room temperature.

Fig. 4 shows the C–V characteristics of the HfO_2/Ge_3N_4/Ge MOS devices after PDA in O_2 and FG at 400, 450, and 500 °C measured at a frequency of 1 MHz. With increasing PDA temperature, the devices were observed to exhibit improved accumulation capacitance, k, and EOT values, irrespective of the annealing atmosphere. This implies that PDA recovers the D_{it} and improves the stability of the interface between HfO_2 and the Ge substrate. As shown in Fig. 4(a), the O_2-annealed devices exhibited clear accumulation, depletion, and inversion regions with no bumps or nicks in all three regions. In contrast, Fig. 4(b) shows that the FG-annealed devices exhibited low accumulation capacitance, and bumps and nicks in the depletion regions, which implies large D_{it} values and Q_{eff} between the HfO_2/Ge_3N_4/Ge layers. The k values of the HfO_2 were extracted from the accumulation region of the C–V plots and the values are 16.0, 19.19, and 19.50 for O_2 PDA at 400, 450, and 500 °C respectively. However, the FG-annealed devices had k values of 13.07, 14.74, and 15 for PDA at 400, 450, and 500 °C, respectively. The O_2-annealed devices exhibited high k values, in agreement with the XRD results. The amounts of trapped Q_{eff} between the HfO_2 layer and the Ge substrate were calculated using the following formula [28,29].

$$Q_{eff} = \frac{\Delta V_{FB}\, C_{0x}}{QA_G} \tag{1}$$

where Q is the charge of the electron, A_G is the area of the gate electrode, C_{ox} is the oxide capacitance, and ΔV_{FB} is the flat band voltage; the values are presented in Table 1. The flat band voltage shifted toward the negative region, which implies that a positive Q_{eff} is present between the HfO_2 layer and the Ge substrate [30] for both O_2– and FG-annealed devices. When the PDA temperature was increased, the flat band voltage shifted toward the positive region for both O_2– and FG-annealed devices. This confirms the improvement in gate stabilization and passivation of Ge dangling bonds. From the C–V results, the O_2 PDA devices exhibited high k values, high capacitance, and lower EOT and Q_{eff}; this implies that O_2 annealing is a promising method to improve the interfacial and electrical properties of the HfO_2/Ge MOS capacitors as compared with FG annealing.

Fig. 5 shows the G–V characteristics of the Au/Cr/HfO_2/Ge_3N_4/Ge MOS devices after PDA with O_2 gas and FG at 400, 450, and 500 °C measured at a frequency of 1 MHz. The D_{it} values were extracted from the capacitance–conductance–voltage characteristics using the following equation [31].

$$D_{it} = \frac{2\omega C_{0x}^2 G_{max}}{QA(G_{max}^2 + \omega^2 (C_{0x} - C_m G_{max})^2)} \tag{2}$$

where C_m and G_m are the maximum capacitance and conductance values, respectively, and ω is the frequency. The obtained D_{it} values for the O_2-annealed devices are 6.36×10^{11}, 4.88×10^{11}, and 2.18×10^{11} ($cm^{-2}\,eV^{-1}$) for PDA at 400, 450, and 500 °C, respectively. The values for the FG-annealed devices are 1.88×10^{12}, 2.50×10^{12}, and 2.20×10^{12} (cm^{-2}) at 400, 450, and 500 °C, respectively. However, the obtained D_{it} values are considerably low and in good agreement with those previously reported by Maeda et al. and Otani et al. [32,33]. The D_{it} values of the O_2-annealed devices were low and gradually decreased with increasing PDA temperature. This behavior indicated that the quality of the interface between HfO_2 and Ge was improving. This in turn demonstrates that O_2 annealing played a more effective role in the passivation of Ge dangling bonds as compared with FG annealing.

The I–V characteristics demonstrate the improvement in gate leakage current densities with the increase in PDA annealing temperatures for both O_2 gas and FG devices as shown in Fig. 6. It is clear that the O_2-annealed devices exhibited low gate leakage currents in the range of 1×0^{-7}, 1×0^{-8}, and 0.5×0^{-9} A/cm² at Vg = 1 V at 400, 450, and 500 °C, respectively. However, FG PDA devices showed gate leakage currents of 1×0^{-5}, 1×0^{-6}, and 1×0^{-8} A/cm² for Vg = 1 V

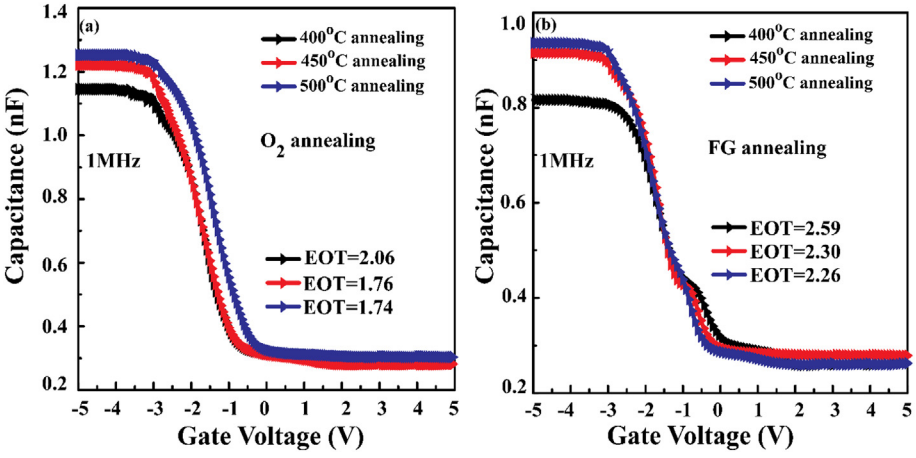

Fig. 4. C–V characteristics of the Au/Cr/HfO_2/Ge_3N_4/Ge MOS capacitors after PDA at 400, 450, and 500 °C in (a) O_2 and (b) FG, respectively.

Table 1
Interfacial properties of the $HfO_2/Ge_3N_4/Ge$ MOS devices after O_2 and FG PDA at 400, 450, and 500 °C.

IL properties	O_2 annealing				FG annealing			
Temperature	k	EOT (nm)	D_{it} ($cm^{-2}eV^{-1}$)	Q_{eff} (cm^{-2})	k	EOT (nm)	D_{it} ($cm^{-2}eV^{-1}$)	Q_{eff} (cm^{-2})
400 °C	16.0	2.06	6.36×10^{11}	7.63×10^{12}	13.07	2.59	1.88×10^{12}	1.60×10^{12}
450 °C	19.19	1.76	4.88×10^{11}	$2.9\,5 \times 10^{12}$	14.74	2.30	2.50×10^{12}	$2.50 \times 1\,0^{12}$
500 °C	19.50	1.74	2.18×10^{11}	2.50×10^{12}	15	2.26	2.20×10^{12}	2.85×10^{12}

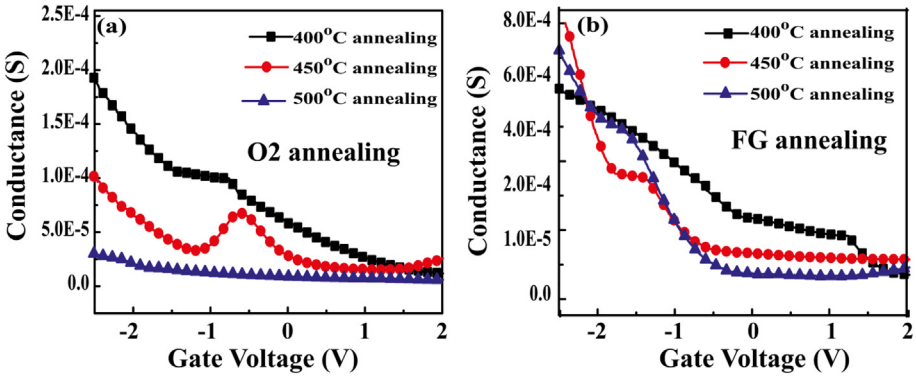

Fig. 5. G–V characteristics of the $Au/Cr/HfO_2/Ge_3N_4/Ge$ MOS capacitors after PDA at 400, 450, and 500 °C in (a) O_2 and (b) FG, respectively.

at 400, 450, and 500 °C, respectively. This implies that O_2 annealing played a key role in suppressing the high D_{it} in the gate dielectric and improving the quality of the interface between the gate dielectric and the substrate material. The leakage current densities in the range of nanoamperes imply low interface trap densities and a smooth dielectric interface with the large conduction-valance band offsets [34]. From the I–V results, O_2 annealing is a more effective method to improve the gate leakage currents of the $HfO_2/Ge_3N_4/Ge$ MOS device as compared with FG annealing.

The Fowler − Nordheim (F–N) current conduction mechanism was used to analyze the current transport and leakage current mechanism of the $Au/Cr/HfO_2/Ge_3N_4/Ge$ MOS devices as shown in Fig. 7. The F–N tunneling mechanism was verified by the following equation [35,36].

$$J = AE^2 \exp(-B/E) \tag{3}$$

where

$$A = \frac{q^3 m_e}{16\pi^2 \hbar m_{0x} \phi_0} \tag{4}$$

and

$$B = \frac{4}{3} \frac{(2m_{0x})^{1/2}}{q\hbar} \phi_0^{3/2} \tag{5}$$

where m_e is the HfO_2 effective mass of an electron that is equal to 0.1 in the free space [35] and ϕ_B is the potential barrier height between HfO_2 and the Ge substrate material. The ϕ_B calculated from the slope of the liner region of the ln (J/E^2) versus 1/E plot, which suggest F–N tunneling through the HfO_2 layer as shown in Fig. 7. From the slope of the liner region of the F–N plots, the obtained barrier heights of the devices subjected to O_2 PDA at 400, 450, and 500 °C of the devices are ϕ_B = 0.80 eV, 0.78 eV, and 0.75 eV, respectively. Meanwhile, the devices subjected to FG PDA devices exhibited ϕ_B = 0.89 eV, 0.87 eV and 0.86 eV at 400, 450, and 500 °C, respectively. For both O_2 and FG annealing, the ϕ_B values decreased as a function of increasing PDA temperature. The reason for the decrease in ϕ_B is the decrease in HfO_2 thickness and change in its stoichiometry as a function of increasing PDA temperature [37–40], which was discussed in relation to the XPS results. The obtained ϕ_B values are comparable with those previously reports of Kumar et al. and Agrawal [37,41].

4. Conclusion

In summary, the effects of O_2 and FG PDA on the interfacial and electrical properties of HfO_2 gate dielectrics on nitrided Ge were investigated and their properties were compared. The XRD results confirmed that the phase and crystallinity of the HfO_2 was improved for the devices annealed in the O_2 atmosphere. The dielectric interface quality and films composition of the $HfO_2/Ge_3N_4/Ge$ stacks were considerably

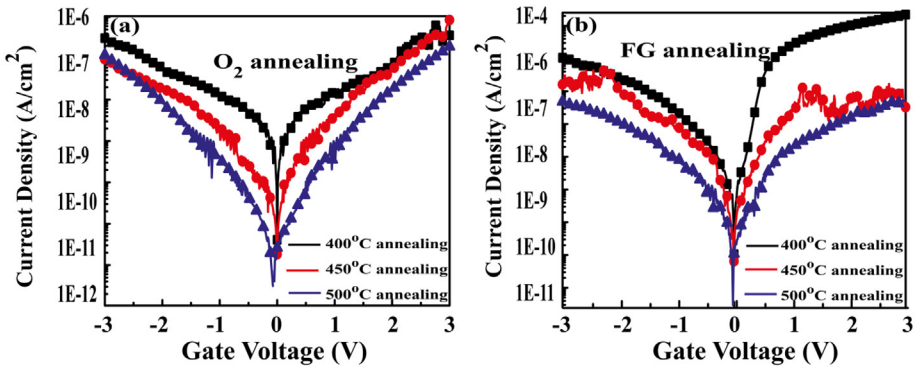

Fig. 6. I–V characteristics of the $Au/Cr/HfO_2/Ge_3N_4/Ge$ MOS devices after PDA at 400, 450, and 500 °C in (a) O_2 and (b) FG, respectively.

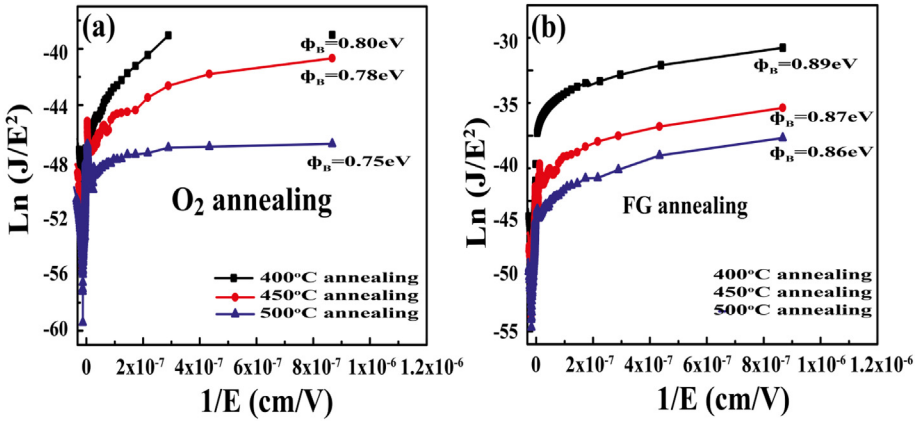

Fig. 7. Fowler – Nordheim (F – N) current conduction mechanism of Au/Cr/HfO_2/Ge_3N_4/Ge MOS devices after PDA at 400, 450, and 500 °C in (a) O_2 and (b) FG, respectively.

improved for the devices annealed in O_2 atmosphere as confirmed from the HR-TEM and XPS study, respectively. Considerable improvement was observed in the interfacial and electrical properties of the HfO_2/Ge_3N_4/Ge devices when the PDA temperatures were increased for both O_2 and FG atmospheres. A lower EOT of 1.7 nm; D_{it}, $2.18 \times 0^{11}\,cm^{-2}\,eV^{-1}$; Q_{eff}, $2.5 \times 0^{12}\,cm^{-2}$; and high k, 19.12 and capacitance, 1.2 nF with improved interfacial and electrical characteristics were exhibited by the O_2-annealed devices. This implies that the quality of the interface between HfO_2 and Ge improved more as compared with the FG annealing process. The gate leakage current densities of the O_2-annealed devices on the order of $0.5 \times 0^{-9}\,A/cm^{-2}$ were obtained at Vg = 1 V (nA). Therefore, these results indicate that O_2 PDA is a more promising method to improve the electrical and interfacial properties of HfO_2/Ge_3N_4/Ge MOS devices.

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