

PAPER

Effects of tunneling dielectrics formed by CO₂ and N₂O plasma-assisted oxidations on memory characteristics in p-channel LTPS NVM devices with ONO structure

To cite this article: Kyungsoo Jang *et al* 2018 *Semicond. Sci. Technol.* **33** 125004

View the [article online](#) for updates and enhancements.



IOP | ebooks™

Bringing you innovative digital publishing with leading voices to create your essential collection of books in STEM research.

Start exploring the collection - download the first chapter of every title for free.

Effects of tunneling dielectrics formed by CO₂ and N₂O plasma-assisted oxidations on memory characteristics in p-channel LTPS NVM devices with ONO structure

Kyungsoo Jang[✉], Sojin Lee, Thi Cam Phu Nguyen, Heejun Park, Jungsoo Kim, Donggi Shin, Youn-Jung Lee, Youngkuk Kim¹ and Junsin Yi¹

College of Information and Communication Engineering, Sungkyunkwan University, 2066 Seobu-ro, Jangan-gu, Suwon-si, Gyeonggi-do, 16419, Republic of Korea

E-mail: bri3tain@skku.edu and junsin@skku.edu

Received 18 January 2018, revised 28 September 2018

Accepted for publication 4 October 2018

Published 24 October 2018



Abstract

Non-volatile memory (NVM) devices using carbon dioxide (CO₂) and nitrous oxide (N₂O) plasma-assisted tunneling layers have outstanding electrical properties measured at 300 K. However, the retention characteristics of NVM devices using CO₂ and N₂O plasma-assisted tunneling oxides are different at 360 K. The memory window of an NVM device using CO₂ tunneling oxide was about 2.01 V (81.7%) after 10 years at 360 K. However, there was retention charge loss in the NVM device using a N₂O tunneling layer at 360 K due to the temperature instability under negative bias. For an actual NVM device using N₂O tunneling oxide, the memory window was reduced to about 1.58 V (65.6%) after 10 years at 360 K.

Keywords: plasma-assisted oxidation, tunneling layer, LTPS, NVM, next-generation display

(Some figures may appear in colour only in the online journal)

1. Introduction

Low-temperature polycrystalline silicon (LTPS) has been widely used as an active channel semiconductor of thin-film transistors (TFTs) because the mobility of LTPS TFTs is higher than that of the conventional TFTs using amorphous silicon (a-Si) [1, 2]. For applications such as system-on-panel displays, many functional devices, including non-volatile memory (NVM) on glass, are required. In next-generation displays, the performance of NVM, one of the embedded functional devices, should be enhanced. It has been found that using a oxide/nitride/oxide structure in NVM devices enables low driving voltage, fast programming/erasing, improved memory retention, and increased endurance [3]. Advancements in ultrathin tunneling oxide have opened the path to improved performance and reliability for NVMs based

on an oxide/nitride/oxide (ONO) structure [4]. However, for NVM fabricated on a glass substrate, there were initial difficulties due to the non-uniform surface of excimer-laser-crystallized poly-Si. According to reports in the mid-2000s, more than 10 nm thick tunneling oxide was directly deposited, resulting in more than +30 V/−30 V switching voltage; however, reliability results such as retention, which is a characteristic of charges held after 10 years, was not good [5, 6]. Since the late 2000s, it has been possible to form a tunneling oxide with a thin and uniform thickness about 3 nm thick using a plasma-assisted oxidation method with nitrous oxide (N₂O) gas. This made switching voltage of about +10 V/−10 V, 70% retention property after 10 years, and 10⁵ P/E cycles possible [7, 8].

Recently, electronic devices such as smartphones and virtual reality have come into wide use. In the case of electronic devices, the heat generated during use can affect device performance. In the future, where more integration is

¹ Authors to whom any correspondence should be addressed.

expected, it is essential to improve device performance through control of heat. Thus, reliability at high temperature is one of the important issues in electronic devices. For NVM devices using tunneling oxide formed by N_2O plasma-assisted oxidation method, the electrical characteristics are excellent at room temperature. However, the effect of heat generation on the NVM device performance has not been studied. In particular, the incorporation of nitrogen (N) atoms at the insulator/channel interface can increase the temperature instability under negative-bias stress [9–12]. Thus, it is necessary to form a high-quality tunneling oxide using a gas other than N_2O . For SiO_2 tunneling oxide using other gases, oxide binding energy should be higher than that of the existing SiO_2 tunneling oxide by N_2O plasma-assisted oxidation. The O composition in the SiO_2 should be high and the defect density, such as Pb center, should be low.

In this study, the fabrication of high-performance NVM devices was performed with ultrathin tunnel layers using carbon dioxide (CO_2) and N_2O plasma-assisted oxidation method. The study compared reliability at high temperature for electronic device applications. The switching and retention characteristics of NVM devices were characterized at 300 and 360 K.

2. Experimental

A 300 nm thick buffer oxide and a 50 nm-thick a-Si film were continuously deposited on a glass substrate. The a-Si film was crystallized using a 308 nm XeCl laser. After the formation of poly-Si, ultrathin tunneling layers were formed by plasma at conditions of a substrate temperature of 180 °C and radio frequency power of 100 W. The CO_2 and N_2O gases were used as a tunneling oxide via the plasma-assisted oxidation method. A tunneling oxide of 3 nm, trapping nitride of 15 nm, and blocking oxide of 20 nm were deposited as a result. It took 4 and 3 min to form tunneling oxide of 3 nm thickness using CO_2 and N_2O plasma-assisted oxidation, respectively. The thickness of each thin film was measured by an ellipsometer (J A Woollam, VASE-VB 250). After the deposition of a gate electrode, the sample was patterned and treated by the boron ion shower method for the source and drain regions. Figure 1 shows a schematic illustration of the NVM devices with CO_2 and N_2O plasma-assisted tunnel oxides. After the fabrication of poly-Si NVM devices with plasma-assisted CO_2 and N_2O oxidation, the electrical properties of the NVM devices were examined with a semiconductor parameter analyzer (SPA, Agilent 4156C) at 300 K and at 360 K, under dark conditions. A channel width of 200 μm and channel length of 50 μm was used for the NVM devices. Furthermore, for the characteristics of ultrathin tunnel oxides, capacitance-voltage (C-V) and x-ray photoelectron spectroscopy (XPS) were also conducted. Furthermore, in this work, the threshold voltage (V_{TH}) was extracted by (drain current) $^{1/2}$ –(gate voltage) extraction method [13].

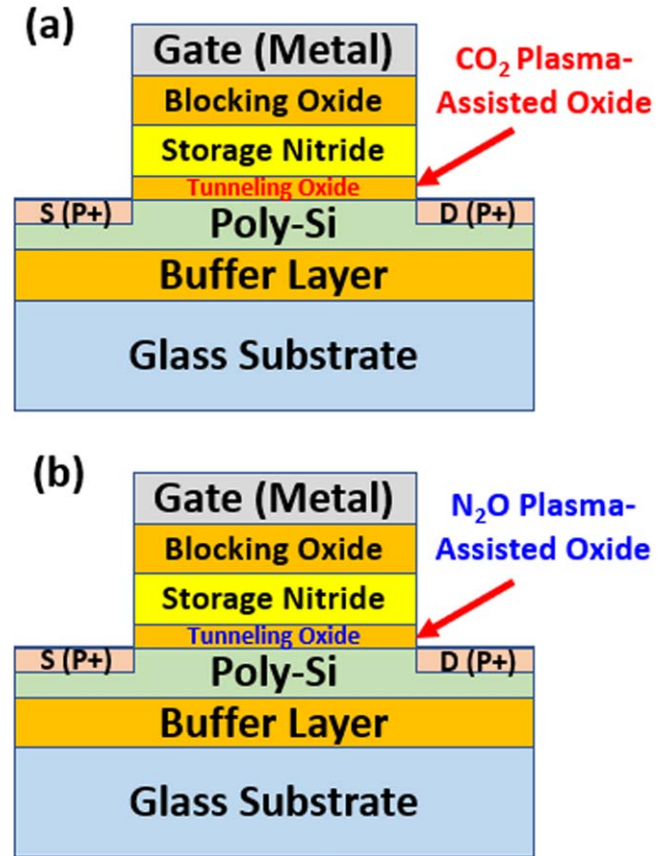


Figure 1. Schematic of NVM devices with ONO structures using (a) CO_2 and (b) N_2O plasma-assisted tunnel oxides.

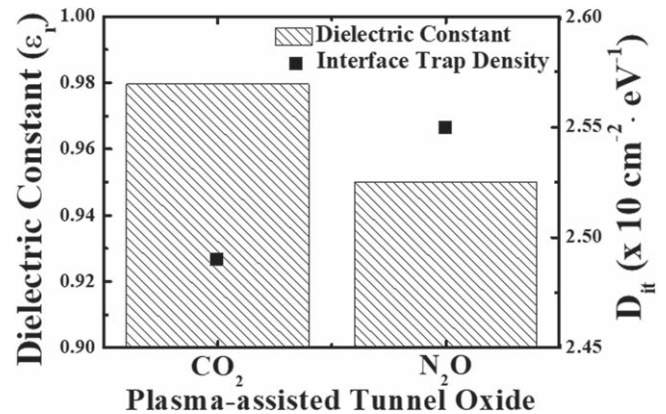


Figure 2. The dielectric constant (ϵ_r) and interface trap density (D_{it}) results of CO_2 and N_2O plasma-assisted tunnel oxides.

3. Results and discussion

Figure 2 shows the electrical properties of plasma-assisted tunneling oxides extracted by C-V measurement. The dielectric constant (ϵ_r) and interface trap density (D_{it}) of both tunneling oxides were extracted. The ϵ_r of the CO_2 plasma-assisted tunneling oxide (sample A) was about 3.2% larger than that of the N_2O plasma-assisted tunneling oxide (sample B). Generally, SiO_2 is known for its hydrophilic properties. It is expected that CO_2 plasma-assisted oxide with relatively high k-values will have greater hydrophilic properties than

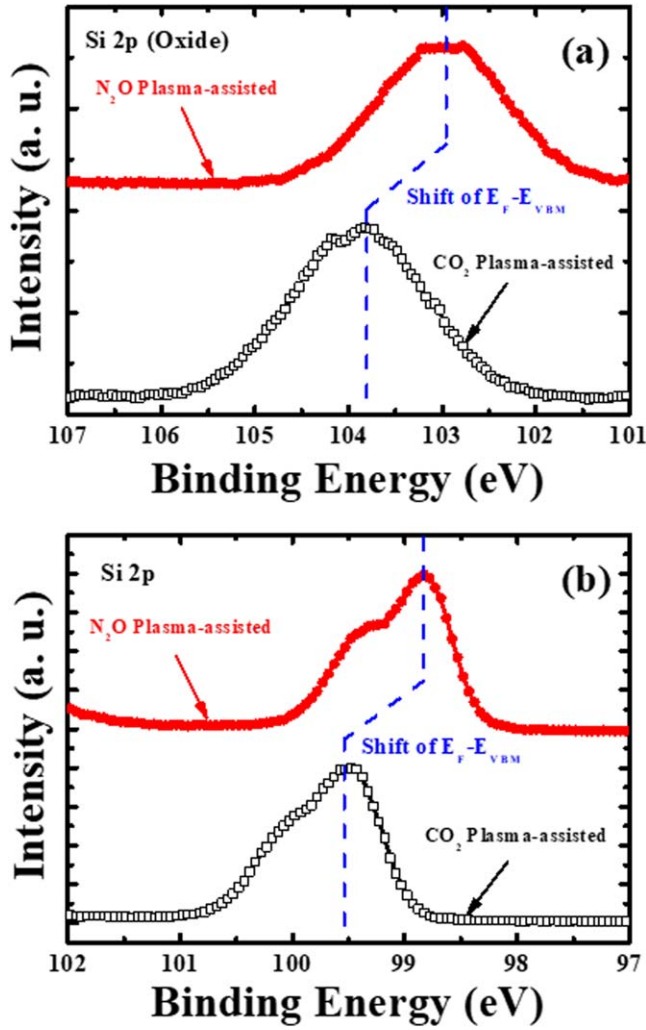


Figure 3. XPS results of (a) CO₂ and (b) N₂O plasma-assisted tunnel oxides using the Si 2p (oxide) and Si 2p peak positions.

N₂O plasma-assisted oxide. The D_{it} of sample A was $2.49 \times 10^{10} \text{ cm}^{-2} \cdot \text{eV}^{-1}$, lower than compared to the D_{it} ($2.55 \times 10^{10} \text{ cm}^{-2} \cdot \text{eV}^{-1}$) of sample B. Based on the results of the extracted ϵ_r and D_{it} characteristics, the quality of the 3 nm thick thin tunneling layer obtained through CO₂ oxidation was better than the oxide formed by N₂O oxidation.

Figure 3 shows the XPS results of the CO₂ plasma-assisted tunneling oxide (sample A) and N₂O plasma-assisted tunneling oxide (sample B) using Si 2p (oxide) and Si 2p peak positions. The Si 2p (oxide) peak positions of samples A and B are 103.7 and 103.0 eV, respectively. The general peak position of Si⁴⁺ (SiO₂) is 103.6 eV, which is like the peak position of A [14]. However, the peak position of B is moved. The peak intensity and area of Si 2p (oxide) of sample A were larger by 25.6% and 27.2%, respectively, compared to those of sample B. The chemical composition ratio of O and Si (O/Si) obtained by XPS measurement showed that sample A was 12.8% larger than sample B. The Si 2p peak position of A and B were 99.4 and 98.8 eV, respectively. Compared to the general Si 2p peak position (99.4 eV), the peak position of A was similar, but that of B was shifted. This meant the difference between Fermi-level (E_F) and valence-band maximum

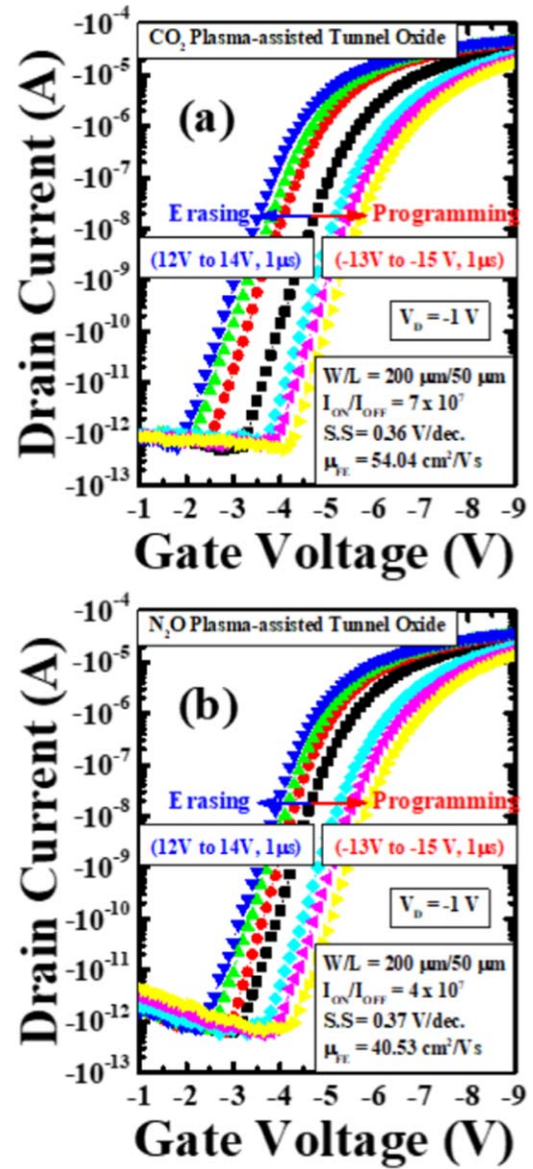


Figure 4. Transfer characteristics of the LTPS NVM devices with (a) CO₂ and (b) N₂O plasma-assisted tunneling oxides on the glass after programming and erasing.

(E_{VBM}) had shifted; it also affected the interface between the oxide and Si along with the change in the energy band diagram [9].

Figure 4 shows the transfer characteristics of the LTPS NVM devices with CO₂ plasma-assisted tunneling oxide (device A) and N₂O plasma-assisted tunneling oxide (device B) on the glass after programming and erasing. The transfer properties of the NVM device were measured at room temperature, where $V_{DS} = -1 \text{ V}$. The basic transfer characteristics of NVM devices with devices A and B were as follows: Device (A), on and off current ratio (I_{ON}/I_{OFF}) of about 7×10^7 , field-effect mobility (μ_{FE}) of $54.40 \text{ cm}^2 \text{ V}^{-1} \cdot \text{s}$, and subthreshold swing (S.S) of 0.36 V/decade; Device (B), I_{ON}/I_{OFF} of about 4×10^7 , μ_{FE} of $40.54 \text{ cm}^2 \text{ V}^{-1} \cdot \text{s}$, and S.S of 0.37 V/decade. Based on the basic transfer characteristics of NVM devices with devices A

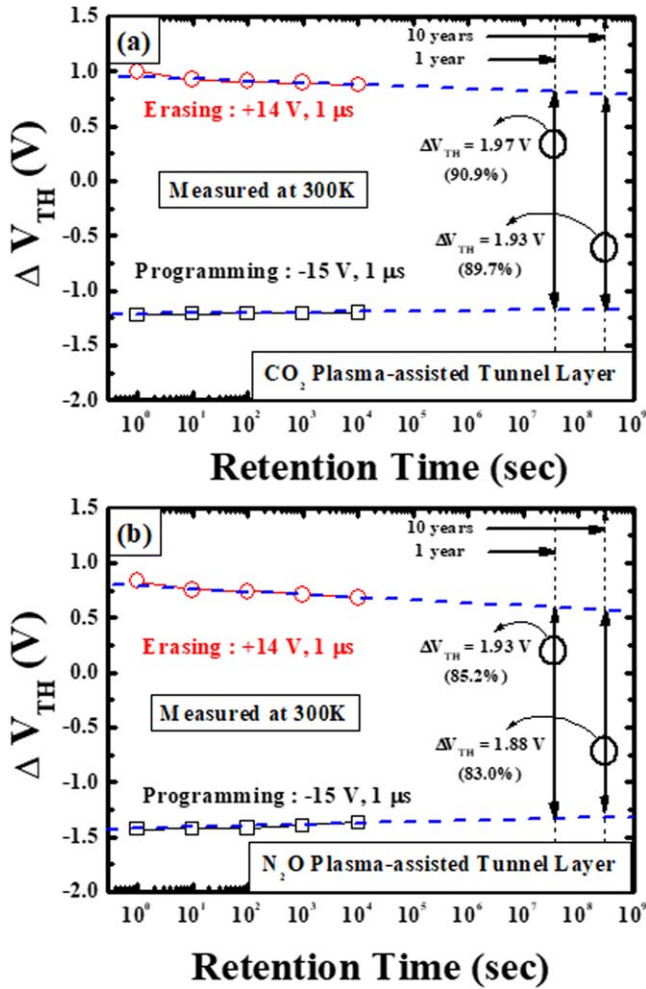


Figure 5. Charge-retention characteristics of NVM devices with (a) CO₂ and (b) N₂O plasma-assisted tunneling oxides measured at 300 K.

and B, the electrical properties of device A were better than those of device B. The programming and erasing properties of NVM were measured by using the shift of threshold voltage of transfer characteristics. The devices were programmed by applying a negative gate voltage up to -15 V for a programming pulse time of $1 \mu\text{s}$ to the control gate where $V_S = V_D = 0$, respectively. When a negative gate voltage is applied to the NVM device on glass, the holes tunnel from the valence band of the poly-Si through the tunneling oxide, and are trapped in the forbidden gap of the trapping layer. The device was erased by applying a positive gate voltage up to $+14$ V for an erasure pulse time of $1 \mu\text{s}$ to the control gate, where $V_S = V_D = 0$. When a positive gate voltage is applied to the NVM device, the electrons tunnel from the poly-Si through the tunneling oxide. The holes either recombine with the electrons trapped in the trapping layer, or the trapped holes may be emitted from the trapped state to the channel. The ΔV_{TH} of devices A and B is 2.22 and 2.26 V, respectively, at a programming voltage of -15 V and erasing voltage of $+14$ V under pulse time of $1 \mu\text{s}$. The ΔV_{TH} values over 2.2 V of both devices are large enough to apply a logic memory circuit.

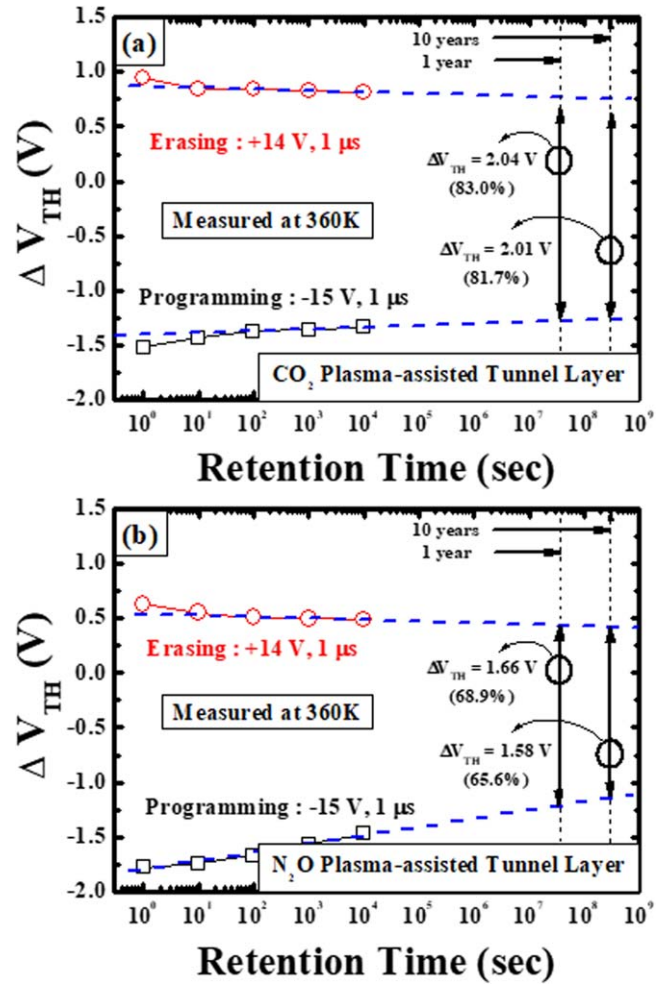


Figure 6. Charge-retention characteristics of NVM devices with (a) CO₂ and (b) N₂O plasma-assisted tunneling oxides measured at 360 K.

Figure 5 shows the charge-retention characteristics of the NVM devices with CO₂ plasma-assisted tunneling oxide (device A) and N₂O plasma-assisted tunneling oxide (device B) on glass. After applying programming and erasing voltages for $1 \mu\text{s}$, the transfer characteristics were measured at waiting durations up to 10^4 s. The ΔV_{TH} between the programming and erasing states of was 2.21 V for device A and 2.05 V for device B after 10^4 s. When making the extrapolation to 10 years, the retention of devices A and B was about 90% and 83%, respectively, of the initial memory window, corresponding to a memory window of 2.08 and 1.88 V. Although the NVM device was fabricated on rough poly-Si, the electrical characteristics of devices A and B measured at 300 K were sufficient for applying a logic memory circuit.

Figure 6 shows the charge-retention characteristics of NVM devices with CO₂ plasma-assisted tunneling oxide (device A) and N₂O plasma-assisted tunneling oxide (device B) measured at 360 K. After applying programming and erasing voltages for $1 \mu\text{s}$, transfer characteristics were measured at waiting durations up to 10^4 s. The ΔV_{TH} between the programming and erasing states of device A was 2.15 V after

10^4 s. When making the extrapolation to 10 years, the retention of the device A was about 82% of the initial memory window, corresponding to a memory window of 2.01 V. There was roughly 8% change in the retention property compared to device A at 300 K. Therefore, the electrical reliability of device A was sufficient. However, the electrical property of device B was not sufficient due to the ΔV_{TH} between the programming and erasing states being 1.58 V after 10 years. This corresponded to about 66% of the initial memory window. In particular, after 10 years of applying programming voltage of -15 V for under $1 \mu\text{s}$, the change in the voltage value (as compared to the reference of 0 V) was 0.65 V, a decrease of 36.7%. At the programming condition of 360 K and negative bias, the incorporation of nitrogen atoms at the insulator/channel interface showed temperature instability [9–12]. Thus the LTPS NVM device using CO_2 plasma-assisted tunneling oxide, with its high electrical reliability, was found to be more adaptable than the device using N_2O plasma-assisted tunneling oxide for data storage in next-generation display applications.

Figure 7 shows schematic energy band diagrams under programming status of NVM devices using CO_2 and N_2O plasma-assisted oxides as a tunnel layer. We already know that the film quality of CO_2 tunnel oxide is better than that of N_2O tunnel oxide from the analysis using the interface trap density, dielectric constant, and O/Si composition ratio. The difference between thin-film qualities is dramatically different from those at high temperature shown in figure 6. This can be explained as negative-bias temperature stress due to N. When applied to NVM with a negative voltage (programming state) applied at 360 K, it is easy to determine the cause of the retention characteristic difference. Under programming state at 360 K, in the case of NVM with the CO_2 oxidation tunnel layer, there are not many holes trapped at the interface between the poly-Si channel and the tunnel oxide, so many holes were trapped in storage nitride film. However, in the case of NVM with N_2O oxidation tunnel layer, there are many holes trapped at the interface between the poly-Si channel and the tunnel oxide, so the initial threshold voltage difference of NVM with N_2O plasma-assisted tunnel oxide was larger than that of NVM with CO_2 plasma-assisted tunnel oxide. However, many holes trapped at the interface can be easily taken off, so the threshold voltage was sharply decreased and the retention characteristics became worse.

4. Conclusion

The electrical characteristics of NVM devices with CO_2 (device A) and N_2O (device B) plasma-assisted tunneling oxides on glass were investigated. At 300 K, the difference in electrical characteristics between devices A and B was not significant. However, there was a big difference in electrical characteristics between devices A and B at 360 K, especially in terms of retention characteristics. These comparative studies could be useful in that they show that LTPS NVMs with CO_2 plasma-assisted tunneling oxides could be sufficient for next-generation display applications.

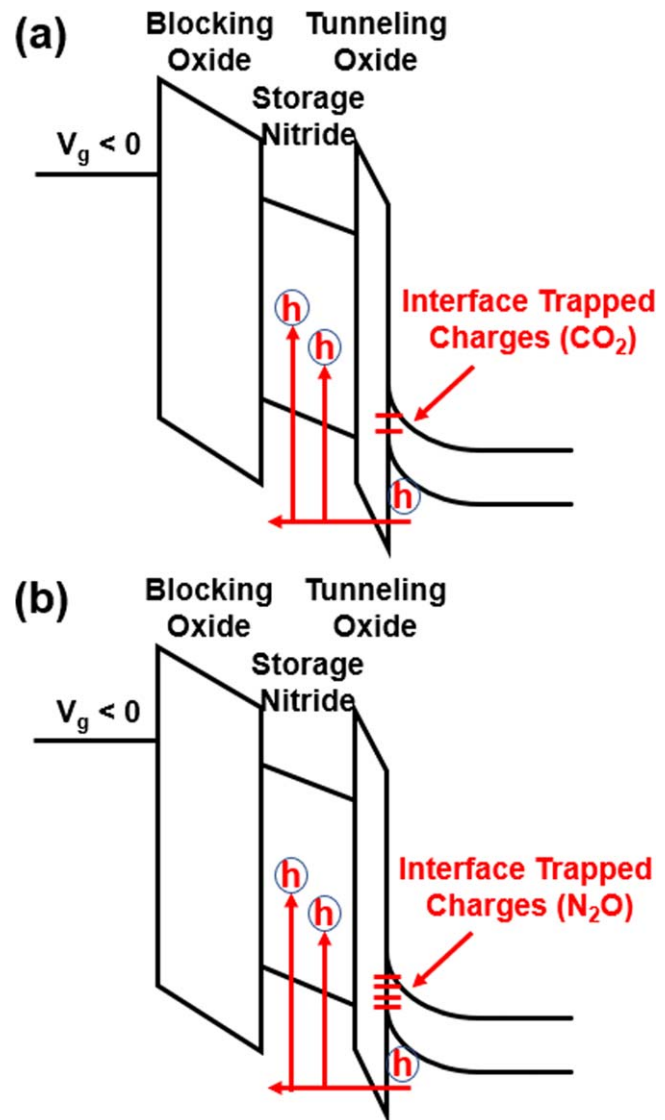


Figure 7. Schematic energy band diagrams under programming status of NVM devices using CO_2 and N_2O plasma-assisted oxides as a tunnel layer.

Acknowledgements

This research was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (NRF-2010-0020210) and by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science, ICT & Future Planning (NRF-2017R1D1A1B03034984).

ORCID iDs

Kyungsoo Jang  <https://orcid.org/0000-0002-0359-2780>

References

- [1] Uchikoga S 2002 *MRS Bull.* **27** 881
- [2] Kang M-K, Kim S J and Kim H J 2014 *Sci. Rep.* **4** 6858
- [3] White M H, Adams D A and Bu J 2000 *IEEE Circuits Devices Mag.* **16** 22
- [4] Brown W D and Brewer J E 1998 *Nonvolatile Semiconductor Memory Technology* (New York: IEEE Press)
- [5] Hsieh S-I, Chen H-T, Chen Y-C, Chen C-L and King Y-C 2006 *IEEE Electron Device Lett.* **27** 272
- [6] Chen S-C, Chang T-C, Liu P-T, Yeh P-H, Weng C-F, Sze S M, Chang C-Y and Lien C-H 2007 *Appl. Phys. Lett.* **90** 122111
- [7] Jung S, Kim J, Son H, Jang K, Cho J, Kim K, Choi B and Yi J 2008 *J. Phys. D:Appl. Phys.* **41** 172006
- [8] Duy N V, Jung S, Kim K, Son D N, Nga N T, Cho J, Choi B and Yi J 2010 *J. Phys. D:Appl. Phys.* **43** 075101
- [9] Kushida-Abdelghafar K and Watanabe K 2002 *Appl. Phys. Lett.* **81** 4362
- [10] Tsujikawa S and Yugami J 2006 *IEEE Trans. Electron Devices* **53** 51
- [11] Tan S S, Chen T P, Soon J M, Loh K P, Ang C H, Teo W Y and Chan L 2003 *Proc. Int. Conf. on Solid State Devices and Materials (Tokyo)* pp 70–1
- [12] Sakuma K, Matsushita D, Muraoka K and Mitani Y 2006 *Proc. IEEE 44th Annual Int. Reliability Physics Symp. (San Jose)* pp 454–9
- [13] Schroder D K 2008 *Semiconductor Material and Device Characterization* 3rd edn (New Jersey: Wiley)
- [14] Himpfel F J, McFeely F R, Taleb-Ibrahimi A, Yarmoff J A and Hollinger G 1998 *Phys. Rev. B* **38** 6084