Article

Journal of
Nanoscience and Nanotechnology
Vol. 16, 4783–4787, 2016
www.aspbs.com/jnn

Effects of Low Temperature Anneal on the Interface Properties of Thermal Silicon Oxide for Silicon Surface Passivation

Nagarajan Balaji[1], Cheolmin Park[1], Sungyoun Chung[2], Minkyu Ju[2], Jayapal Raja[2], and Junsin Yi[1, 2, *]

[1] Department of Energy Science, Sungkyunkwan University, 300 Cheoncheon-dong, Jangan-gu, Suwon, Gyeonggi-do 440-746, Republic of Korea
[2] College of Information and Communication Engineering, Sungkyunkwan University, 300 Cheoncheon-dong, Jangan-gu, Suwon, Gyeonggi-do 440-746, Republic of Korea

High quality surface passivation has gained a significant importance in photovoltaic industry for reducing the surface recombination and hence fabricating low cost and high efficiency solar cells using thinner wafers. The formation of good-quality SiO_2 films and SiO_2/Si interfaces at low processing temperatures is a prerequisite for improving the conversion efficiency of industrial solar cells with better passivation. High-temperature annealing in inert ambient is promising to improve the SiO_2/Si interface. However, annealing treatments could cause negative effects on SiO_2/Si interfaces due to its chemical at high temperatures. Low temperature post oxidation annealing has been carried out to investigate the structural and interface properties of Si–SiO_2 system. Quasi Steady State Photo Conductance measurements shows a promising effective carrier lifetime of 420 μs, surface recombination velocity of 22 cm/s and a low interface trap density (D_{it}) of 4×10^{11} states/cm^2/eV after annealing. The fixed oxide charge density was reduced to 1×10^{11}/cm^2 due to the annealing at 500 °C. The FWHM and the Si–O peak wavenumber corresponding to the samples annealed at 500 °C reveals that the Si dangling bonds in the SiO_2 films due to the oxygen defects was reduced by the low temperature post oxidation annealing.

Keywords: Thermal Silicon Oxide, Surface Passivation, Low Temperature Annealing, Interface Trap Density.

1. INTRODUCTION

A significant loss mechanism in industrial solar cells is recombination of charge carriers in the silicon material. To achieve high efficiency solar cells, recombination losses must be minimized.[1] The wafer thickness has been continuously decreased, due to high material costs, and the solar cells become thinner. Hence, the electrical property of surface passivation is indispensable to achieve high conversion efficiency especially for thin wafers. Passivation methods for crystalline Si solar cells can be done by (i) elimination of interface states which is effective for both *n*- and *p*-Si based solar cells; hence conversion efficiency can be improved and (ii) induction of charges in Si surface regions which prevents recombination by repelling one kind of charges.

Thermal silicon dioxide remains the main dielectric in many industrial applications[2] due to its best characteristics of an insulator-semiconductor system. SiO_2 has several features which makes it an attractive photovoltaic material. The high efficient silicon solar cells[3, 4] uses thermal oxide since it provides the adequate mean for surface passivation with reduced minority carrier loss by surface recombination. Thermally grown SiO_2 layers at high temperatures above 900 °C in oxidizing atmosphere form an SiO_2/Si interface provides all major requirements such as good surface passivation, good rear reflectance, and thermal stability in solar cell production processes. Surface recombination velocity (SRV) less than 2.4 and 11.8 cm/s on *n*- and *p*-type floating-zone (FZ) c-Si wafers, respectively

*Author to whom correspondence should be addressed.

was achieved by Kerr et al.[5] The formation of good-quality SiO_2 films and SiO_2/Si interfaces at low processing temperatures is a prerequisite for improving the conversion efficiency of industrial solar cells with better passivation. High-temperature annealing in inert ambient is promising to improve the SiO_2/Si interface. However, annealing treatments could cause negative effects on SiO_2/Si interfaces at high temperatures. Hence understanding the nature of the SiO_2/Si interface in thermally oxidized silicon and its dependence on process is crucial for effective passivation. The SiO_2/Si interface formed by thermal oxidation has been shown to be neither abrupt on an atomic scale, nor strain free.[6] Several factors contribute to interfacial bond-strain. Differences in linear thermal expansion coefficients contribute to thermal strain when the oxides grown at higher temperatures. These level of interfacial bond-strain cannot be relieved elastically. In this study, low temperature post oxidation annealing has been carried out to investigate the structural and interface properties of Si–SiO_2 system.

2. EXPERIMENTAL DETAILS

For oxidation characterization, *p*-type Czochralski (CZ)-grown crystalline Si wafers with resistivity of 1–2 Ω-cm were first cleaned with SC-1(NH_4OH:H_2O_2:DI-H_2O in the ratio of 1:1:5). After SC-1 cleaning, the wafers were cleaned by dipping in 10% HCl and 10% HF to remove the oxide formed during the SC-1 cleaning and the wafers were then rinsed in DI water. After purging the quartz chamber with N_2, the wafers were immediately loaded into the quartz chamber at 600 °C. Thermal oxide was grown in nominally dry oxidation ambient by flowing oxygen gas at temperature in the range of 900 to 1100 °C for fixed oxidation time. Annealing was performed at 500 °C and 700 °C for 30 min in the ambient of molecular nitrogen with constant flow rate and then sample was unloaded at the same temperature. The whole process of thermal oxidation and post oxidation annealing (POA) cycle is summarized in Figure 1. The thickness of SiO_2 was fixed at ~20 nm for all samples. The thicknesses of the SiO_2 films were estimated by using Spectroscopic ellipsometer (SE), VASE®, J. A. Woollam. The minority carrier lifetime (τ_{eff}) of the passivated wafers were measured by the quasi-steady-state photo-conductance (QSSPC) method, using a commercial WCT-120 photo-conductance set-up from Sinton Consulting. In order to fabricate the Metal-Oxide-Semiconductor

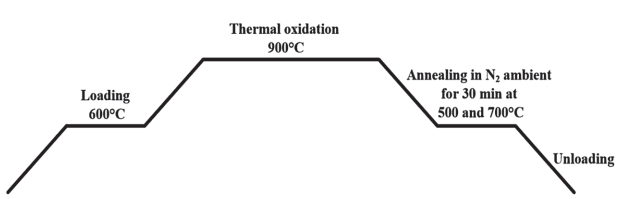

Figure 1. Process flow for thermal oxidation and post oxidation annealing of SiO_2 layer.

(MOS) structures, grown oxide layer on the rear side of the silicon surface was fully removed using Buffer Oxide Etchant (BOE) by protecting the front surface of the silicon by positive photoresist. Ohmic contact was performed on the front surface with the deposition of the Al (200 nm) using thermal evaporation method in the vacuum range of 10^{-6} Torr. To estimate the shift in flat-band voltage and the interface trap states (D_{it}), high-frequency capacitance–voltage (C–V) of the MOS structure was characterized using an MDC meter (model 825). The molecular vibration mode and functional groups in the SiO_2 films were characterized by Fourier Transform Infrared (FTIR) spectroscopy (Prestige-21 spectrometer, Shimadzu). The X-rays photoelectron spectroscopic (XPS) ESCA2000 (VG microtech) system with monochromatic Al K (1486.6 eV) source was used to analyze the chemical composition and binding states of the SiO_2 films.

Solar cells were fabricated using *p*-type c-Si wafers of thickness 200 ± 25 μm with a resistivity of 0.5–2 Ωcm and saw damage depth of 3 μm. *N*-type emitter layer was formed by phosphorous diffusion using $POCl_3$ as source material at 830 °C for 20 minutes. Subsequent to n^+ emitter diffusion, phosphorous silica glass removal was performed using a diluted HF solution for a few minutes. Thermally oxidized SiO_2 layers of 20 nm thick were used as passivation layer whereas a silicon nitride was deposited on the front side of wafers using plasma-enhanced chemical vapor deposition for anti-reflection (AR) coating. High throughput metal contacts were formed on front and back surface using standard silver paste and aluminum by screen-printing technique. The samples were then baked at 150 °C and co-fired in a conveyer belt furnace. The speed of the belt was 120–170 inch/minute and the temperatures at different zones of the furnace were 450, 500, 600 and 940 °C. The samples were edge isolated by laser and the solar cell performance was characterized by I–V measurement under air mass 1.5 global (100 mW/cm^2, AM1.5G) condition at 25 °C.

3. RESULTS AND DISCUSSION

Figure 2 shows the typical high frequency C–V curve of POA samples with different annealing temperature in MOS structure. The variation in temperature was fixed as 500 °C, 700 °C with a gate bias sweep from −6 V to 2 V. This was done by performing the high frequency C–V measurements at room temperature. The flat band voltage (V_{FB}) was calculated by comparing the reference curve (900 °C). A noticable positive flat band voltage shift in the characterisitic of the sample that received the annealing temperature of 500 °C is considered to be caused by the variation in the fixed oxide charge (Q_f). A voltage shift in the same direction is observed for the 700 °C. However there is also an evident stretch out of the C–V for both samples. The entire shift is due to changes in the interface and oxide charge.

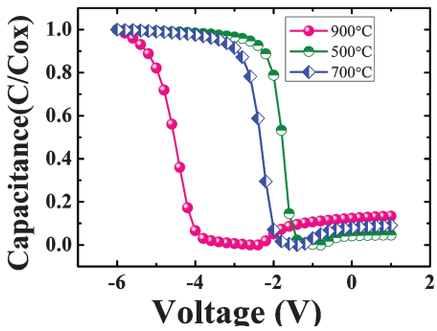

Figure 2. A typical plot of high frequency CV curves of the MOS structure of the SiO_2 films annealed at different temperatures.

The other noticeable feature of the SiO_2 films contributing to effective passivation is the interface trap states (D_{it}). The D_{it} of the SiO_2 films with different POA is shown in Figure 3, in which the D_{it} of the interface between the SiO_2 and the Si surface was determined by high frequency capacitance method developed by Terman at room temperature.[7] For the oxides annealed at 500 and 700 °C generated interface states are minimized with a value of about 4×10^{11} cm^{-2} eV^{-1} and 8×10^{11} cm^{-2} eV^{-1} respectively. The maximum value of generated interface states is about 16×10^{11} cm^{-2} eV^{-1} for 900 °C.

The D_{it} is related to the structural defects at the insulator/semiconductor surface. It is commonly accepted that the amount of fixed charge and the D_{it} depend on the bond density within the films. Lucovsky et al. developed a model for the positive fixed charge Q_f, and D_{it} generation at SiO_2/Si interface. The amount of positive fixed charge and interface trap states is directly proportional to ≡Si–O–Si≡, H–O–Si≡, and ≡Si–H bonds:[8]

$$\equiv\text{Si–H} + \equiv\text{Si–O–Si}\equiv + h^+ \rightarrow \equiv\text{Si}^0 + \text{H–O}^+\text{–(Si}\equiv)_2\text{:}$$
$$\text{generation of } D_{it} \text{ and } Q_f(O_3^+) \quad (1)$$

$$\text{Si–Si} + (\text{O}) \rightarrow (\text{Si–O})^+ + \text{Si}\equiv + e^-$$
$$(\text{Si–O})^+ + \text{Si}\equiv + e \rightarrow \text{Si–O–Si}^-\text{: generation of } Q_f(O_3^+) \quad (2)$$

At high annealing temperature Si–O bond destruction occurs creating oxygen deficiency defects[9, 10] which may be responsible for the increased interface state density.

From the data of V_{FB}, which was obtained from the C–V measurement for MIS structures at 1.0 MHz, the value of the Q_f at the insulator may be evaluated as[11]

$$Q_f = \frac{c_i}{A}(\triangle\varphi_{ms} - V_{FB}) \quad (3)$$

where C_i is the insulator capacitance, A is the area of the diode, and $\Delta\varphi_{ms}$ is the work function difference between the metal and the silicon (aluminum was used as the metal electrode in this study hence, $\Delta\varphi_{ms} = -0.87$ eV). For the oxides annealed at 500 and 700 °C generated fixed charges are about 2×10^{11} and 1×10^{11} for 700 °C and 500 °C respectively as depicted in Figure 4. From Eq. (2) it can be explained as $(Si–O)^+$ silicon–oxygen complexes are responsible for the formation of a fixed charge in the oxide. The first process gives rise to $(Si–O)^+$ positively charged complexes and to an equal number of three coordinated silicon atoms ≡Si bonded to silicon atoms at the silicon surface; these atoms can act as surface states. An increase in temperature brings about an enhancement of the second process, i.e., annihilation of the $(Si–O)^+$ complexes and, correspondingly, a decrease in the fixed charge. Thus the reduced Q_f is attributed to the complete relaxation of internal stresses due to processes of structural rearrangement in SiO_2/Si interface.

Figure 5(a) shows the absorption spectra in the infrared region for the POA SiO_2 films with different temperatures. The peak wave number of the optical absorption band caused by the Si–O–Si anti-symmetric stretching vibration mode and the full-width at haft maximum (FWHM) of the absorption band as a function of different POA temperatures is also depicted in Figure 5(a). Large absorption peak corresponding to the Si–O–Si antisymmetric stretching at 1064 cm^{-1} is observed. To elucidate the reason for altering of D_{it} with variation of annealing temperature, the bond densities of Si–O–Si within the films as a function of different annealing temperature was calculated from Figure 5(b) we can learn that the wave number increased

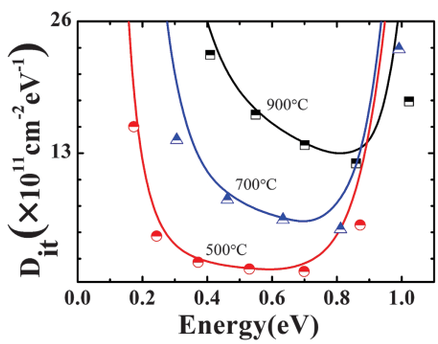

Figure 3. The interface trap density (D_{it}) of the SiO_2 films annealed at different temperatures.

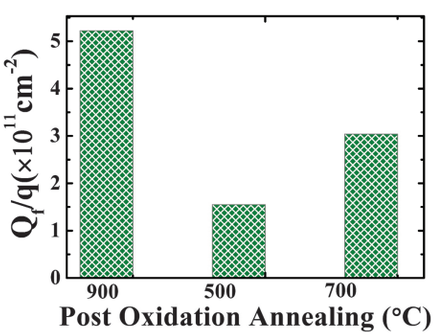

Figure 4. The oxide fixed charge (Q_f) of the SiO_2 films annealed at different temperatures.

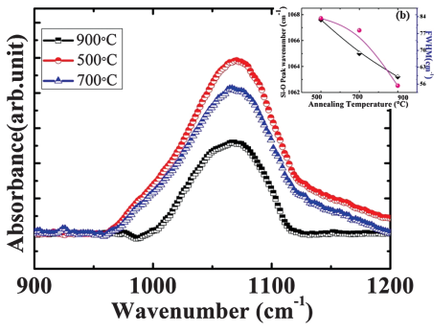

Figure 5. (a) The typical FT-IR spectra for SiO_2 films annealed at different temperatures (b) FTIR analysis of Si–O bonding concentration and its FWHM variation SiO_2 films annealed at different temperatures.

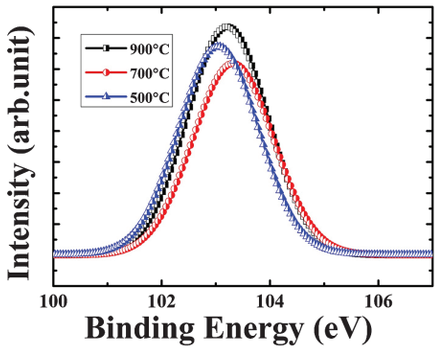

Figure 7. High resolution XPS spectra of the representative silicon dioxide film annealed at different temperatures.

to 1067 cm^{-1}, with FWHM of 84 cm^{-1} with decreasing the POA temperature. It is well known that the shift of the Si–O–Si absorption peak towards a lower wave-number, with wider FWHM results in larger silicon content inside the films. As a consequence the films composition of SiO_2 was shifted from oxygen-rich phase to silicon-rich phase.[11]

Figure 6 shows the change in lifetime and surface recombination velocity (S_{eff}) in CZ silicon wafers as a function of POA temperature. The oxide annealed at higher temperature (900 °C) had a high S_{eff}. The surface recombination velocity of CZ silicon wafers coated SiO_2 films decreases with decrease in annealing temperature. This means that there was a high density of trap states for the effective minority carrier lifetime at the interface of the oxide annealed at 900 °C. The maximum effective lifetime gave the minimum S_{eff} of ~22 cm/s. The highest τ_{eff} (420 μs) and lowest interface trap states for the oxide annealed at 500 °C indicates that the formation of neutralization of defect of interface states at the SiO_2/Si interface plays an important role in surface passivation.

The surface composition of the SiO_2 films after annealing was characterized by XPS and is shown in Figure 7. The Si 2*p* spectra can be interpreted in terms of five oxidation states Si^0, Si^{1+}, Si^{2+}, Si^{3+} and Si^{4+}. The increasing electronegativity of the Si–O bond relative to the Si–Si bond results in a shift to higher binding energy of the core–level electrons in Si atom. The binding energies for the progression of Si^0 to Si^{4+} range from approximately 99.3 to 103.3 eV with a shift of 1 eV per Si–O bond.[12–14] The symmetrical peak at 103 eV corresponding to Si^{4+} in SiO_2 indicates that almost stoichiometric SiO_2 films was obtained. The contributions of the intermediate Si peaks corresponding to the sub oxide phases become smaller while Si^{4+} peak for SiO_2 and Si^0 peak for elemental Si are dominant. This observation indicates that the unstable sub oxides have separated into two more stable Si–Si_4 and Si–O tetrahedras. Thus, there is a clear phase separation of the SiO_2 films after annealing at 500 °C.

In order to demonstrate the potential of the surface passivation of the SiO_2 with different post oxidation annealing for high-efficiency silicon solar cells, simplified passivated emitter cells were fabricated on *p*-type CZ c-Si substrates. The illuminated current–voltage characteristics of the c-Si solar cells fabricated for SiO_2 with POA at 500 and 700 °C were observed by the AM 1.5 global spectrums, is shown in Figure 8. The short circuit current density (J_{sc}), the open circuit voltage (V_{oc}), and the conversion efficiency of the c-Si solar cell fabricated for the samples annealed at 500 °C were 37.4 mA/cm^2, 635 mV, and 18.36%, respectively, whereas the solar cell fabricated for the samples annealed at 700 °C were 37 mA/cm^2, 629 mV, and 17.87%, respectively. The higher V_{oc} of the c-Si solar

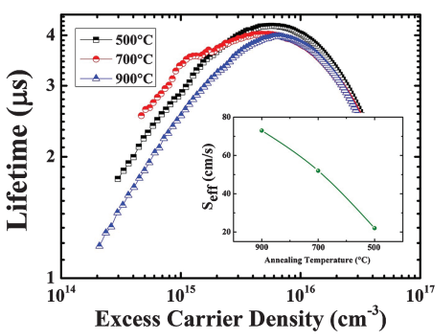

Figure 6. Lifetime and surface recombination velocity of the SiO_2 films as a function of annealing temperature.

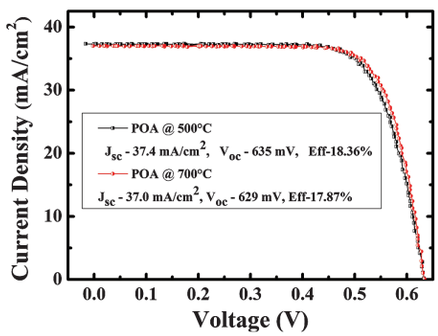

Figure 8. Illuminated voltage current characteristics of CZ Si solar cells using SiO_2 as a passivation annealed at different temperatures.

cells was achieved with highest passivation ability of low temperature annealing.

4. CONCLUSION

Structural and interface properties of Si–SiO_2 system with low temperature post oxidation annealing has been investigated. Effective carrier lifetime of 420 μs, surface recombination velocity of 22 cm/s and a low interface trap density of 4×10^{11} states/cm^2/eV were obtained after annealing at 500 °C. The fixed oxide charge density was also reduced to 1×10^{11}/cm^2 due to the annealing at 500 °C. The FWHM and the Si–O peak wavenumber corresponding to the samples annealed at 500 °C reveals that the Si dangling bonds in the SiO_2 films due to the oxygen defects was reduced by the low temperature post oxidation annealing. Finally, simplified passivated emitter solar cells were fabricated on c-Si substrates showing highest efficiency of 18.36% with SiO_2 films act as a passivation layer. These results indicate that the passivation quality of the SiO_2 films should be carefully tuned in order to obtain the maximum efficiency for c-Si solar cells.

Acknowledgment: This work was supported by the Human Resources Development program (No. 2014 4030200580) of the Korea Institute of Energy Technology Evaluation and Planning (KETEP) grant funded by the Korea government Ministry of Trade, Industry and Energy and this research was also supported by the Global Excellent Technology Innovation of the Korea Institute of Energy Technology Evaluation and Planning (KETEP), granted financial resource from the Ministry of Trade, Industry and Energy, Republic of Korea (No. 2013 5020910050).

References and Notes

1. A. G. Aberle, *Prog. Photovolt. Res. Appl.* 8, 473 (**2000**).
2. T. Hiramatsu, T. Matsuda, H. Furuta, H. Nitta, T. Kawaharamura, C. Li, M. Furuta, and T. Hirao, *Jpn. J. Appl. Phys.* 49, 03CA03 (**2010**).
3. J. Zhao, A. Wang, and M. A. Green, *Prog. Photovolt. Res. Appl.* 7, 471 (**1999**).
4. M. J. Kerr and A. Cuevas, *Semicond. Sci. Technol.* 17, 35 (**2002**).
5. J. Park, Y. Kim, S. Lee, Y. Lee, S. Q. Hussain, N. Balaji, and J. Yi, *Transactions on Electrical and Electronic Materials* 13, 192 (**2012**).
6. D. E. Aspnes and J. B. Theeten, *Phy. Rev. Lett.* 43, 1046 (**1979**).
7. F. T. Himpsel, F. R. McFeely, J. A. Yarmoff, and G. Hollinger *Phys. Rev. B* 38, 6084 (**1988**).
8. S. Jung, D. Gong, and J. Yi, *Sol. Energy Mater. Sol. Cells* 95, 546 (**2011**).
9. G. Lucovsky, Z. Jing, and D. Lee, *J. Vac. Sci. Techol. B* 14, 2832 (**1996**).
10. W. L. Warren, D. M. Fleetwood, M. R. Shaneyfelt, J. R. Schwank, P. S. Winokur, R. A. B. Devine, and D. Mathiot, *Appl. Phys. Lett.* 64, 3452 (**1994**).
11. N. Balaji, C. Park, Y. Lee, S. Jung, and J. Yi, *Vacuum* 96, 69 (**2013**).
12. T. Sameshima, K. Sakamoto, Y. Tsunoda, and T. Saitoh, *Jpn. J. Appl. Phys.* 37, L1452 (**1998**).
13. F. G. Bell and L. Ley, *Phys. Rev. B* 37, 8383 (**1988**).
14. S. Hayashi, S. Tanimoto, and K. Yamanoto, *J. Appl. Phys.* 68, 5300 (**1990**).
15. B. H. Augustine, E. A. Irene, Y. J. He, K. J. Price, L. E. McNeil, K. N. Christensen, and D. M. Maher, *J. Appl. Phys.* 78, 4020 (**1995**).

Received: 10 February 2015. Accepted: 1 June 2015.